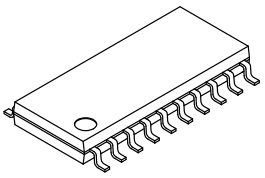
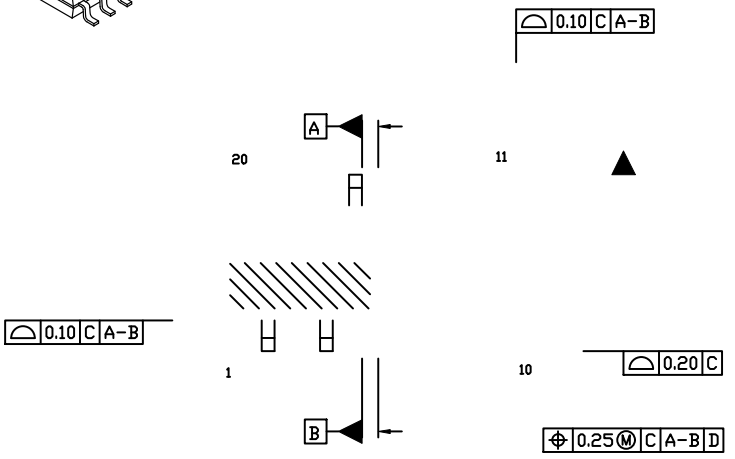
SOIC20 NB LESS PIN 17 & 19
CASE 751EZ
ISSUE O

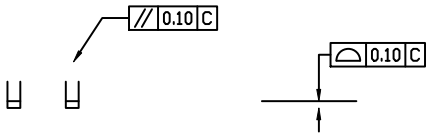
NOTE 4
DATE 23 SEP 2019



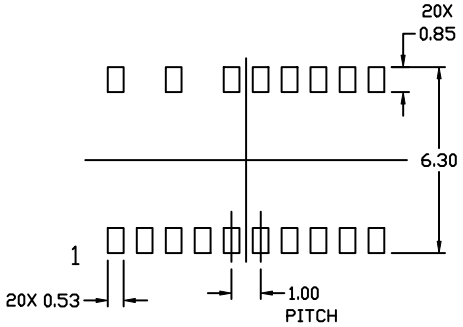
NOTE 5



TOP VIEW



SIDE VIEW



RECOMMENDED
MOUNTING FOOTPRINT

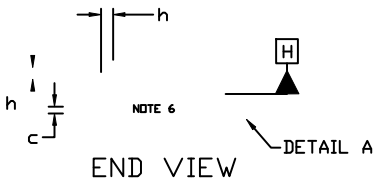
* For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual,

NOTE 4

FROM THE TIP.

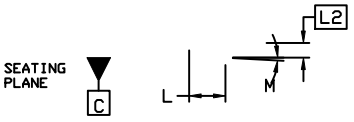
PROTRUSIONS, OR GATE BURRS BUT
MISMATCH. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15 mm PER SIDE. DIMENSIONS D AND E1 ARE DETERMINED AT DATUM H.

6. A1 IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE



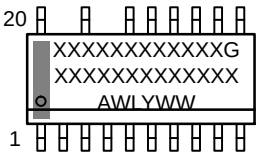
END VIEW

			MAX.
			1.70
			0.20
b	0.31	0.41	0.51
c	0.10	0.20	0.25
	9.80	9.90	10.00
E	5.90		6.10
	3.80		4.00
			0.50
			0.85
			8°



DETAIL A

GENERIC
MARKING DIAGRAM*



XXXXX	= Specific Device Code
A	= Assembly Location
WL	= Wafer Lot
YY	= Year
WW	= Work Week
G	= Pb ïFree Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb ïFree indicator, “G” or microdot “ ”, may or may not be present. Some products may not follow the Generic Marking.