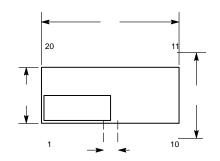
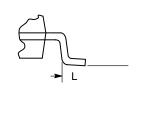
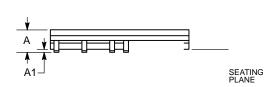
SOIC20 NB LESS PINS 2, 4 & 19 CASE 751BS ï01 ISSUE O

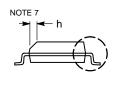
DATE 28 APR 2011

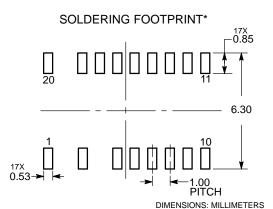
SCALE 1:1











*For additional information on our Pb ïFree strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

NOTES:

- DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.

 CONTROLLING DIMENSION: MILLIMETERS.

 DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION.
 ALLOWABLE PROTRUSION SHALL BE 0.10 TOTAL IN EXCESS

 OF THE b DIMENSION. DIMENSION b APPLIES TO THE FLAT
 PORTION OF THE LEAD AND SHALL BE MEASURED BETWEEN
 0.13 AND 0.25 FROM THE TIP
- PORTION OF THE LEAD AND SHALL BE MEASURED BETWEEN 0.13 AND 0.25 FROM THE TIP.
 DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH,
 PROTRUSIONS, OR GATE BURRS BUT DO INCLUDE MOLD MISMATCH. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15mm PER SIDE. DIMENSIONS D AND E1 ARE DETERMINED AT DATUM H.
 DATUMS A AND B ARE TO BE DETERMINED AT DATUM H.
 A1 IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEAT ING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.
 CHAMFER FEATURE IS OPTIONAL IF NOT PRESENT, THEN A PIN ONE IDENTIFIER MUST BE LOCATED IN THIS AREA.



GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code = Assembly Location

WL = Wafer Lot = Year WW = Work Week = Pb ïFree Package G

*This information is generic. Please refer to device data sheet for actual part marking. Pb ïFree indicator, "G" or microdot " ", may or may not be present.