

MECHANICAL CASE OUTLINE  
PACKAGE DIMENSIONS

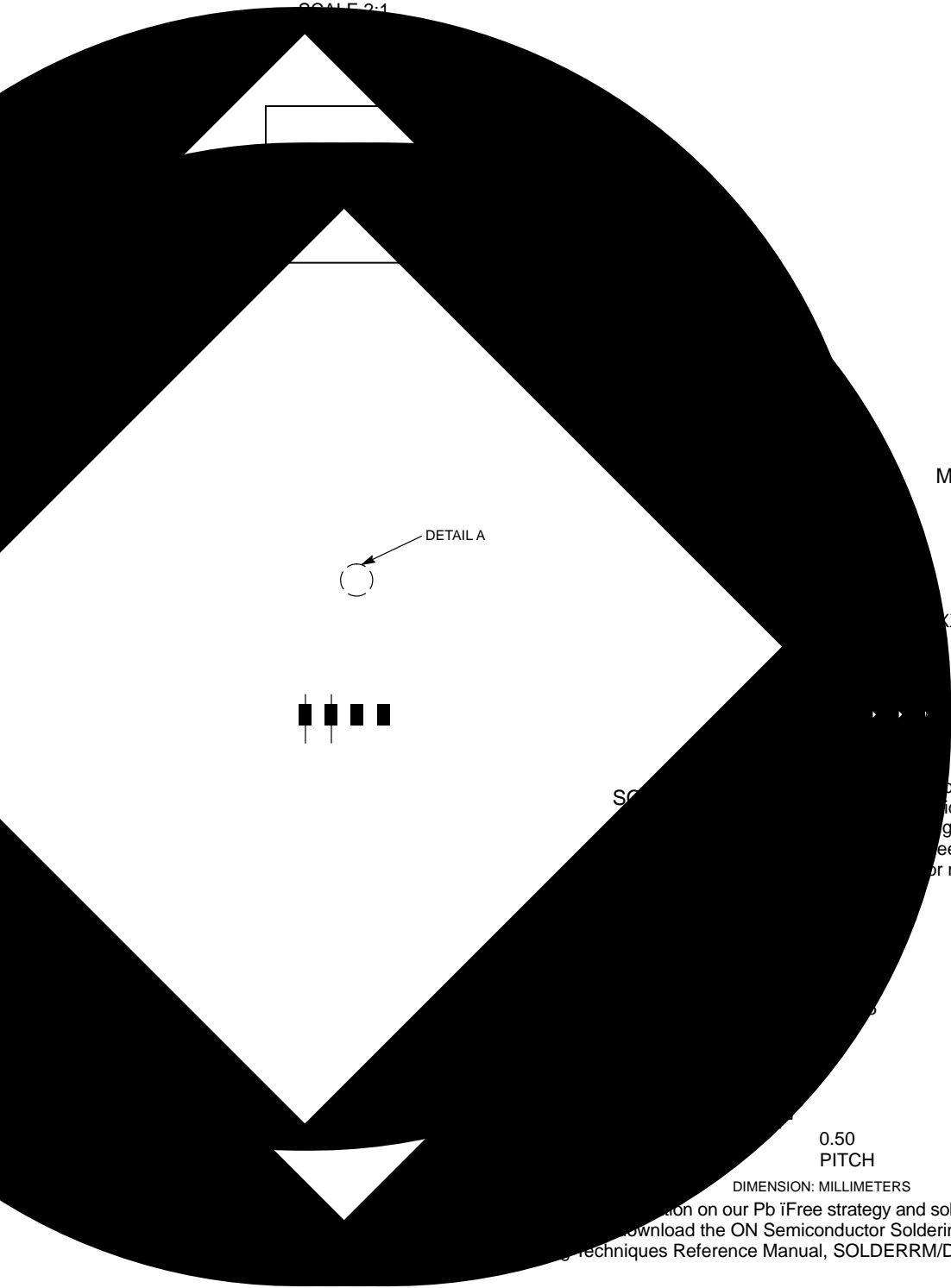
ON Semi



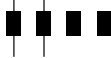
DFN8 3x3, 0.5P  
CASE 506BJ i01  
ISSUE O

DATE 08 NOV 2007

SCALE 2:1



DETAIL A



GENERIC  
MARKING DIAGRAM\*

○ 8

- XXX = Specific Device Code
- = Assembly Location
- = Wafer Lot
- = Year
- = Work Week
- = Pb iFree Package

(microdot may be in either location)  
 Information is generic. Please refer to the device data sheet for actual part marking.  
 \*Pb-free indicator, "G" or microdot " ", may not be present.

0.50  
PITCH

DIMENSION: MILLIMETERS

For more information on our Pb iFree strategy and soldering techniques, please visit our website or  
 download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.