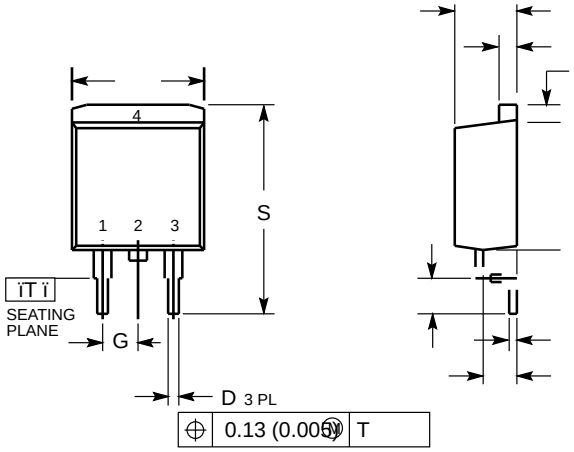
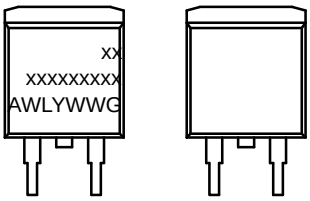


STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 2:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

STYLE 3:
PIN 1. ANODE
2. CATHODE
3. ANODE
4. CATHODE

GENERIC
MARKING DIAGRAM*



xx = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week(Assembly Location)]T uevice-6 nC3E7295.9(PbGRAM*)]T3 /TT4 0 3 -3.6 Lo 0 g