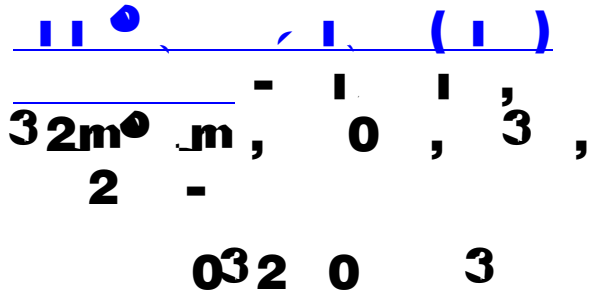


Your Feedback is Important to Us 





- Typical $R_{DS(ON)} = 32 \text{ m}\Omega$ @ $V_{GS} = 18 \text{ V}$
 - Ultra Low Gate Charge ($Q_{G(tot)} = 55 \text{ nC}$)
 - High Speed Switching with Low Capacitance ($C_{OSS} = 114 \text{ pF}$)
 - 100% Avalanche Tested
 - This Device is Halide Free and RoHS Compliant with exemption 7a, Pb-Free 2LI (on second level interconnection)
-
- SMPS, Solar Inverters, UPS, Energy Storage, EV Charging Infrastructure

($T_J = 25^\circ\text{C}$ unless otherwise noted)

Drain-to-Source Voltage	V_{DSS}	650	V
Gate-to-Source Voltage	V_{GS}	-8/+22	V
Continuous Drain Current	$T_C = 25^\circ\text{C}$	I_D	50 A

Thermal Resistance, Junction-to-Case (Note 4)	$R_{\theta JC}$	0.80	°C/W
Thermal Resistance, Junction-to-Ambient (Note 4)	$R_{\theta JA}$	40	

4. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.

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Operation Values of Gate-to-Source Voltage

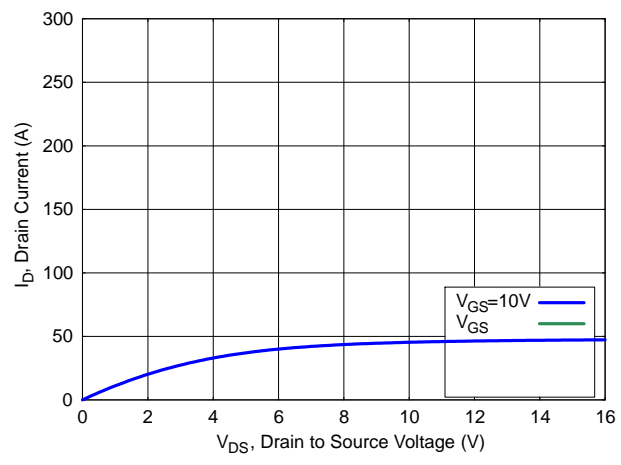


(T_J = 25°C unless otherwise specified) (continued)

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Turn-On Delay Time	t _{d(ON)}	V _{GS} = -3/18 V, V _{DD} = 400 V, I _D = 15 A, R _G = 4.7 Ω, T _J = 175°C	-	7.8	-	ns
Turn-Off Delay Time	t _{d(OFF)}	(Notes 5, 6)	0.08	63.7228	698.57	14.4 ref 449.405 693.12881 14.4 ref 449.405 693.12881









TO-247-4LD
CASE 340CJ
ISSUE A

DATE 16 SEP 2019

A E A B
A2 E1 \emptyset p1
D2

E/2 Q

D D1

\emptyset

L1

b2 A1

b1 (3X) L

1 4

e1 b(4X) c

e 2X

\oplus 0.254 (M) B A (M)

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