Your Feedback is Important to U[redacted]

Figure 1. Typical USB 2.0 Application Circuit

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Input Voltage, operating, steady−state (V_{CC} to GND) Transient (100 ms)	V_{CC}	−0.3 to +10 −0.3 to +10	V
Output Voltage, operating, steady−state (SRC to GND)	V_{OUT}	−0.3 to +20	V
Voltage range on ILIM pin	V_{ILIM}	−0.3 to +20	V
Voltage range on Enable pin	V_{EN}	−0.3 to 5	V
Voltage range on FLAG pin	V_{FLAG}	−0.3 to 6	V
Voltage range on all other pins		−0.3 to 5	V
Electrostatic Discharge Human Body Model (All pins) Charged Device Model (All pins) IEC61000−4−2 Contact (Source pins, with 22 μF C_{SOURCE} condition)	ESD	 ±2 ±1 ±7	kV

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality

ELECTRICAL CHARACTERISTICS (Unless otherwise noted: V_{CC} = 5 V, C_L = 22 μF, R_{limit} = 15 Ω, T_A = −40 to 125°C)

Characteristics	Symbol	Min	Typ	Max	Unit
POWER FET					

APPLICATIONS INFORMATION

Basic Operation

This device is a self−protected, resettable, electronic fuse. It contains circuits to monitor the input voltage, output voltage, output current and die temperature.

On application of the input voltage, the device will apply the input voltage to the load based on the restrictions of the controlling circuits. The output voltage, which is controlled by an internal dv/dt circuit, will slew from 0 V to the rated output voltage in 1 ms.

The device will remain on as long as the temperature does not exceed the 175°C limit that is programmed into the chip.

The internal current limit circuit does not shut down the part but will reduce the conductivity of the FET to maintain a constant current at the internally set current limit level. The input overvoltage clamp also does not shutdown the part, but will limit the output voltage in the event that the input exceeds the Vclamp level. This operation can be seen in Figure 5.

An internal charge pump provides bias for the gate voltage of the internal n−channel power FET and also for the current limit circuit. The remainder of the control circuitry operates between the input voltage (VCC) and ground.

The VCC line can generate spike noise in fast transient conditions such as short circuit, and this high peak can cause over−stress and malfunction. To prevent this, a low ESR capacitor (i.e. MLCC) of at least 47 μF is required.

Reverse Current Protection

The NIS6350 monitors and protects against reverse current events, which can be the result of a malfunction in the power supply or noise induced in the input voltage rail under certain load characteristics (for example, when the load is largely capacitive).

The protection mechanism disables the eFuse's output and triggers when the reverse voltage drop exceeds 100 mV in magnitude and this condition remains for at least 4 μs.

The NIS6350 automatically re−enables its output once the input voltage exceeds the output voltage for at least 100 μs.

Overvoltage Clamp

The overvoltage clamp consists of an amplifier and reference. It monitors the output voltage and if the input voltage exceeds the Vclamp voltage, the gate drive of the main FET is reduced to limit the output. This is intended to allow operation through transients while protecting the load. If an overvoltage condition exists for many seconds, the device may overheat due to the voltage drop across the FET combined with the load current. In this event, the thermal protection circuit would shut down the device.

The Vc_SEL pin can be used to select the Vclamp level. By allowing this pin to float high, the Vclamp value will be set to 6.2 − 7.5 V. By pulling this pin low (to 0V), the Vclamp value will be set to 5.6 − 6.5 V. This allows the NIS6350 to be used in both short and long haul USB applications where the VBUS voltage is adjusted for cable loss compensation. This operation can be seen in Figure 5.

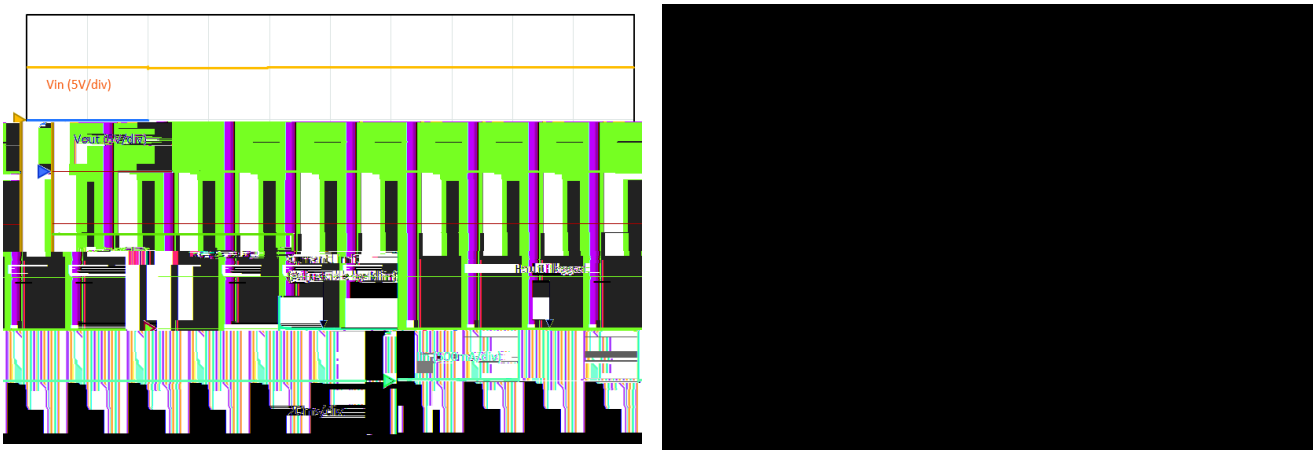
Thermal Protection

The NIS6350 includes an internal temperature sensing circuit that senses the temperature on the die of the power FET. Operation on o

Latching vs. Auto−Retry

This device features two options regarding its reset ability after a thermal shutdown event. These are called latching and auto−retry which are respectively marked MT1 and MT2 as part number suffixes. Upon reaching a thermal shutdown state, a latching device (MT1) will remain shutdown with no power supplied to the output (SRC pins). The only way to reset the device is to either perform a power cycle on the VCC bus or pull the EN pin low (<0.4 V). By doing either of these actions, the fault state is cleared and the device is allowed to pull−up the output to its normal, high state.

Instead of remaining in thermal shutdown, an Auto−retry device (MT2) will automatically attempt to pull up the output once the die temperature cools to < 135°C. If the fault remains on the output during this attempt, the device will once again enter a short period of current limiting that will eventually lead to thermal shutdown for which the auto−retry process will repeat indefinitely.



Latch version | Auto−Retry version

Figure 4. Output Short Circuit

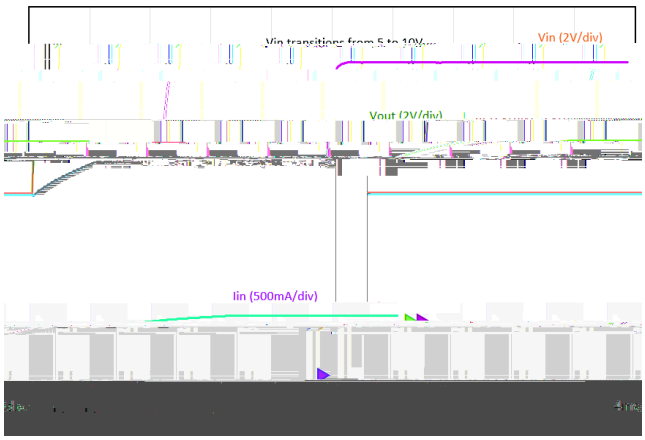


Figure 5. Output Voltage Protection

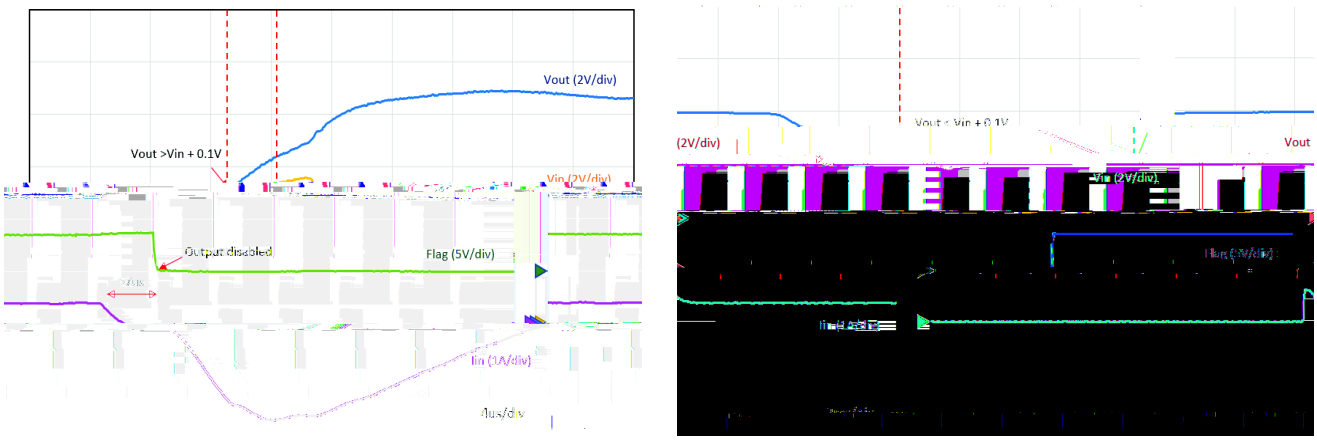


Figure 6. Reverse Current Protection

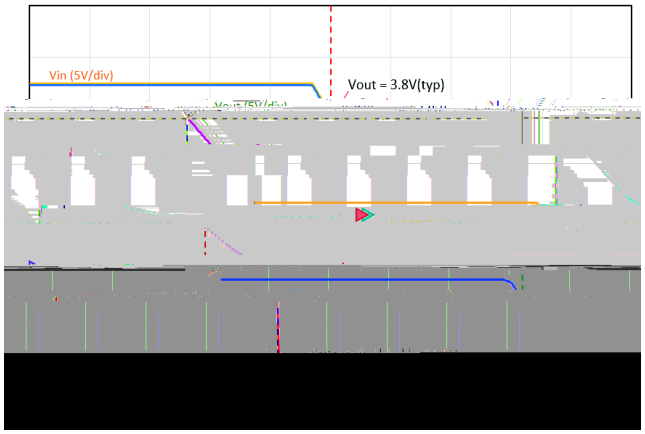


Figure 7. UVLO

ORDERING INFORMATION

Device	Shutdown Version	Marking	Package	Shipping†
NIS6350MT1TXG	Latching	6350	WDFNW10 (Pb−Free)	3000 / Tape and Reel
*NIV6350MT1TXG	Latching	6350		
NIS6350MT2TXG	Auto−Retry	6350H		
*NIV6350MT2TXG	Auto−Retry	6350H		

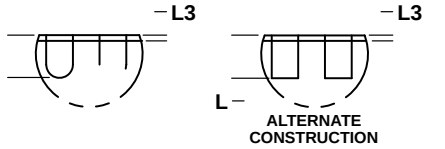
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*NIV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable.

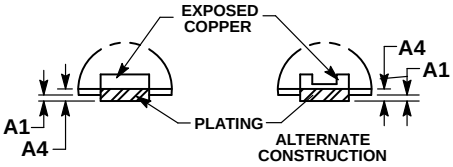
WDFNW10, 3x3, 0.5P
CASE 515AB
ISSUE A

1
SCALE 2:1

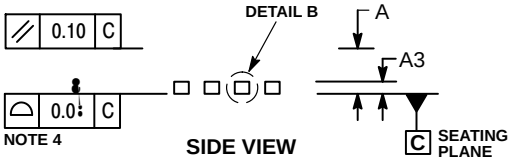
DATE 15 JUN 2018



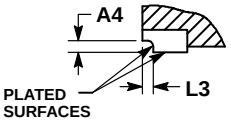
DETAIL A



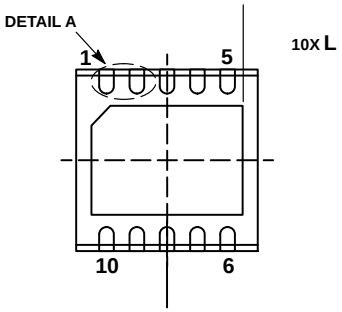
DETAIL B



SIDE VIEW



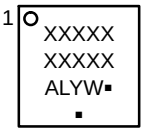
SECTION C−C



NOTES:
1.

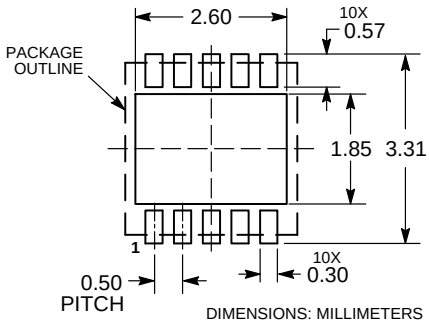
DIM	MILLIMETERS		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	0.03	0.05
A3		0.20 REF	
A4			
b	0.20	0.25	0.30
D	2.90	3.00	3.10
D2	2.40	2.50	2.60
E	2.90	3.00	3.10
E2	1.70	1.80	1.90
e		0.50 BSC	
K			
L	0.30	0.40	0.50
L3			

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package
(Note: Microdot may be in either location)

RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.