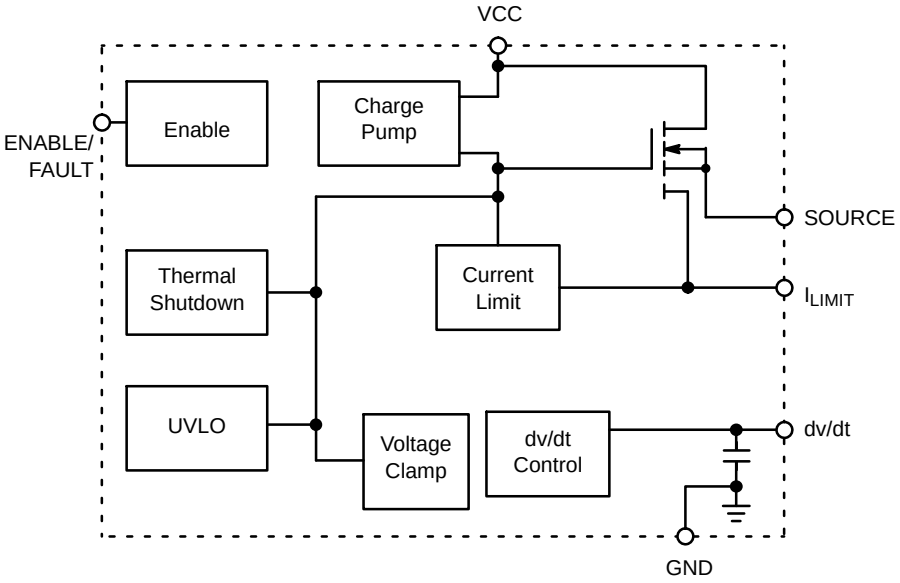
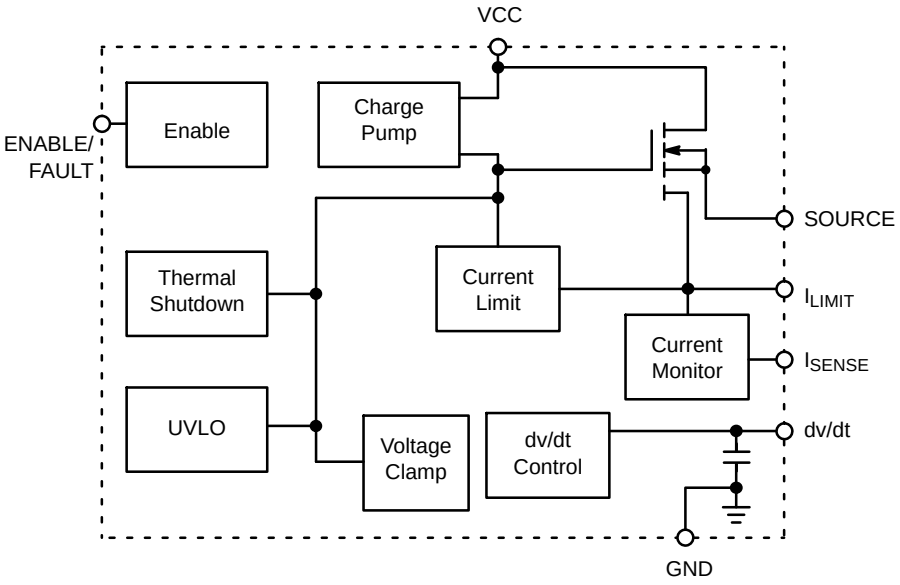
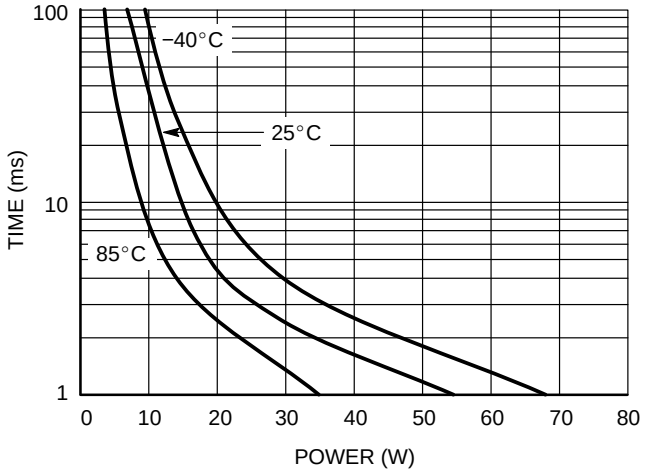
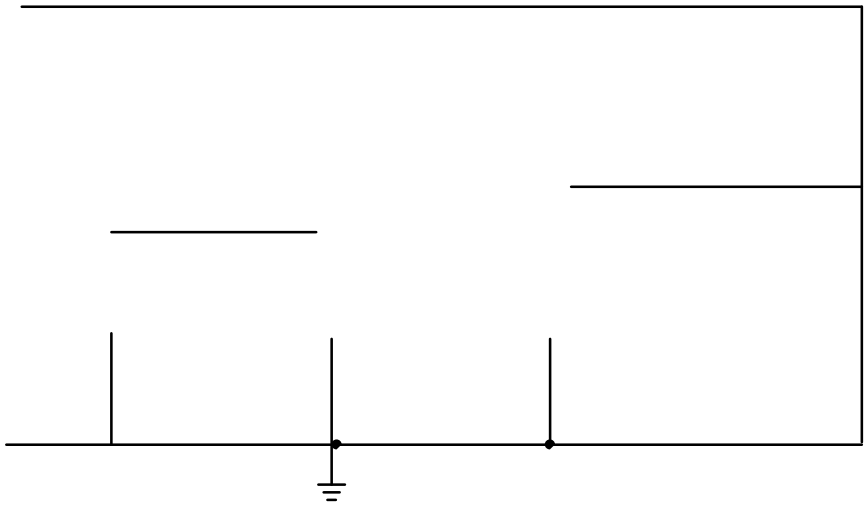

VCC
ENABLE/
FAULT
Enable
Charge
Pump
SOURCE
Thermal
Shutdown
Current
Limit
I_{LIMIT}
UVLO
Voltage
Clamp
dv/dt
Control
dv/dt
GND

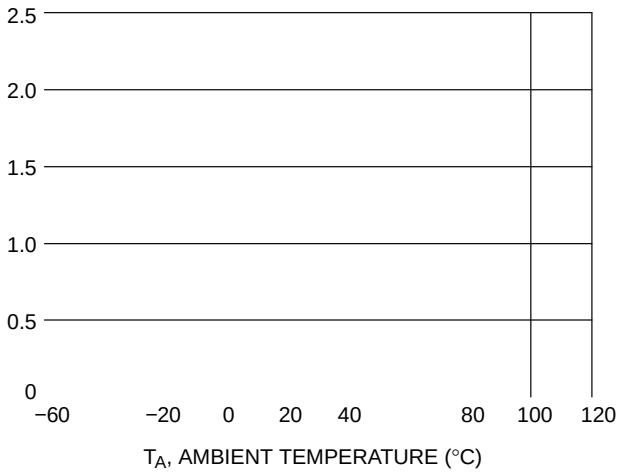

VCC
ENABLE/
FAULT
Enable
Charge
Pump
SOURCE
Thermal
Shutdown
Current
Limit
I_{LIMIT}
Current
Monitor
I_{SENSE}
UVLO
Voltage
Clamp
dv/dt
Control
dv/dt
GND

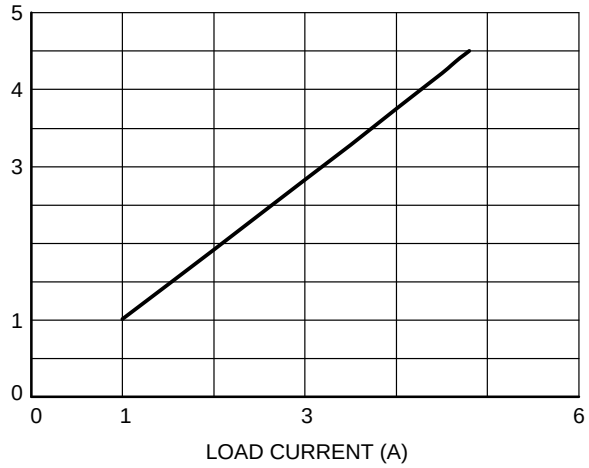
(V_{CC} = 12 V, C_L = 100 μF, dv/dt pin open, R_{LIMIT} = 20 Ω, T_j = 25°C unless otherwise noted.)

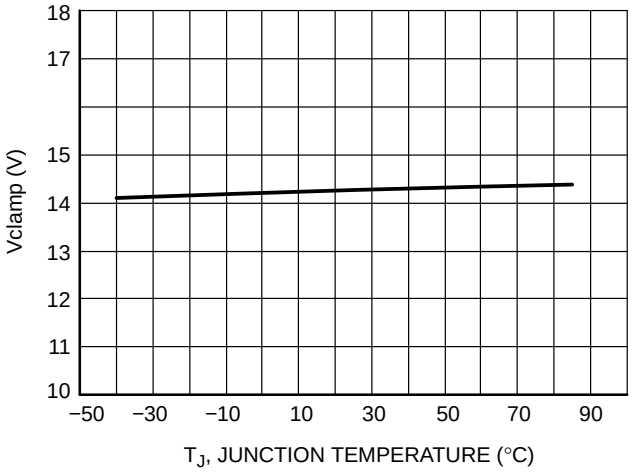
Delay Time (enabling of chip to I_D = 100 mA with 1 A resistive load)	T_{dly}	−	220	−	μs
Kelvin ON Resistance (Note 2) T_J = 140°C (Note 3)	R_{DSon}	30 −	39 60	50 −	mΩ
Off State Output Voltage (V_{CC} = 18 V_{dc}, V_{GS} = 0 V_{dc}, R_L = ∞)	V_{off}	−	−	50	mV
Continuous Current (T_A = 25°C, 100 mm^2 copper) (Note 3) (T_A = 80°C, minimum copper)	I_D I_D	− −	− −	4.6 3.5	A
Shutdown Temperature (Note 3)	T_{SD}	150	175	200	°C
Thermal Hysteresis (Auto−retry part only)	T_{Hyst}	−	45	−	°C
Thermal Shutdown Response Time	T_{SDRes}	10	15	−	μs
Output Clamping Voltage (NIS5420MT2, NIS5420MT7)	V_{Clamp1}	12.5	−	14.5	V
Output Clamping Voltage (NIS5420MT1, NIS5420MT4, NIS5420MT5, NIS5420MT6)	V_{Clamp2}	13.6	−	16	V
Output Clamping Response Time	T_{Clamp_Res}	−	−	10	μs
Undervoltage Lockout (NIS5420MT1, NIS5420MT3, NIS5420MT4, NIS5420MT5, NIS5420MT6)	V_{UVLO1}	7.8	8.5	9.2	V
Undervoltage Lockout (NIS5420MT2, NIS5420MT6, NIS5420MT8)	V_{UVLO2}	6	6.5	7	V
UVLO Hysteresis	V_{Hyst}	−	0.80	−	V
Kelvin Short Circuit Current Limit (R_{Limit} = 20 Ω, Note 4)	I_{Lim-SS}	1.76	2.1	2.64	A
Kelvin Overload Current Limit (R_{Limit} = 20 Ω, Note 4)	I_{Lim-OL}	−	4.2	−	A
Output Voltage Ramp Time (Enable to V_{OUT} = 11.7 V and 10% to 90% − V_{OUT} = 1.2 V to 10.8 V with 12Ω Load)	t_{slew}	−	2.0	−	ms
Maximum Capacitor Voltage	V_{max}	−	−	V_{CC}	V
Logic Level Low (Output Disabled)	V_{in-low}	0.35			

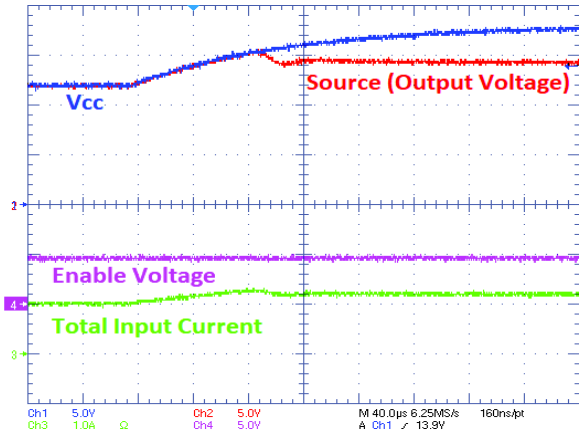

100
10
1
TIME (ms)
−40°C
25°C
85°C
0
10
20
30
40
50
60
70
80
POWER (W)




2.5
2.0
1.5
1.0
0.5
0
−60
−20
0
20
40
80
100
120
T_A, AMBIENT TEMPERATURE (°C)


5
4
3
1
0
0
1
3
6
LOAD CURRENT (A)


Vclamp (V)
18
17
15
14
13
12
11
10
−50
−30
−10
10
30
50
70
90
T_J, JUNCTION TEMPERATURE (°C)


Vcc
Source (Output Voltage)
Enable Voltage
Total Input Current
Ch1 5.0V
Ch2 5.0V
M 40.0µs 6.25MS/s
160ns/pt
Ch3 1.0A Ω
Ch4 5.0V
A Ch1 13.9V

This device is a self protected, resettable, electronic fuse. It contains circuits to monitor the input voltage, output voltage, output current and die temperature.

On application of the input voltage, the device will apply the input voltage to the load based on the restrictions of the controlling circuits. The dv/dt of the output voltage will be controlled by the internal dv/dt circuit. The output voltage will slew from 0 V to the rated output voltage in 1.4 ms, unless additional capacitance is added to the dv/dt pin.

The device will remain on as long as the temperature does not exceed the 175°C limit that is programmed into the chip. The current limit circuit does not shut down the part but will reduce the conductivity of the FET to maintain a constant current at the internally set current limit level. The input overvoltage clamp also does not shutdown the part, but will limit the output voltage to 13.5/15 V in the event that the input exceeds that level.

An internal charge pump provides bias for the gate voltage of the internal n channel power FET and also for the current limit circuit. The remainder of the control circuitry operates between the input voltage (V_{CC}) and ground.

The current limit circuit uses a SENSEFET along with a reference and amplifier to control the peak current in the device. The SENSEFET allows for a small fraction of the load current to be measured, which has the advantage of reducing the losses in the sense resistor as well as increasing the value and decreasing the power rating of the sense resistor. Sense resistors are typically in the tens of ohms range with power ratings of several milliwatts making them very inexpensive chip resistors.

The current limit circuit has two limiting values, one for short circuit events which are defined as the mode of operation in which the gate is high and the FET is fully enhanced. The overload mode of operation occurs when the device is actively limiting the current and the gate is at an intermediate level. For a more detailed description of this circuit please refer to application note AND9441.

There are two methods of biasing the current limit circuit for this device. They are shown in the two application figures. Direct current sensing connects the sense resistor between the current limit pin and the load. This method includes the bond wire resistance in the current limit circuit. This resistance has an impact on the current limit levels for a given resistor and may vary slightly depending on the impedance between the sense resistor and the source pins. The on resistance of the device will be slightly lower in this configuration since all five source pins are connected in parallel and therefore, the effective bond wire resistance is one fifth of the resistance for any given pin.

The other method is Kelvin sensing. This method uses one of the source pins as the connection for the current sense resistor. This connection senses the voltage on the die and therefore any bond wire resistance and external impedance on the board have no effect on the current limit levels. In this configuration the on resistance is slightly increased relative to the direct sense method since only four of the source pins are used for power.

The overvoltage clamp consists of an amplifier and reference. It monitors the output voltage and if the input voltage exceeds the overvoltage value, the gate drive of the main FET is reduced to limit the output. This is intended to allow operation through transients while protecting the load. If an overvoltage condition exists for many seconds, the device may overheat due to the voltage drop across the FET combined with the load current. In this event, the thermal protection circuit would shut down the device.

The undervoltage lockout circuit uses a comparator with hysteresis to monitor the input voltage. If the input voltage drops below the specified level, the output switch will be switched to a high impedance state.

The dv/dt circuit brings the output voltage up under a linear, controlled rate regardless of the load impedance characteristics. An internal ramp generator creates a linear ramp, and a control circuit forces the output voltage to follow that ramp, scaled by a factor.

The default ramp time is approximately 2 ms. This can be modified by adding an external capacitor at the dv/dt pin. Since the current level is very low, it is important to use a ceramic cap or other low leakage capacitor. Aluminum electrolytic capacitors are not recommended for this circuit.

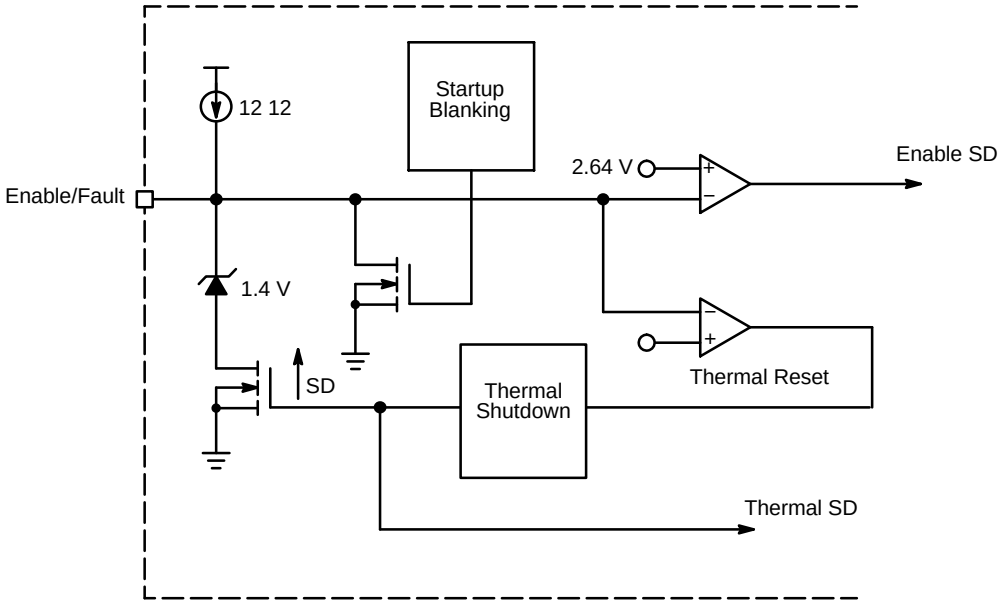
The ramp time from 0 to the nominal output voltage can be determined by the following equation, where *t* is in seconds:

$$t_{1.2-10.8t}$$

turned on. If a thermal fault occurs, this pin will be pulled low to an intermediate level by an internal circuit.

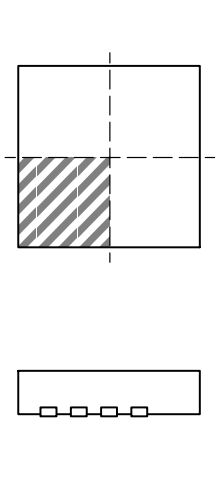
To use as a simple enable pin, an open drain or open collector device should be connected to this pin. Due to its tri state operation, it should not be connected to any type of logic with an internal pullup device.

If the chip shuts down due to the die temperature reaching its thermal limit, this pin will be pulled down to an intermediate level. This signal can be monitored by an external circuit to communicate that a thermal shutdown has occurred. If this pin is tied to another device in this family,


12 12
Startup
Blanking
2.64 V
Enable SD
Enable/Fault
1.4 V
SD
Thermal
Shutdown
Thermal Reset
Thermal SD

WDFN10, 3x3, 0.5P
CASE 522AA−01
ISSUE A

DATE 02 JUL 2007



NO E :
1. DIMEN IONING AND OLE ANCING PE A ME 14.5M, 1994.
2. CON OLLING DIMEN ION: MILLIME E .
3. DIMEN ION APPLIE O PLA ED E MINAL AND MEA ED BE EEN 0.15 AND 0.30 F OM E MINAL.
4. COPLANA I APPLIE O HE E PO ED PAD A EL A HE E MINAL .