+1

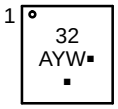
S 1 S

The NIS5132 is a cost effective, resettable fuse which can greatly enhance the reliability of a hard drive or other circuit from both catastrophic and shutdown failures.

It is designed to buffer the load device from excessive input voltage which can damage sensitive circuits. It also includes an overvoltage clamp circuit that limits the output voltage during transients but does not shut the unit down, thereby allowing the load circuit to continue operation. Two thermal options are available, latching and auto−retry.

- Integrated Power Device
- Power Device Thermally Protected
- No External Current Shunt Required
- 9 V to 18 V Input Range
- 44 mΩ Typical
- Internal Charge Pump
- Internal Undervoltage Lockout Circuit
- Internal Overvoltage Clamp (MN1 and MN2 versions)
- ESD Ratings: Human Body Model (HBM); 2000 V
  Machine Model (MM); 200 V
- These Devices are Pb−Free and are RoHS Compliant

- Hard Drives
- Mother Board Power Management



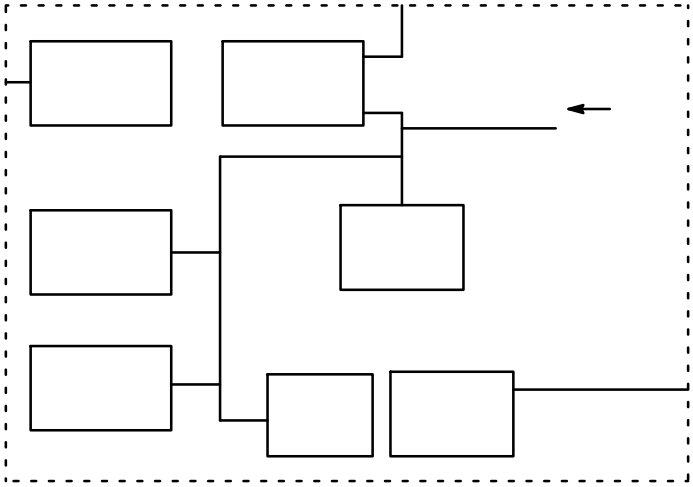
Pin	Function
1	GND
2	dv/dt
3	Enable/Fault
4	ILIMIT
5	NC
6−10	SOURCE
11 (flag)	VCC

32 = Latching Version with V_{Clamp}
32B = Latching Version without V_{Clamp}
32H = Auto−Retry Version with V_{Clamp}
A = Assembly Location
Y = Year
W = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

See detailed ordering and shipping information in the ordering information section on page 10 of this data sheet.

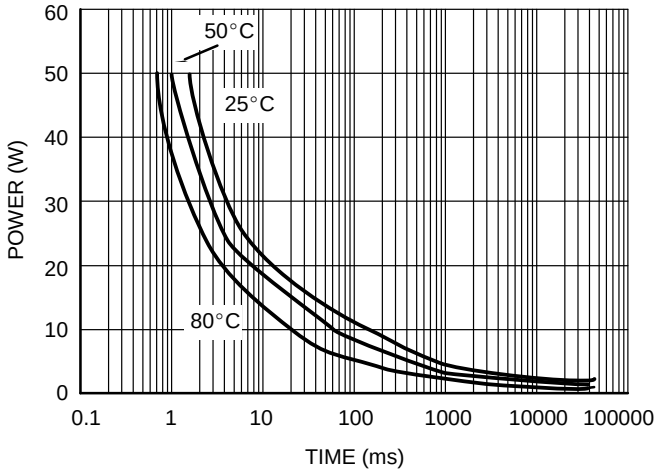
Publication Order Number:

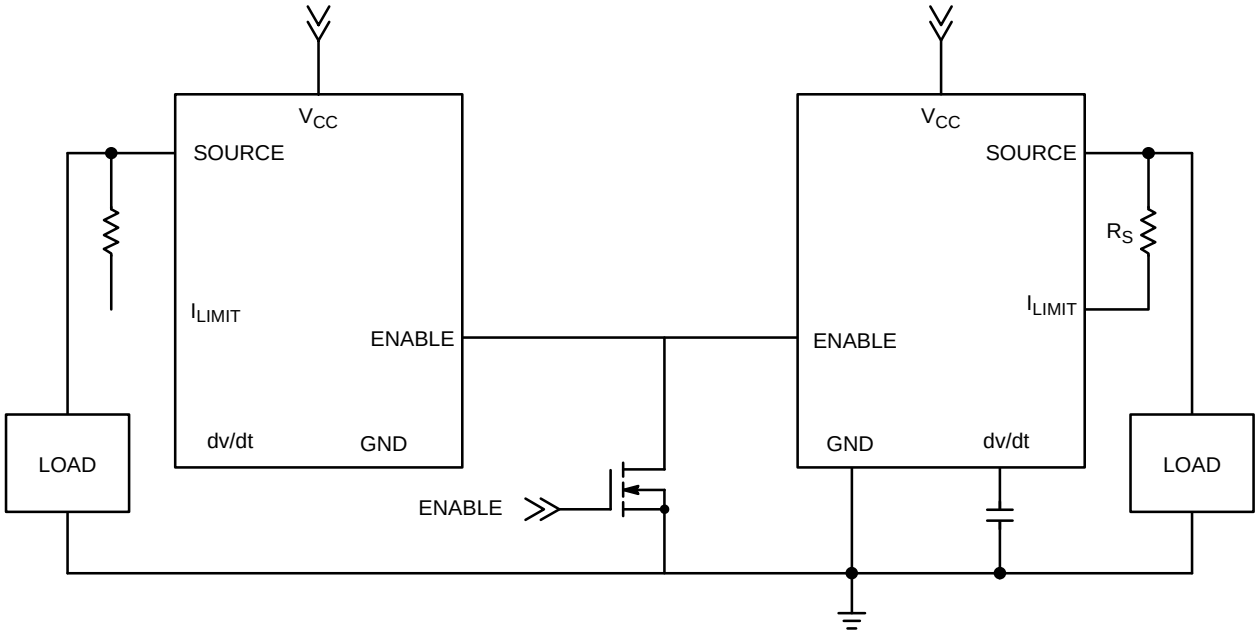


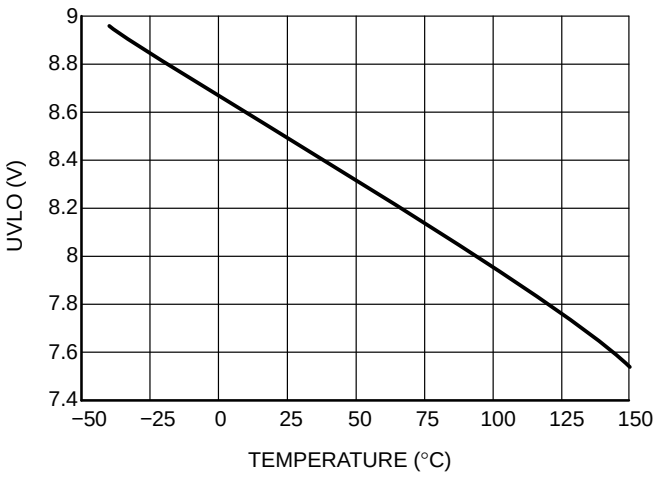
(Unless otherwise noted: V_{CC} = 12 V, C_L = 100 μF, dv/dt pin open, R_{LIMIT} = 10 Ω, T_j = 25°C unless otherwise noted.)

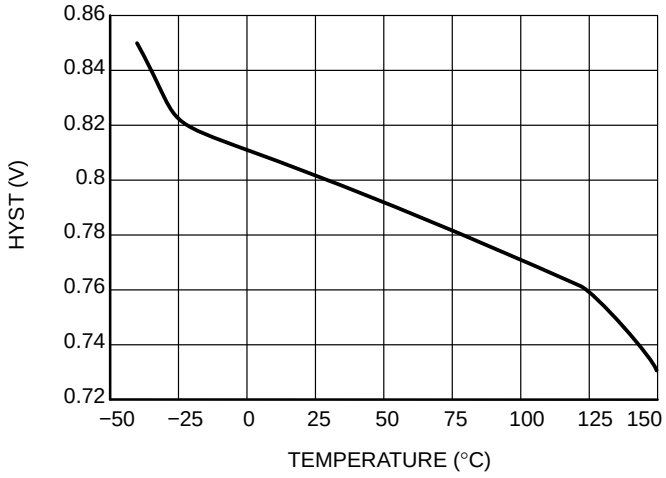
Delay Time (enabling of chip to I_D = 100 mA with 1 A resistive load)	T_{dly}		220		μs
Kelvin ON Resistance (Note 4) T_J = 140°C (Note 5)	R_{DSon}	35	44 62	55	mΩ
Off State Output Voltage (V_{CC} = 18 V_{dc}, V_{GS} = 0 V_{dc}, R_L = □)	V_{off}		190	300	mV
Output Capacitance (V_{DS} = 12 V_{dc}, V_{GS} = 0 V_{dc}, f = 1 MHz)			250		pF
Continuous Current (T_A = 25°C, 0.5 in^2 pad) (Note 5) (T_A = 80°C, minimum copper)	I_D I_D		3.6 1.7		A
Shutdown Temperature (Note 5)	T_{SD}	150	175	200	°C
Thermal Hysteresis (Decrease in die temperature for turn on, does not apply to latching parts)	T_{Hyst}		45		°C
Output Clamping Voltage (Overvoltage Protection) (V_{CC} = 18 V) (Note 6)	V_{Clamp}	14	15	16.2	V
Undervoltage Lockout (Turn on, voltage going high)	V_{UVLO}	7.7	8.5	9.3	V
UVLO Hysteresis	V_{Hyst}	−	0.80	−	V
Kelvin Short Circuit Current Limit (R_{Limit} = 15.4 Ω, Note 7)	I_{Lim-SS}	2.75	3.44	4.25	A
Kelvin Overload Current Limit (R_{Limit} = 15.4 Ω, Note 7)	I_{Lim-OL}		4.6		A
Output Voltage Ramp Time (Enable to V_{OUT} = 11.7 V)	t_{slew}	0.5	0.9	1.8	ms
Maximum Capacitor Voltage	V_{max}			V_{CC}	V
Logic Level Low (Output Disabled)	V_{in-low}	0.35	0.58	0.81	V
Logic Level Mid (Thermal Fault, Output Disabled)	V_{in-mid}	0.82	1.4	1.95	V
Logic Level High (Output Enabled)	$V_{in-high}$	1.96	2.64	3.30	V
High State Maximum Voltage	V_{in-max}	3.40	4.30	5.2	V
Logic Low Sink Current (V_{enable} = 0 V)	I_{in-low}		−17	−25	μA
Logic High Leakage Current for External Switch (V_{enable} = 3.3 V)	$I_{in-leak}$			1.0	μA
Maximum Fanout for Fault Signal (Total number of chips that can be connected to this pin for simultaneous shutdown)	Fan			3.0	Units
Bias Current (Operational)	I_{Bias}		1. 8	2.5	mA
Bias Current (Shutdown)	I_{Bias}		1.0		mA
Minimum Operating Voltage (Notes 5 and 8)	V_{min}			7.6	V

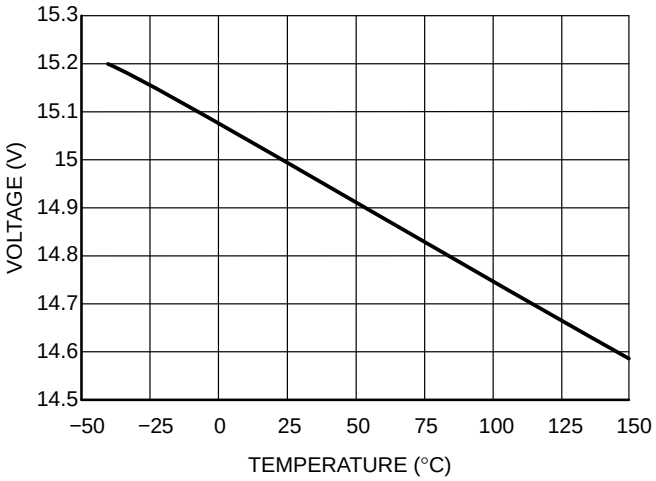
Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product

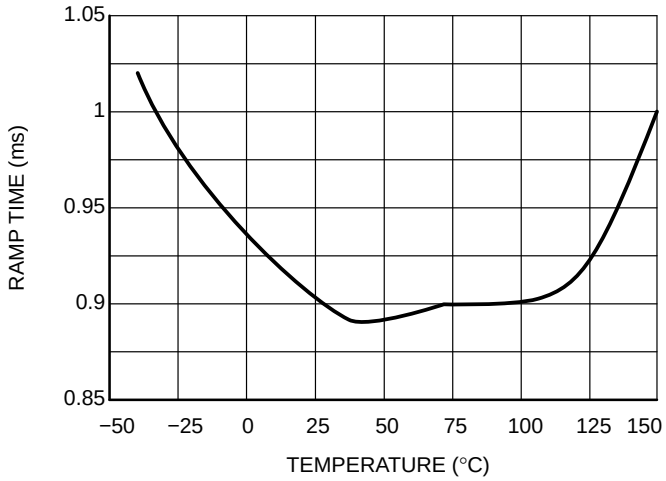

60
50
40
30
20
10
0
POWER (W)
50°C
25°C
80°C
0.1
1
10
100
1000
10000
100000
TIME (ms)

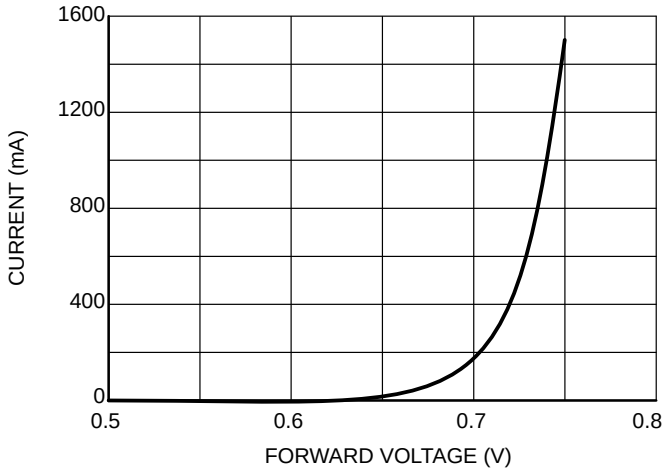

VCC
SOURCE
ILIMIT
ENABLE
dv/dt
GND
LOAD
ENABLE
VCC
SOURCE
RS
ILIMIT
ENABLE
GND
dv/dt
LOAD

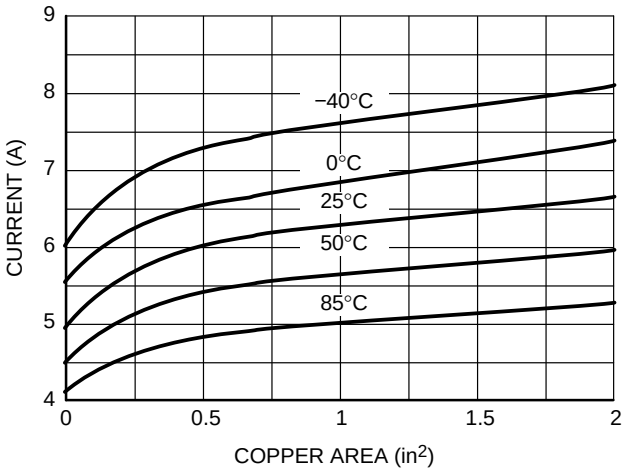

UVLO (V)
9
8.8
8.6
8.4
8.2
8
7.8
7.6
7.4
−50 −25 0 25 50 75 100 125 150
TEMPERATURE (°C)

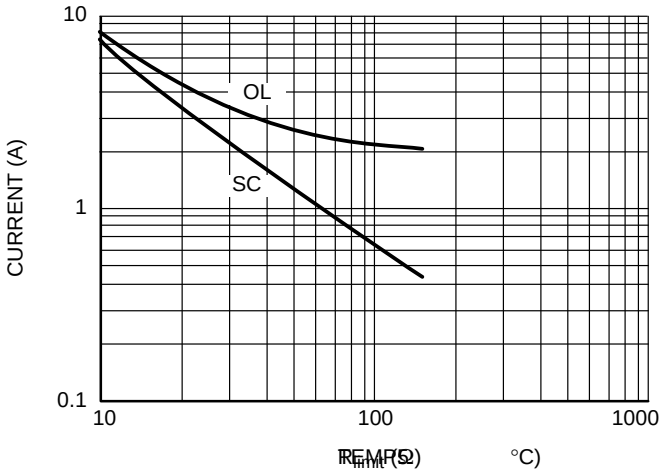

HYST (V)
0.86
0.84
0.82
0.8
0.78
0.76
0.74
0.72
−50 −25 0 25 50 75 100 125 150
TEMPERATURE (°C)

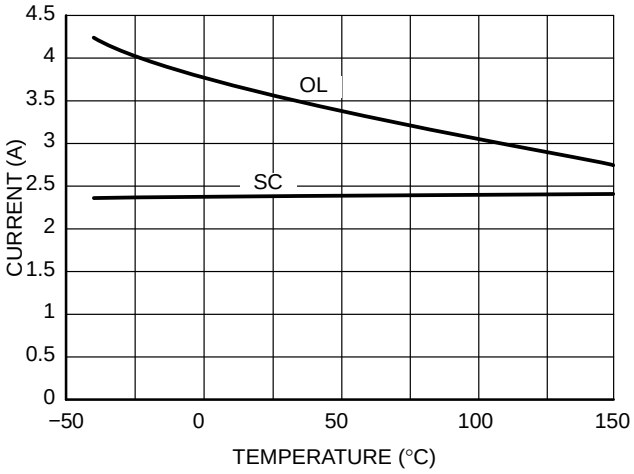

VOLTAGE (V)
15.3
15.2
15.1
15
14.9
14.8
14.7
14.6
14.5
−50 −25 0 25 50 75 100 125 150
TEMPERATURE (°C)

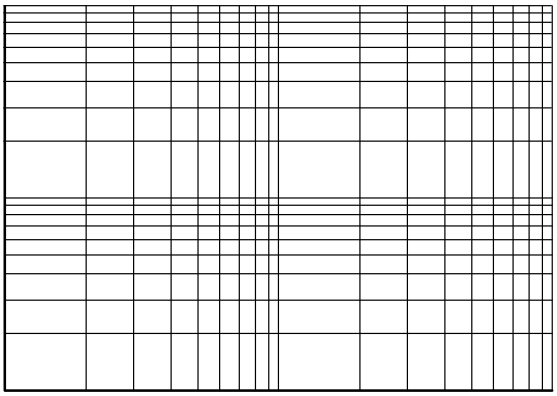

RAMP TIME (ms)
1.05
1
0.95
0.9
0.85
−50 −25 0 25 50 75 100 125 150
TEMPERATURE (°C)


CURRENT (mA)
1600
1200
800
400
0
0.5 0.6 0.7 0.8
FORWARD VOLTAGE (V)

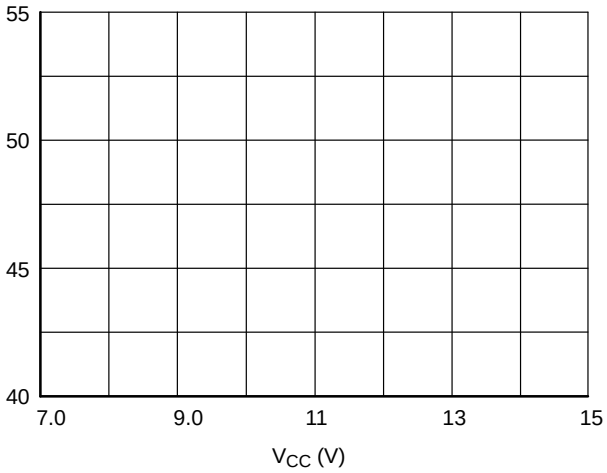

9
8
7
6
5
4
CURRENT (A)
−40°C
0°C
25°C
50°C
85°C
0
0.5
1
1.5
2
COPPER AREA (in2)


10
1
0.1
CURRENT (A)
OL
SC
10
100
1000
°C)


4.5
4
3.5
3
2.5
2
1.5
1
0.5
0
CURRENT (A)
OL
SC
−50
0
50
100
150
TEMPERATURE (°C)



Ω


55
50
45
40
7.0
9.0
11
13
15
V_{CC} (V)

The undervoltage lockout circuit uses a comparator with hysteresis to monitor the input voltage. If the input voltage drops below the specified level, the output switch will be switched to a high impedance state.

The dv/dt circuit brings the output voltage up under a linear, controlled rate regardless of the load impedance characteristics. An internal ramp generator creates a linear ramp, and a control circuit forces the output voltage to follow that ramp, scaled by a factor.

The default ramp time is approximately 2 ms. This can be modified by adding an external capacitor at the dv/dt pin. This pin includes an internal current source of approximately 85 nA. Since the current level is very low, it is important to use a ceramic cap or other low leakage capacitor. Aluminum electrolytic capacitors are not recommended for this circuit.

The ramp time from 0 to the nominal output voltage can be determined by the following equation, where *t* is in seconds:

$$t_{0\square 12} \square 24e6 \square \square 50\ pF \square C_{ext} \square$$