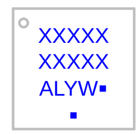
9 24 E F

4461

ON Semiconductor

wfA 0 0 m1.304 .737 1.587 1.474 185 flt



Features

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Typical Applications

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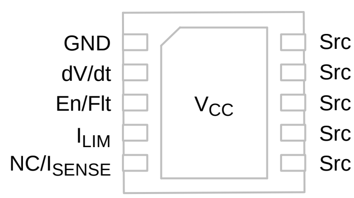
PIN CONNECTIONS



WDFN10

(Top View)

ORDERING INFORMATION

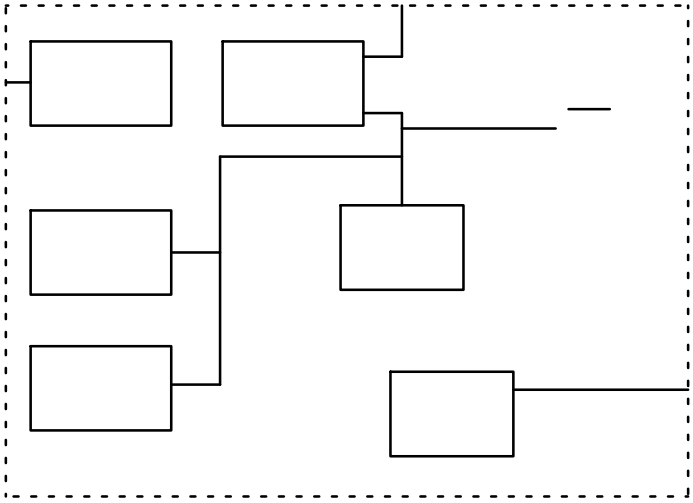


Figure 1. Block Diagram
(NIS4461MT2TXG, NIS4461MT4TXG)

Table 1. FUNCTIONAL PIN DESCRIPTION

Pin	Function	Description
1	Ground	Negative input voltage to the device. This is used as the internal reference for the IC.
2	dv/dt	The internal dv/dt circuit controls the slew rate of the output voltage at turn on. It has an internal capacitor that allows it to ramp up over a period of 2 ms. An external capacitor can be added to this pin to increase the ramp time. If an additional time delay is not required, this pin should be left open.
3	Enable/Fault	The enable/fault pin is a tri−state, bidirectional interface. It can be pulled to ground with external open−drain or open collector device to shutdown the eFuse. It can also be used as a status indicator; if the voltage level is intermediate around 1.4 V − the eFuse is in the thermal shutdown, if the voltage level is high around 3 V − the eFuse is operating normally. Do not actively drive this pin to any voltage. Do not connect a capacitor to this pin.
4	I_{Limit}	A resistor between this pin and the source pin sets the overload and short circuit current limit levels.
5	NC	For NIS4461MT2TXG and NIS4461MT4TXG
	I_{SENSE}	For NIS4461MT1TXG and NIS4461MT3TXG load current monitor allows the system to monitor the load current in real time. Connect R_{SENSE} to GND.
6−10	Source	This pin is the source of the internal power FET and the output terminal of the fuse. Connect an electrolytic capacitor or Schottky diode for 27 V or higher.
11 (belly pad)	V_{CC}	Positive input voltage to the device.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Input Voltage, operating, steady−state (V_{CC} to GND, Note 1) Transient (100 ms)	V_{IN}	−0.6 to 30 −0.6 to 30	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Negative voltage will not damage device provided that the power dissipation is limited to the rated allowable power for the package.

Table 2. THERMAL RATINGS

Rating	Symbol	Value	Unit
Thermal Resistance, Junction−to−Air (4 layer High−K JEDEC JESD51−7 PCB, 100 mm^2, 2 oz. Cu)	θ_{JA}	90	°C/W
Thermal Characterization Parameter, Junction−to−Lead (4 layer High−K JEDEC JESD51−7 PCB, 100 mm^2, 2 oz. Cu)	θ_{J-L}	27.5	°C/W
Thermal Characterization Parameter, Junction−to−Board (4 layer High−K JEDEC JESD51−7 PCB, 100 mm^2, 2 oz. Cu)	θ_{J-B}	27.5	°C/W
Thermal Characterization Parameter, Junction−to−Case Top (4 layer High−K JEDEC JESD51−7 PCB, 100 mm^2, 2 oz. Cu)	θ_{J-T}	7.6	°C/W
Total Power Dissipation @ T_A = 25°C (4 layer High−K JEDEC JESD51−7 PCB, 100 mm^2, 2 oz. Cu) Derate above 25°C	P_{max}		

ELECTRICAL CHARACTERISTICS (V_{CC} = 24 V, C_L = 100 □F, dv/dt pin open, R_{LIMIT} = 20 □, T_j = 25°C unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
POWER FET					
Delay Time (enabling of chip to I_D = 100 mA with 1 A resistive load)	T_{dly}	−	220	−	□s
Kelvin ON Resistance (Note 2) T_J = 140°C (Note 3)	R_{DSon}	30 −	39 60	50 −	m□
Continuous Current (T_A = 25°C, 0.5 in^2 copper) (Note 3) (T_A = 80°C, minimum copper)	I_D I_D	− −	4.2 2.5	− −	A
THERMAL LATCH					
Shutdown Temperature (Note 3)	T_{SD}	150	175	200	°C
Thermal Hysteresis (Auto−retry part only)	T_{Hyst}	−	45	−	°C
Thermal Shutdown Response Time	T_{SDRes}	10	15	20	□s
UNDERVOLTAGE PROTECTION					
Undervoltage Lockout	V_{UVLO}	6	6.5	7	V
UVLO Hysteresis	V_{Hyst}	−	0.80	−	V
CURRENT LIMIT					
Kelvin Short Circuit Current Limit (R_{Limit} = 20 □, Note 4)	I_{Lim-SS}	1.76	2.1	2.64	A
Kelvin Overload Current Limit (R_{Limit} = 20 □, Note 4)	I_{Lim-OL}	−	4.6	−	A
dv/dt CIRCUIT					
Output Voltage Ramp Time (Enable to V_{OUT} = 23.7 V)	t_{slew}	−	2.0	−	ms
Output Voltage Ramp Time (10% to 90% − V_{OUT} = 2.4 V to 21.6 V with 24□ Load)	t_{slew}	−	1.2	−	ms
Maximum Capacitor Voltage	V_{max}	−	−	V_{CC}	V
ENABLE/FAULT					
Logic Level Low (Output Disabled)	V_{in-low}	0.35	0.58	0.81	V
Logic Level Mid (Thermal Fault, Output Disabled)	V_{in-mid}	0.82	1.4	1.95	V
Logic Level High (Output Enabled)	$V_{in-high}$	1.96	2.6	3.0	V
High State Maximum Voltage	V_{in-max}	2.51	4.6	5	V
Logic Low Sink Current (V_{enable} = 0 V)	I_{in-low}	−	−15	−25	□A
Logic High Leakage Current for External Switch (V_{enable} = 3.3 V)	$I_{in-leak}$	−	−	1.0	□A
Maximum Fanout for Fault Signal (Total number of chips that can be connected to this pin for simultaneous shutdown)	Fan	−	−	3.0	Units
TOTAL DEVICE					
Bias Current (Operational)	I_{Bias}	−	−	450	□A
Bias Current (Shutdown)					

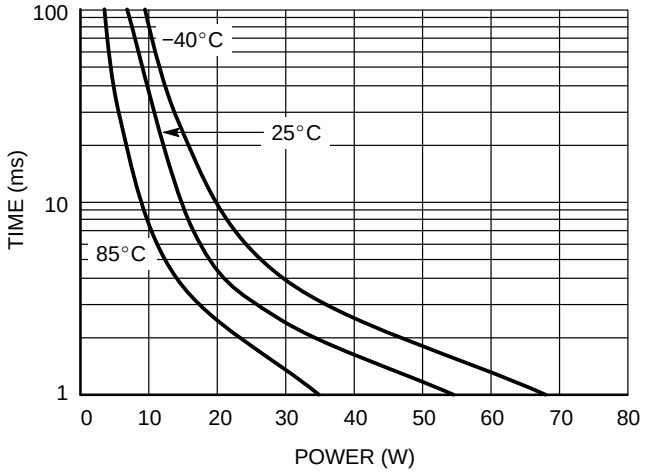


Figure 3. Thermal Trip Time vs. Power Dissipation

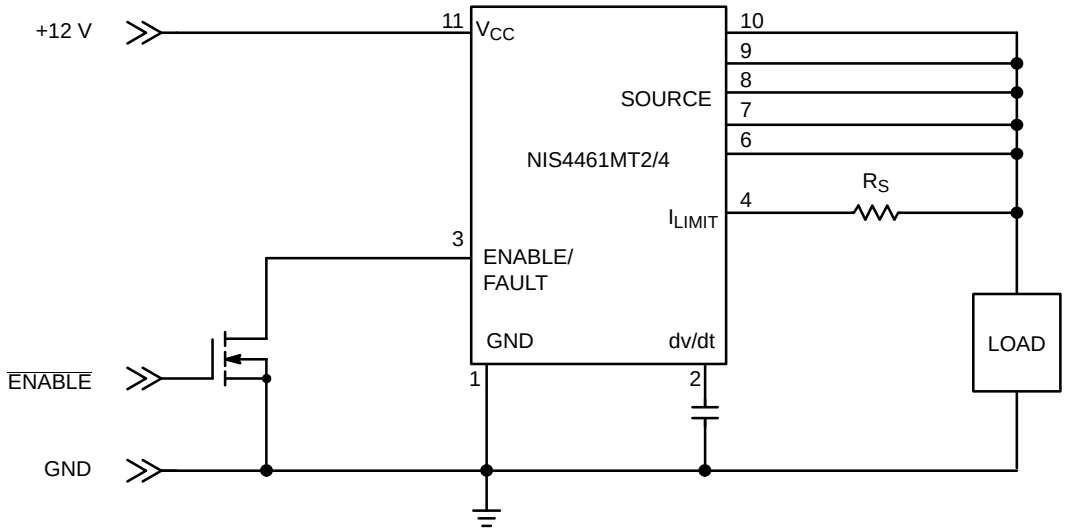


Figure 4. Application Circuit with Direct Current Sensing

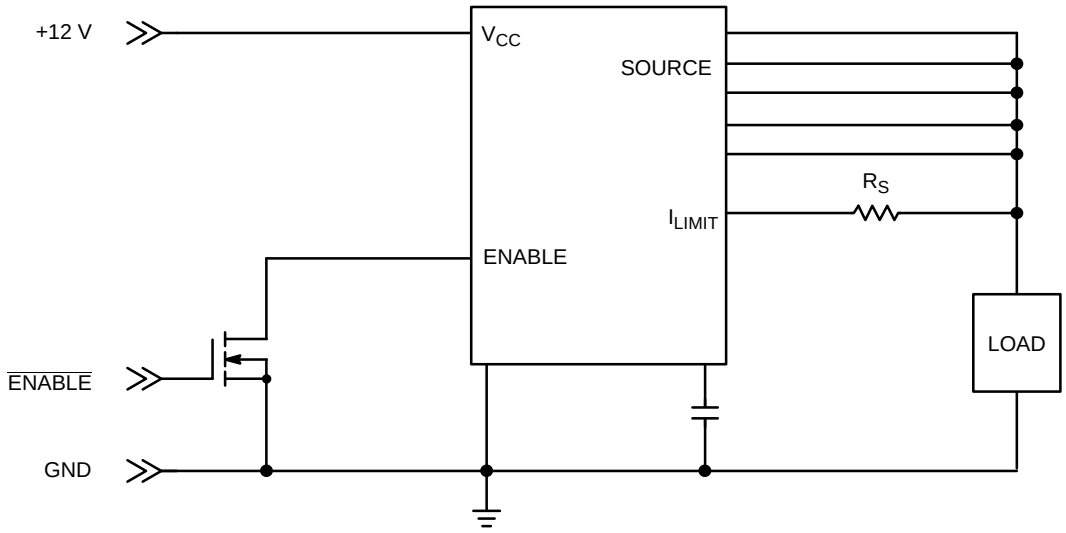


Figure 5. Application Circuit with Direct Current Sensing

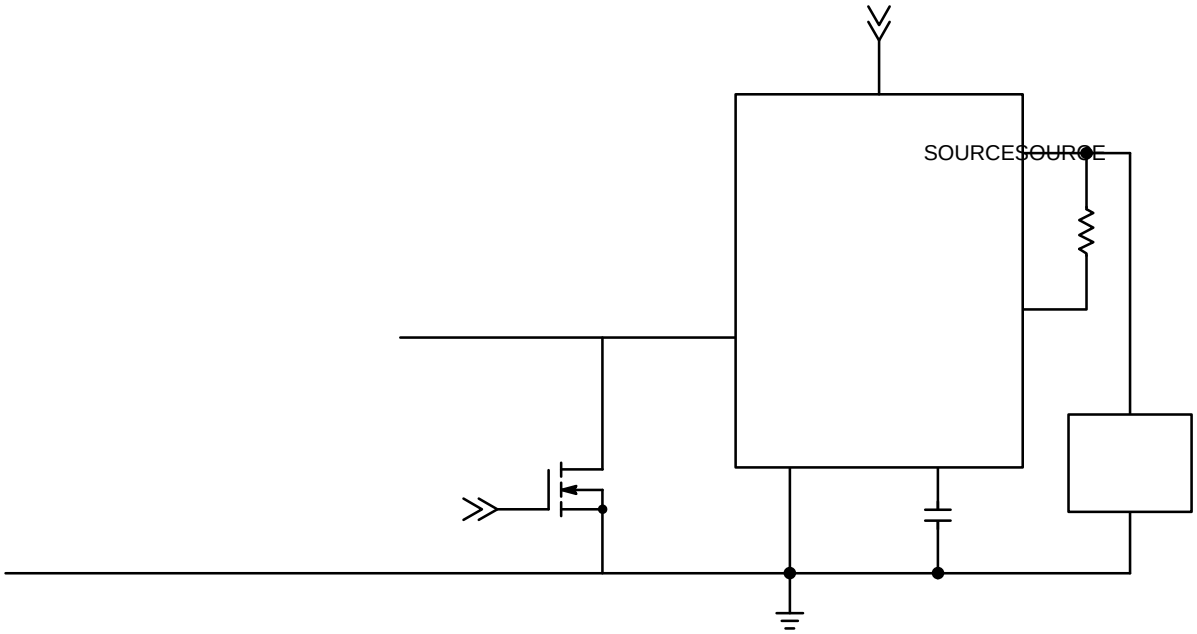


Figure 6. Common Thermal Shutdown

TYPICAL CHARACTERISTICS

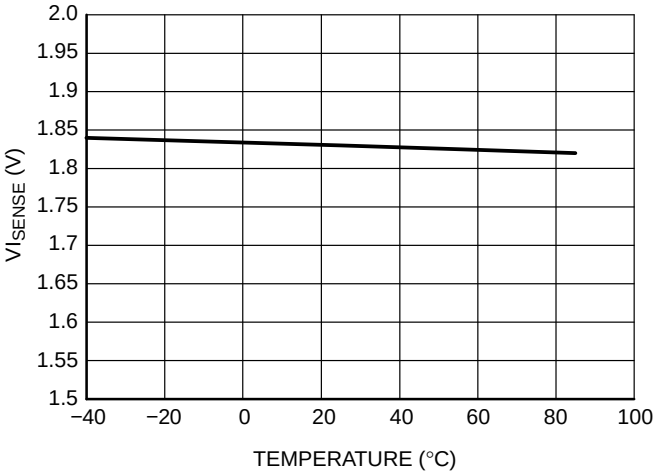


Figure 7. VI_{SENSE} vs. Temperature

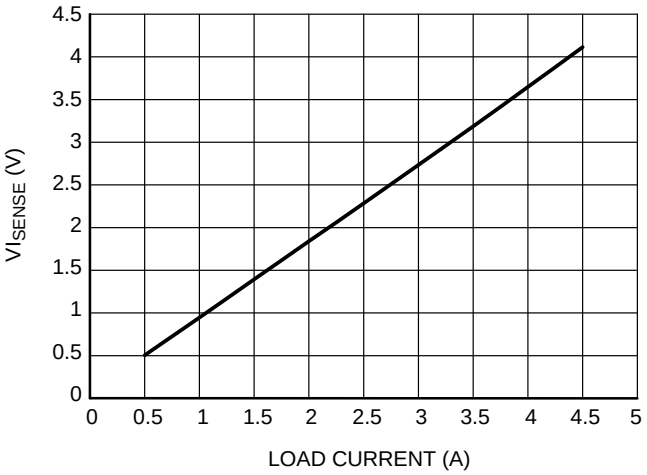


Figure 8. VI_{SENSE} vs. Load Current

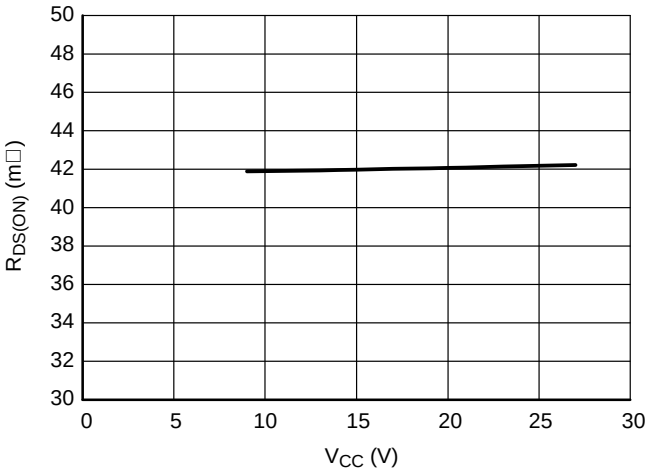


Figure 9. $R_{DS(ON)}$ vs. V_{CC}

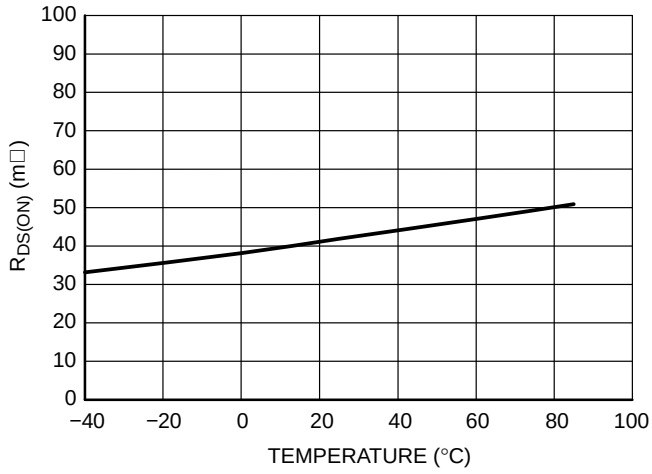


Figure 10. $R_{DS(ON)}$ vs. Temperature

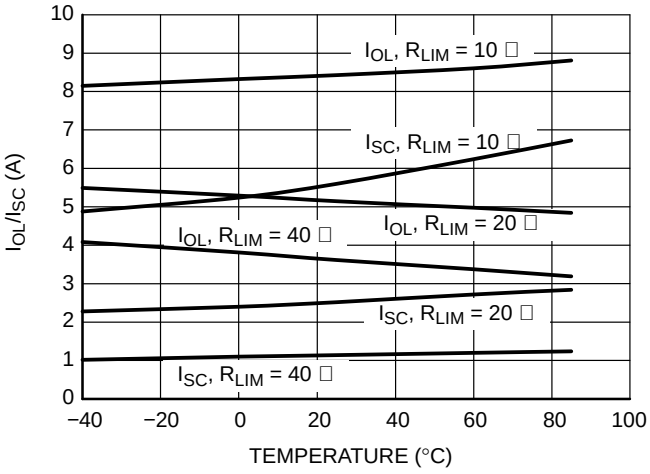


Figure 11. I_{OL} and I_{SC} vs. Temperature

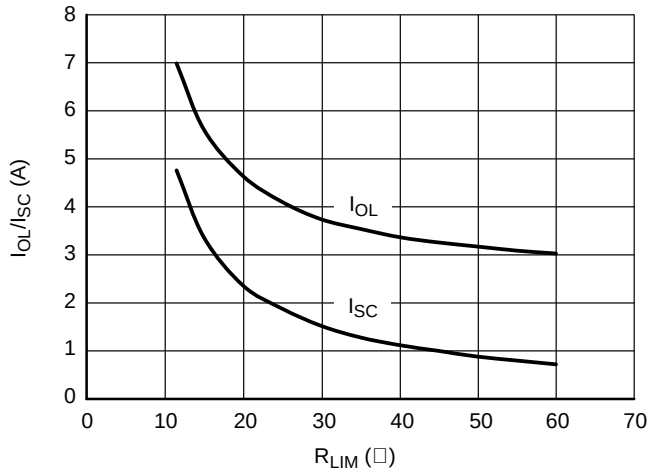


Figure 12. I_{OL} and I_{SC} vs. R_{LIM}

TYPICAL CHARACTERISTICS

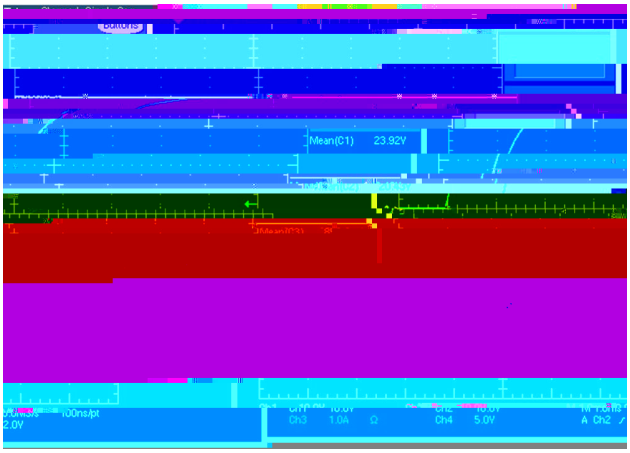


Figure 13. Slew Rate Control Screenshot

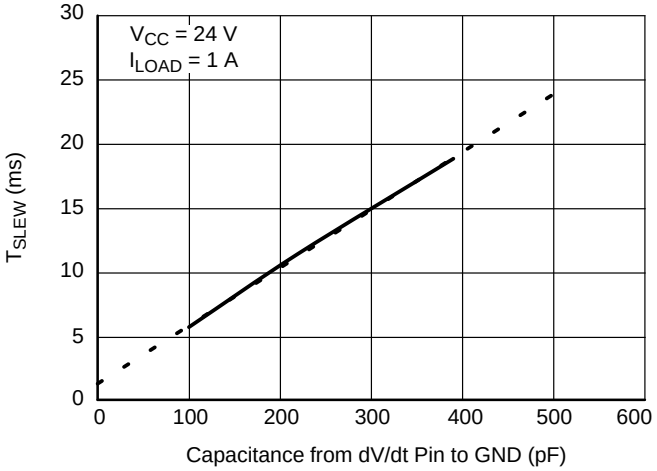


Figure 14. T_{SLEW} vs. dV/dt Capacitance

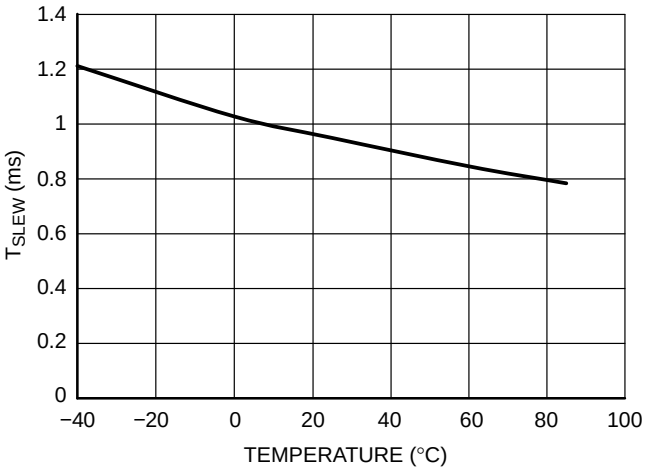


Figure 15. T_{SLEW} vs. Temperature

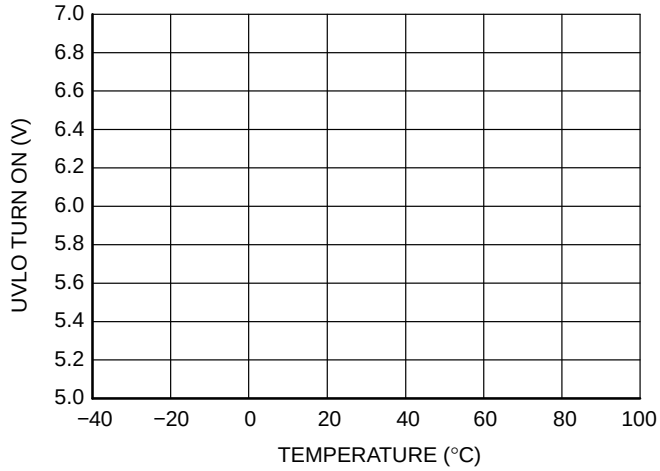


Figure 16. UVLO TURN ON vs. Temperature

APPLICATION INFORMATION

Basic Operation

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Current Limit

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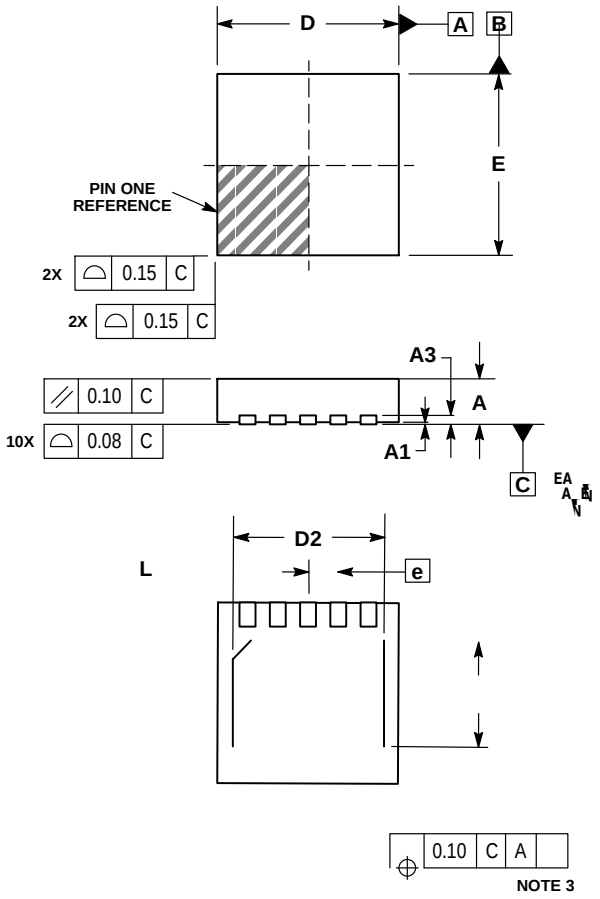
Thermal Protection

NIS4461 Series

PACKAGE DIMENSIONS

WDFN10, 3x3, 0.5P
CASE 522AA
ISSUE A



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30mm FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	E E		
D			A
A	0.70	0.75	0.80
A1	0.00	0.03	0.05
A3		0.20 REF	
	0.18	0.24	0.30
D		3.00 BSC	
D2	2.45	2.50	2.55
E		3.00 BSC	
E2	1.75	1.80	1.85
		0.50 BSC	
		0.19 TYP	