4461

The NIS4461 eFuse is a cost effective, resettable fuse which can greatly enhance the reliability of a hard drive or other circuit from both catastrophic and shutdown failures.

It is designed to protect the downstream circuitry against an overcurrent event by limiting the current while protecting against high inrush current, as well as monitoring the load current in real time.

Features

- Integrated Power Device
- Power Device Thermally Protected
- No External Current Shunt Required
- 9 V to 24 V Input Range
- 39 m Typical
- Internal Charge Pump
- Internal Undervoltage Lockout Circuit
- ESD Ratings:

Human Body Model (HBM); 2000 V Charged Device Model (CDM); 2000 V Latch-Up; Class 1

 These Devices are Pb–Free, Halogen Free/BFR Free and are RoHS Compliant

Typical Applications

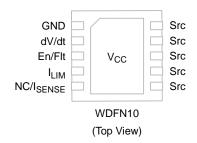
- Hard Drives
- Mother Board Power Management
- Fan Drives
- Industrial
- Handheld Devices
- Portable Instruments



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PIN CONNECTIONS



ORDERING INFORMATION

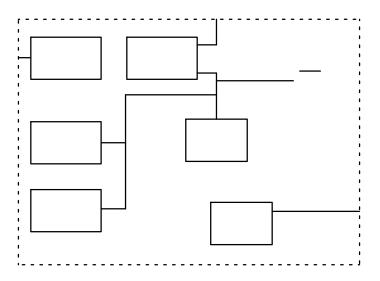


Figure 1. Block Diagram (NIS4461MT2TXG, NIS4461MT4TXG)

Table 1. FUNCTIONAL PIN DESCRIPTION

| Pin | Function | Description |
|----------------|--------------------|--|
| 1 | Ground | Negative input voltage to the device. This is used as the internal reference for the IC. |
| 2 | dv/dt | The internal dv/dt circuit controls the slew rate of the output voltage at turn on. It has an internal capacitor that allows it to ramp up over a period of 2 ms. An external capacitor can be added to this pin to increase the ramp time. If an additional time delay is not required, this pin should be left open. |
| 3 | Enable/Fault | The enable/fault pin is a tri–state, bidirectional interface. It can be pulled to ground with external open–drain or open collector device to shutdown the eFuse. It can also be used as a status indicator; if the voltage level is intermediate around 1.4 V – the eFuse is in the thermal shutdown, if the voltage level is high around 3 V – the eFuse is operating normally. Do not actively drive this pin to any voltage. Do not connect a capacitor to this pin. |
| 4 | I _{Limit} | A resistor between this pin and the source pin sets the overload and short circuit current limit levels. |
| 5 | NC | For NIS4461MT2TXG and NIS4461MT4TXG |
| | I _{SENSE} | For NIS4461MT1TXG and NIS4461MT3TXG load current monitor allows the system to monitor the load current in real time. Connect R _{SENSE} to GND. |
| 6–10 | Source | This pin is the source of the internal power FET and the output terminal of the fuse. Connect an electrolytic capacitor or Schottky diode for 27 V or higher. |
| 11 (belly pad) | V _{CC} | Positive input voltage to the device. |

MAXIMUM RATINGS

| I | Rating | Symbol | Value | Unit |
|---|--|----------|--------------------------|------|
| | Input Voltage, operating, steady-state (V _{CC} to GND, Note 1) Transient (100 ms) | V_{IN} | -0.6 to 30 -0.6 to 30 | V |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Negative voltage will not damage device provided that the power dissipation is limited to the rated allowable power for the package.

Table 2. THERMAL RATINGS

| Rating | Symbol | Value | Unit |
|--|------------------|-------|------|
| Thermal Resistance, Junction–to–Air (4 layer High–K JEDEC JESD51–7 PCB, 100 mm², 2 oz. Cu) | JA | 90 | °C/W |
| Thermal Characterization Parameter, Junction-to-Lead (4 layer High-K JEDEC JESD51-7 PCB, 100 mm², 2 oz. Cu) | J–L | 27.5 | °C/W |
| Thermal Characterization Parameter, Junction-to-Board (4 layer High-K JEDEC JESD51-7 PCB, 100 mm², 2 oz. Cu) | J–B | 27.5 | °C/W |
| Thermal Characterization Parameter, Junction-to-Case Top (4 layer High-K JEDEC JESD51-7 PCB, 100 mm², 2 oz. Cu) | J–T | 7.6 | °C/W |
| Total Power Dissipation @ T _A = 25°C (4 layer High–K JEDEC JESD51–7 PCB, 100 mm², 2 oz. Cu) Derate above 25°C | P _{max} | | |

| 222011110712 0117117101211101100 (VCC = 24 V, OL = 100 1, dV/ | ат р орон, т <u>е</u> | | = 20 0 dilioo | O CLI ICI WIOC II | 0.00.) |
|---|-----------------------|----------------------------|------------------------------|--------------------------|---------------|
| Characteristics | Symbol | Min | Тур | Max | Unit |
| POWER FET | | | | | |
| Delay Time (enabling of chip to I _D = 100 mA with 1 A resistive load) | T_{dly} | _ | 220 | _ | S |
| Kelvin ON Resistance (Note 2) T _J = 140°C (Note 3) | Rუგჯ\$hut | down)3 1 JET32 - | 5.077 398 6.589 60 | .90 759 3.77 – | 6 renf0325.0° |
| Continuous Current ($T_A = 25$ °C, 0.5 in ² copper) (Note 3) ($T_A = 80$ °C, minimum copper) | I _D | - | 4.2 2.5 | - | А |
| THERMAL LATCH | | | | | |
| Shutdown Temperature (Note 3) | T_{SD} | 150 | 175 | 200 | °C |
| Thermal Hysteresis (Auto-retry part only) | T _{Hyst} | _ | 45 | - | °C |
| Thermal Shutdown Response Time | T _{SDRes} | 10 | 15 | 20 | S |
| UNDERVOLTAGE PROTECTION | | | | | |
| Undervoltage Lockout | V _{UVLO} | 6 | 6.5 | 7 | V |
| UVLO Hysteresis | V_{Hyst} | _ | 0.80 | - | V |
| CURRENT LIMIT | | | | | |
| Kelvin Short Circuit Current Limit (R _{Limit} = 20 , Note 4) | I _{Lim-SS} | 1.76 | 2.1 | 2.64 | Α |
| Kelvin Overload Current Limit (R _{Limit} = 20 , Note 4) | I _{Lim-OL} | - | 4.6 | - | Α |
| dv/dt CIRCUIT | | | | | |
| Output Voltage Ramp Time (Enable to V _{OUT} = 23.7 V) | t _{slew} | _ | 2.0 | - | ms |
| Output Voltage Ramp Time (10% to 90% – V _{OUT} = 2.4 V to 21.6 V with 24 Load) | t _{slew} | - | 1.2 | - | ms |
| Maximum Capacitor Voltage | V _{max} | _ | _ | V _{CC} | V |
| ENABLE/FAULT | | | | | |
| Logic Level Low (Output Disabled) | V_{in-low} | 0.35 | 0.58 | 0.81 | V |
| Logic Level Mid (Thermal Fault, Output Disabled) | V_{in-mid} | 0.82 | 1.4 | 1.95 | V |
| Logic Level High (Output Enabled) | $V_{in-high}$ | 1.96 | 2.6 | 3.0 | V |
| High State Maximum Voltage | V _{in-max} | 2.51 | 4.6 | 5 | V |
| Logic Low Sink Current (V _{enable} = 0 V) | I _{in-low} | - | -15 | -25 | Α |
| Logic High Leakage Current for External Switch (V _{enable} = 3.3 V) | I _{in-leak} | - | - | 1.0 | Α |
| Maximum Fanout for Fault Signal (Total number of chips that can be connected to this pin for simultaneous shutdown) | Fan | - | - | 3.0 | Units |
| TOTAL DEVICE | | | | | |
| Bias Current (Operational) | I _{Bias} | _ | - | 450 | Α |
| Bias Current (Shutdown) | _ | = | · ' | = | - · |
| | | | | | |

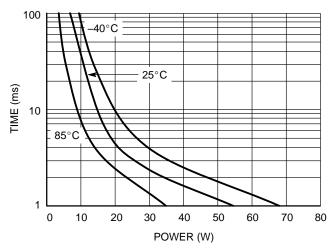


Figure 3. Thermal Trip Time vs. Power Dissipation

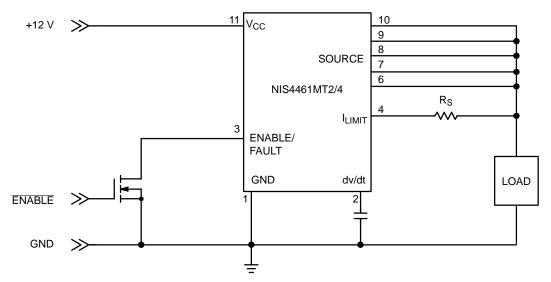


Figure 4. Application Circuit with Direct Current Sensing

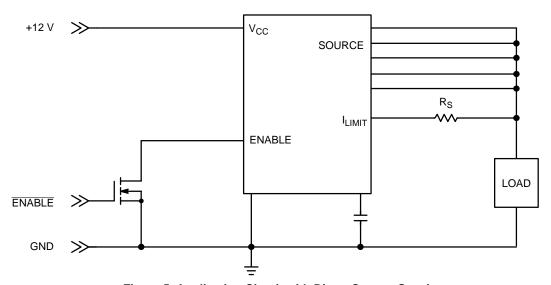


Figure 5. Application Circuit with Direct Current Sensing

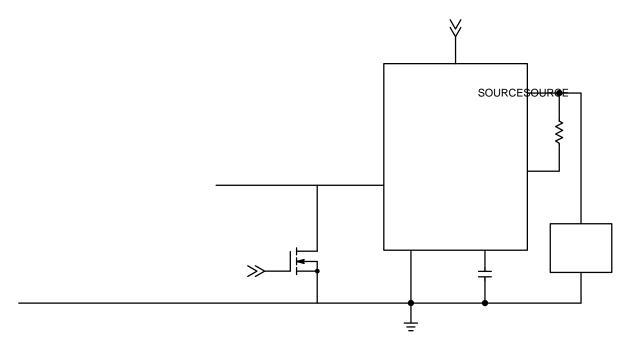
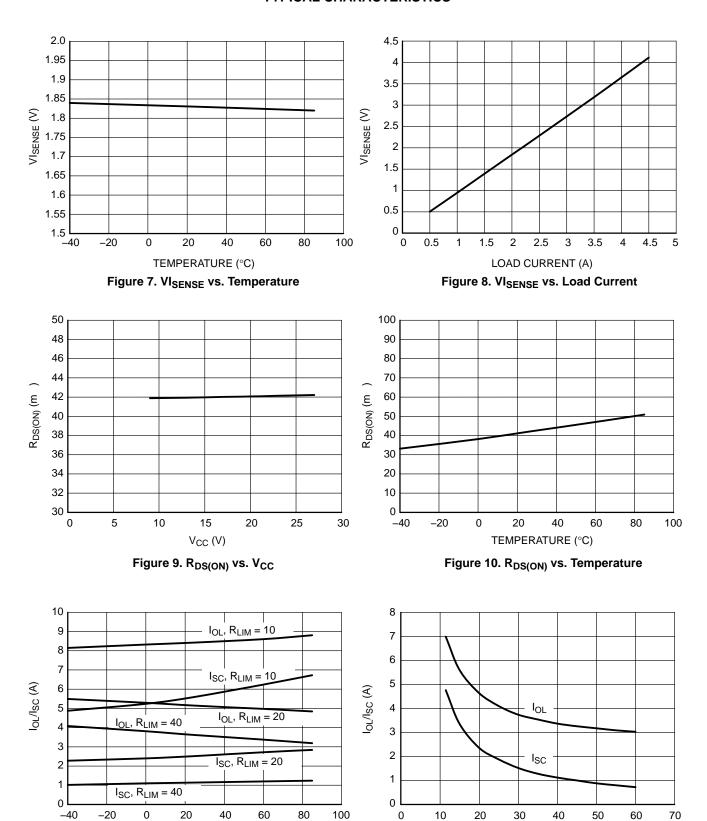


Figure 6. Common Thermal Shutdown

TYPICAL CHARACTERISTICS



 $\label{eq:temperature} \mbox{TEMPERATURE (°C)}$ Figure 11. \mbox{I}_{OL} and \mbox{I}_{SC} vs. Temperature

 $$\rm R_{LIM}\,(\)$$ Figure 12. I_{OL} and I_{SC} vs. R_{LIM}

TYPICAL CHARACTERISTICS

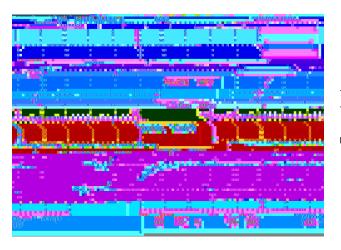


Figure 13. Slew Rate Control Screenshot

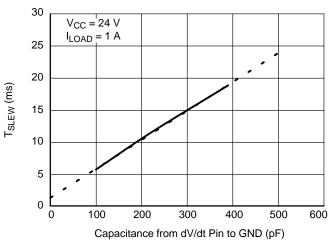


Figure 14. T_{SLEW} vs. dV/dt Capacitance

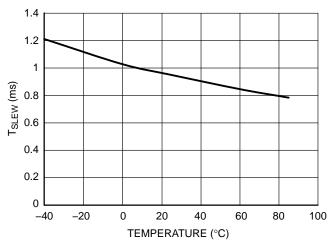


Figure 15. T_{SLEW} vs. Temperature

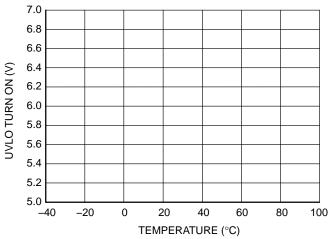


Figure 16. UVLO TURN ON vs. Temperature

APPLICATION INFORMATION

Basic Operation

This device is a self-protected, resettable, electronic fuse. It contains circuits to monitor the input voltage, output voltage, output current and die temperature.

On application of the input voltage, the device will apply the input voltage to the load based on the restrictions of the controlling circuits. The dv/dt of the output voltage will be controlled by the internal dv/dt circuit. The output voltage will slew from 0 V to the rated output voltage in 1 ms, unless additional capacitance is added to the dv/dt pin.

The device will remain on as long as the temperature does not exceed the 175°C limit that is programmed into the chip. The current limit circuit does not shut down the part but will reduce the conductivity of the FET to maintain a constant current at the internally set current limit level.

An internal charge pump provides bias for the gate voltage of the internal n-channel power FET and also for the current limit circuit. The remainder of the control circuitry operates between the input voltage ($V_{\rm CC}$) and ground.

Current Limit

a thermal shutdown of one device will cause both devices to disable their outputs. Both devices will turn on once the fault is removed for the auto-retry devices.

For the latching thermal device, the outputs will be enabled after the enable pin has been pulled to ground with an external switch and then allowed to go high or after the input power has been recycled. For the auto retry devices, both devices will restart as soon as the die temperature of the device in shutdown has been reduced to the lower thermal limit.

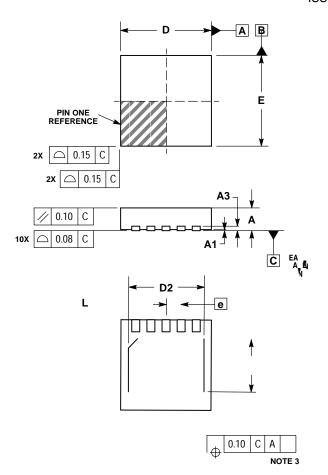
Thermal Protection

The NIS4461 includes an internal temperature sensing circuit that senses the temperature on the die of the power

FET. If the temperature reaches 175°C, the device will shut down, and remove power from the load. Output power can be restored by either recycling the input power or toggling the enable pin for thermally latching devices. Power will automatically be reapplied to the load for auto

PACKAGE DIMENSIONS

WDFN10, 3x3, 0.5P CASE 522AA **ISSUE A**



- NOTES:
 1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
 2. CONTROLLING DIMENSION: MILLIMETERS.
 3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30mm FROM TERMINAL.
 4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

| | E E | | | | |
|----|--------------|---------------|------|--|--|
| D | | _ | Α | | |
| Α | 0.7 0 | v i.75 | 0.80 | | |
| A1 | 0.00 | 0.03 0.05 | | | |
| A3 | 0.20 REF | | | | |
| | 0.18 | 0.24 | 0.30 | | |
| D | 3.00 BSC | | | | |
| D2 | 2.45 | 2.50 2.5 | | | |
| E | 3.00 BSC | | | | |
| E2 | 1.75 | 1.80 | 1.85 | | |
| | 0.50 BSC | | | | |
| | 0 19 TVP | | | | |