NIS1050

Protection Interface Circuit for PMICs with Integrated OVP Control

The NIS1050 is a protection IC targeted at the latest generation of PMICs from the leading mobile phone and UMPC chipset vendors. It includes a highly stable low-current LDO and a low impedance power N-Channel MOSFET.

The LDO provides a low current, five volt supply to the PMIC, and the NFET is the external pass element for the OVIC circuit. These stages combine with the internal PMIC to protect the charging circuit from low-impedance overvoltage conditions that can occur from either the AC/DC or USB supply.

The NIS1050 is available in the low−profile 6-lead 2x2mm WDFN6 surface mount package.

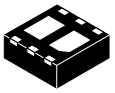
Features

- Lower Power Dissipation and Higher Efficiency vs. Zener Shunt Regulator
- LDO Highly Stable across Temperature, Operates Without Bypass Capacitors
- Wide 3-30 V Power Supply Voltage Input Range
- Low−Profile (0.75mm) 6-Lead 2x2mm WDFN6 Package
- This is a Pb−Free Device

Typical Applications

- Power Interface for New Generation PMICs from Leading Mobile Phone and UMPC Chipset Vendors

http://onsemi.com



WDFN6, 2x2
CASE 506AN

MARKING DIAGRAMS

PM = Specific Device Code
M = Date Code

ORDERING INFORMATION

Device	Package	Shipping†
NIS1050MNTBG	WDFN6 (Pb−Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

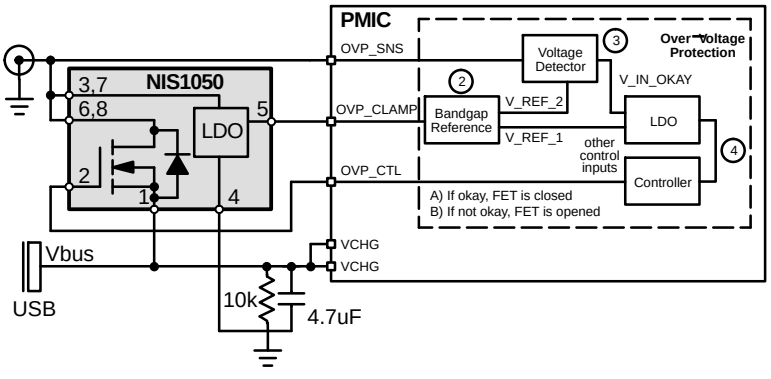


Figure 1. Typical Application

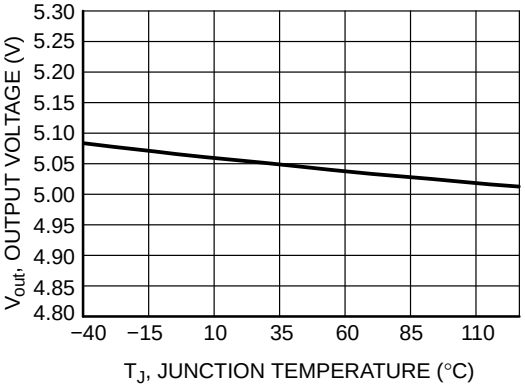


Figure 2. Output Voltage Variation with Temperature

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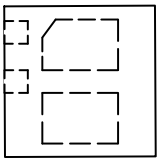

Figure 3. Pin Assignment

Table 4. ELECTRICAL CHARACTERISTICS (Unless otherwise noted: Vcc (OVP_sense) = 5.0 V, T_J = 25°C)

Characteristics	Symbol	Min	Typ	Max	Unit
POWER FET					
Zero Gate Voltage Drain Current (V_{DS} = 24 V_{dc}, V_{GS} = 0 V) T_J = 85°C	I_{DSS}			1.0 10	μA
Gate-to-Source Leakage Current (V_{DS} = 0 V, V_{GS} = ±8 V)	I_{GSS}			100	nA
Gate Threshold Voltage (V_{GS} = V_{DS}, I_D = 250 μA)	$V_{GS(th)}$	0.4	0.7	1.0	V
Negative Gate Threshold Temperature Coefficent	$V_{GS(th)}/T_J$		2.8		mV/°C
Drain-to-Source On-Resistance (Note 5) V_{GS} = 4.5 V, I_D = 2.0 A V_{GS} = 2.5 V, I_D = 2.0 A	$R_{DS(on)}$		 47 56	 70 90	mΩ
Forward Transconductance (V_{DS} = 5 V, I_D = 2.0 A)	g_{FS}		4.5		

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