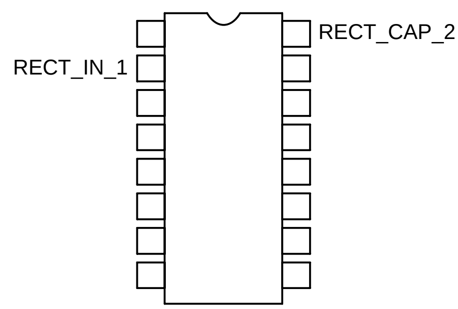
http://onsemi.com

SOIC−16 WB
D SUFFIX
CASE 751G

**PIN CONNECTIONS**




(Top View)

**ORDERING INFORMATION**

See detailed ordering and shipping information in the package dimensions section on page 9 of this data sheet.

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|---|---|---|---|
| Maximum Operating Voltage | $V_{CC}$ | 24 | $V_{DC}$ |
| Operating Ambient Temperature Range | $T_A$ | 0 to +70 | °C |
| Operating Junction Temperature | $T_J$ | 150 | °C |
| Power Dissipation | $P_D$ | 400 | mW |
| Thermal Resistance, Junction−to−Ambient | $R_{\theta JA}$ | 105 | °C/W |

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

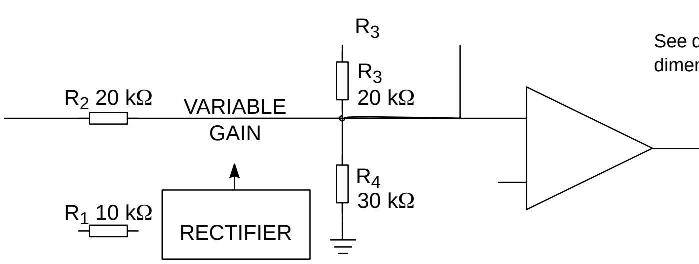



**Figure 1. Block Diagram**

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

## CIRCUIT DESCRIPTION

The NE570 compandor building blocks, as shown in the block diagram, are a full−wave rectifier, a variable gain cell, an operational amplifier and a bias system. The arrangement of these blocks in the IC result in a circuit which can perform well with few external components, yet can be adapted to many diverse applications.

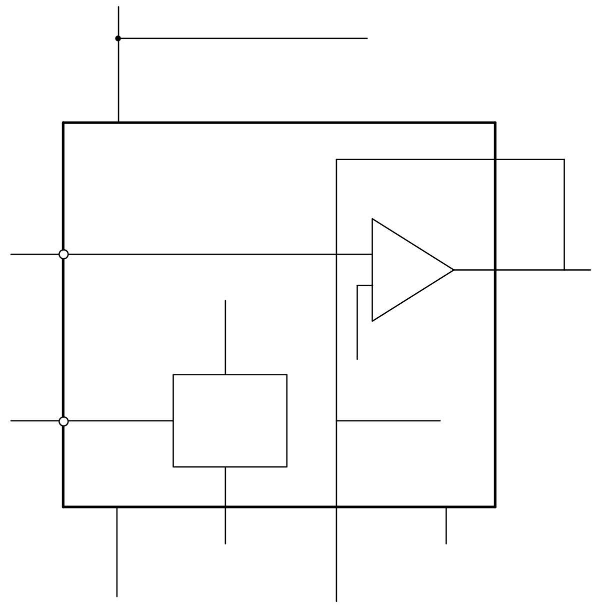
The full−wave rectifier rectifies the input current which flows from the rectifier input, to an internal summing node which is biased at $V_{REF}$. The rectified current is averaged on an external filter capacitor tied to the $C_{RECT}$ terminal, and the average value of the input current controls the gain of the variable gain cell. The gain will thus be proportional to the average value of the input signal for capacitively−coupled voltage inputs as shown in the following equation. Note that for capacitively−coupled inputs there is no offset voltage capable of producing a gain error. The only error will come from the bias current of the rectifier (supplied internally) which is less than 0.1 μA.

$$G \propto \frac{|V_{IN} - V_{REF}|\,avg}{R_1}$$

or

$$G \propto \frac{|\,V_{IN}\,|\,avg}{R_1}$$

The speed with which gain changes to follow changes in input signal levels is determined by the rectifier filter capacitor. A small capacitor will yield rapid response but will not fully filter low frequency signals. Any ripple on the gain control signal will modulate the signal passing through the variable gain cell. In an expander or compressor application, this would lead to third harmonic distortion, so there is a trade−off to be made between fast attack and decay times and distortion. For step changes in amplitude, the



## BASIC CIRCUIT HOOK−UP AND OPERATION

Figure 5 shows the block diagram of one half of the chip, (there are two identical channels on the IC). The full−wave averaging rectifier provides a gain control current, $I_G$, for the variable gain (ΔG) cell. The output of the ΔG cell is a current which is fed to the summing node of the operational amplifier. Resistors are provided to establish circuit gain and set the output DC bias.

## CIRCUIT DETAILS−RECTIFIER

Figure 8 shows the concept behind the full−wave averaging rectifier. The input current to the summing node of the op amp, $V_{IN}/R_1$, is supplied by the output of the op amp. If we can mirror the op amp output current into a unipolar current, we will have an ideal rectifier. The output current is averaged by $R_5$, $C_R$, which set the averaging time constant, and then mirrored with a gain of 2 to become $I_G$, the gain control current.

Figure 9 shows the rectifier circuit in more detail. The op amp is a one−stage op amp, biased so that only one output device is on at a time. The non−inverting input, (the base of $Q_1$), which is shown grounded, is actually tied to the internal 1.8 V $V_{REF}$. The inverting input is tied to the op amp output, (the emitters of $Q_5$ and $Q_6$), and the input summing resistor

At very high frequencies, the response of the rectifier will fall off. The roll−off will be more pronounced at lower input levels due to the increasing amount of gain required to switch between $Q_5$ or $Q_6$ conducting. The rectifier frequency response for input levels of 0 dBm, −20 dBm, and −40 dBm is shown in Figure 11. The response at all three levels is flat to well above the audio range.

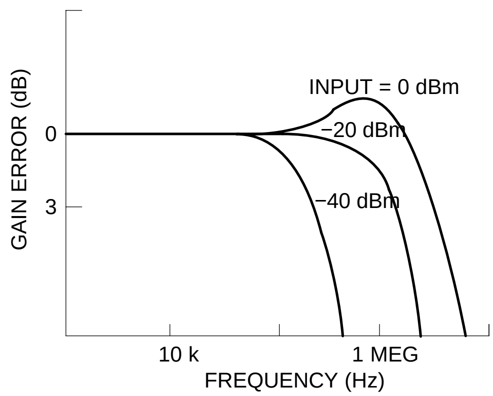
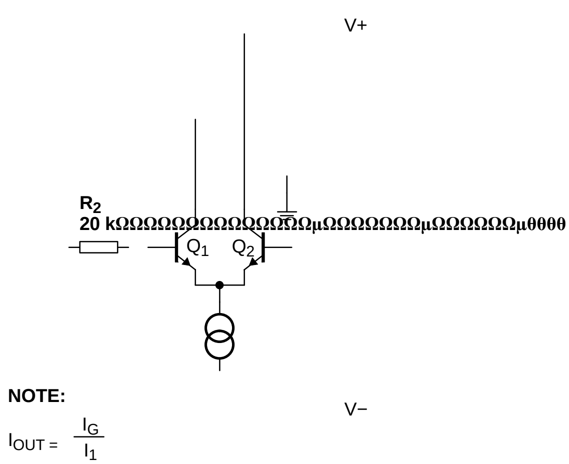



**Figure 11. Rectifier Frequency Response vs. Input Level**

## VARIABLE GAIN CELL

Figure 12 is a diagram of the variable gain cell. This is a linearized two−quadrant transconductance multiplier. $Q_1$, $Q_2$ and the op amp provide a predistorted drive signal for the gain control pair, $Q_3$ and $Q_4$. The gain is controlled by $I_G$ and a current mirror provides the output current.



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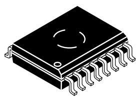
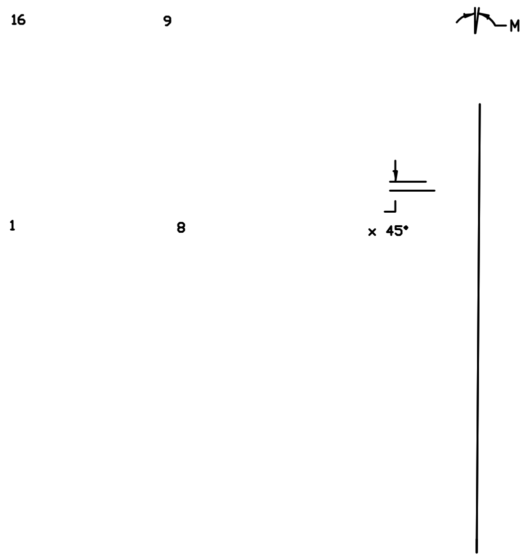


## SOIC−16 WB

SCALE 1:1




### GENERIC
### MARKING DIAGRAM*