nse '

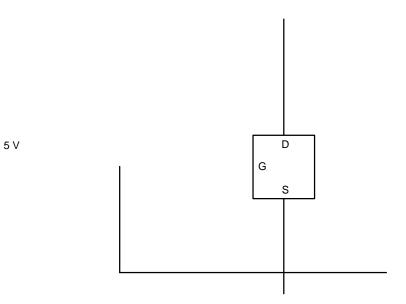
## **MAXIMUM RATINGS** ( $T_J = 25 C$ unless otherwise noted)

Rating		Value	Unit
Drain-to-Source Voltage Internally Clamped	$V_{DSS}$	42	Vdc
Drain-to-Gate Voltage Internally Clamped $(R_{GS} = 1.0 \text{ M}\Omega)$	$V_{DGR}$	42	V
Gate-to-Source Voltage	V <sub>GS</sub>	14	Vdc
Continuous Drain Current	D	Internally Limited	
Gate Input Current (V <sub>GS</sub> = 14 V <sub>DC</sub> )		10	mA
Source to Drain Current	SD	4.0	Α

Total Power Dissipation
@ T<sub>A</sub> = 25 C (Note 1)
@ T<sub>A</sub>

ELECTRICAL CHARACTERISTICS (T <sub>J</sub> = 25				

### **TEST CIRCUITS AND WAVEFORMS**



## **TEST CIRCUITS AND WAVEFORMS**

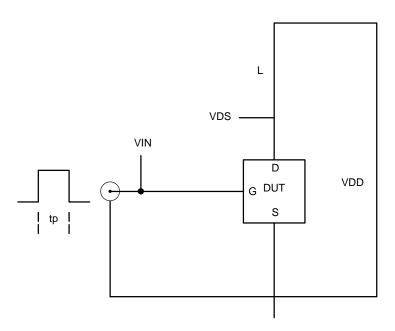


Figure 4. Inductive Load Switching Test Circuit

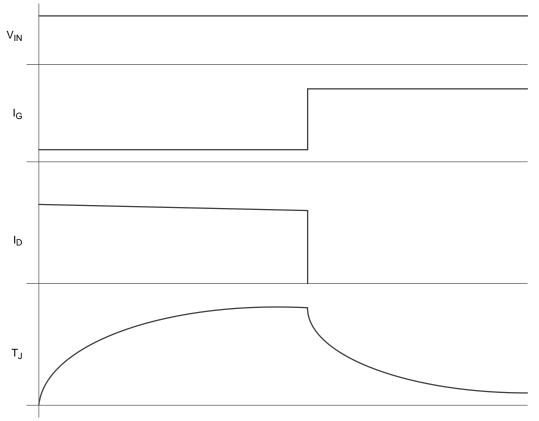


Figure 6. Short-Circuit Protection Behavior

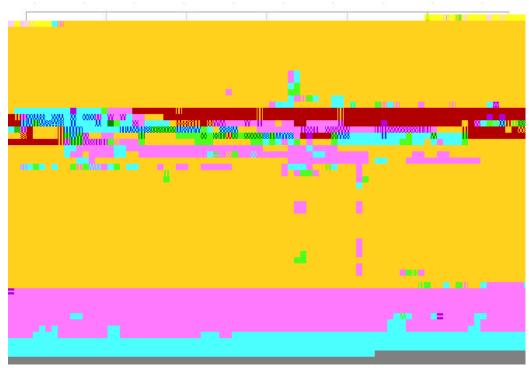
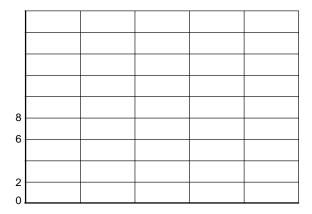


Figure 7. Turn on into Short Circuit Device Response

### **TYPICAL CHARACTERISTICS**



### **TYPICAL CHARACTERISTICS**

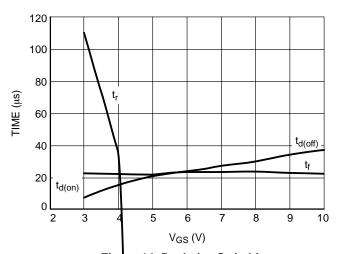


Figure 14. Resistive Switching

# 4 1 2 3 3 SCALE 1:1

### DPAK (SINGLE GAUGE) CASE 369C ISSUE G

DATE 31 MAY 2023

STYLE 1: PIN 1. BASE 2. COLLECTOR 3. EMITTER	STYLE 2: PIN 1. GATE 2. DRAIN 3. SOURCE	STYLE 3: PIN 1. ANODE 2. CATHODE 3. ANODE	STYLE 4: PIN 1. CATHODE 2. ANODE 3. GATE 4. ANODE	STYLE 5: PIN 1. GATE 2. ANODE 3. CATHODE
4. COLLECTOR	4. DRAIN	<ol><li>CATHODE</li></ol>	4. ANODE	4. ANODE

STYLE 6: PIN 1. MT1 2. MT2 3. GATE	STYLE 7: PIN 1. GATE 2. COLLECTOR 3. EMITTER	STYLE 8: PIN 1. N/C 2. CATHODE 3. ANODE	PIN 1. ANODE 2. CATHODE 3. RESISTOR ADJUST	STYLE 10: PIN 1. CATHODE 2. ANODE 3. CATHODE
4. MT2	4. COLLECTOR	4. CATHODE	4. CATHODE	4. ANODE

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