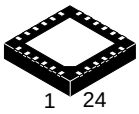
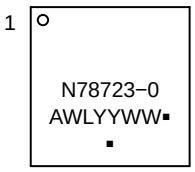
High Efficiency Buck Dual LED Driver with Integrated Current Sensing for Automotive Front Lighting

NCV78723





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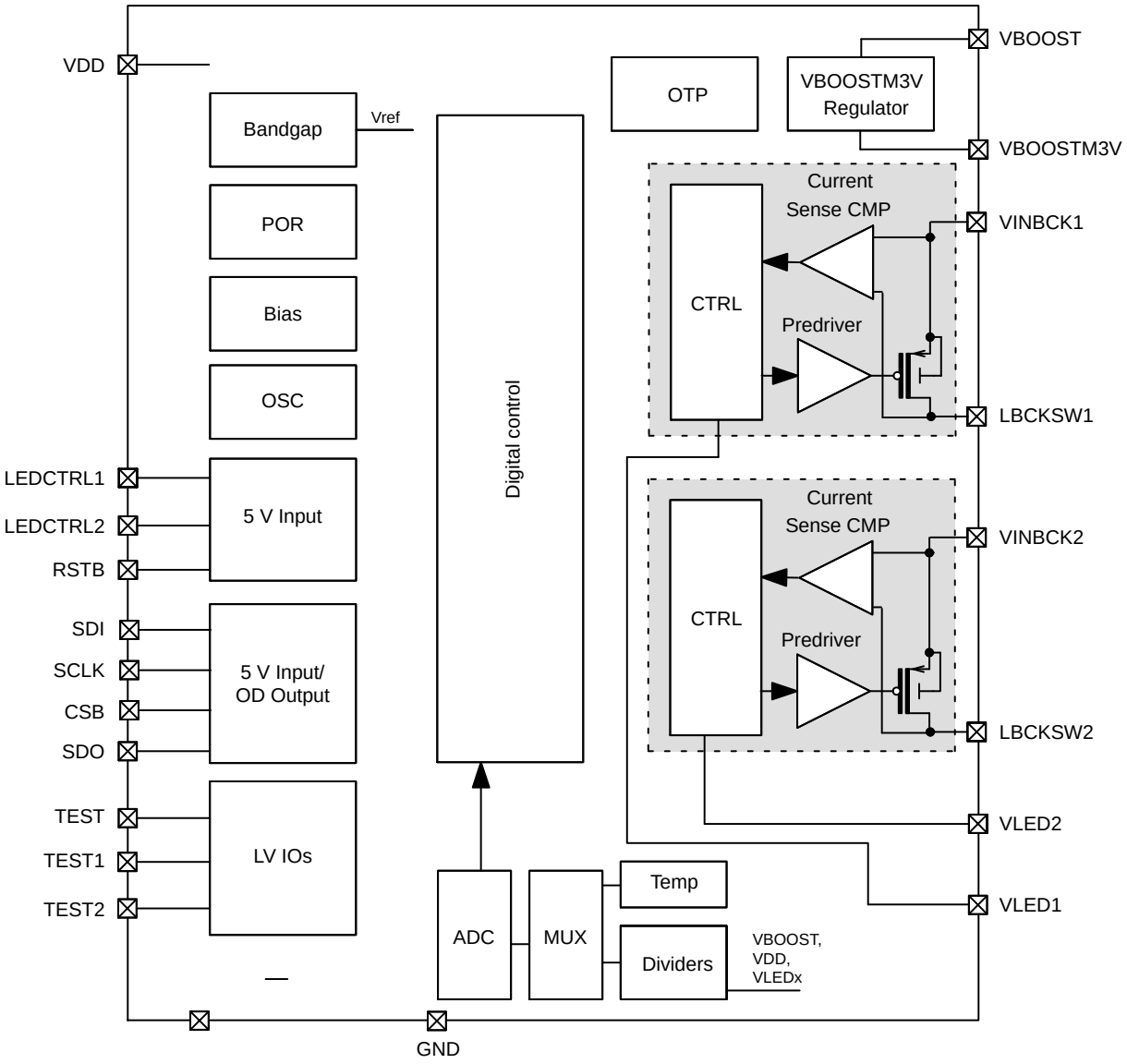
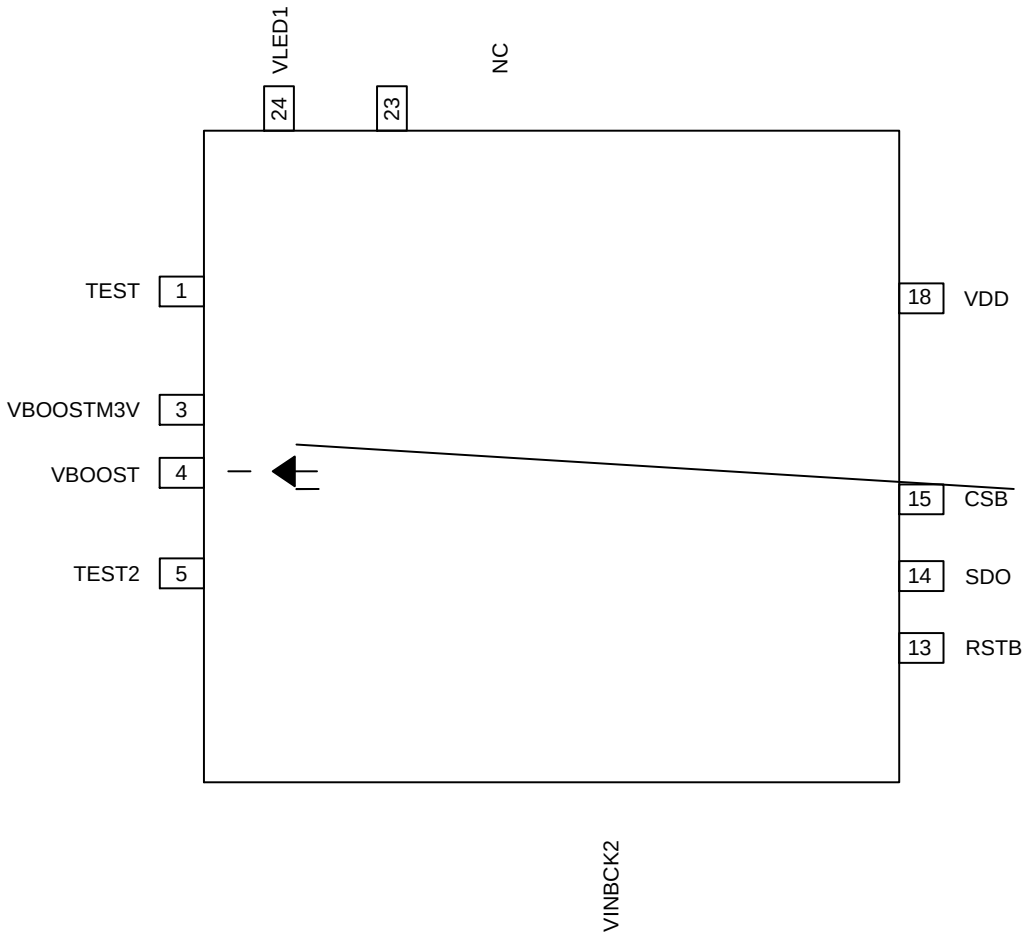
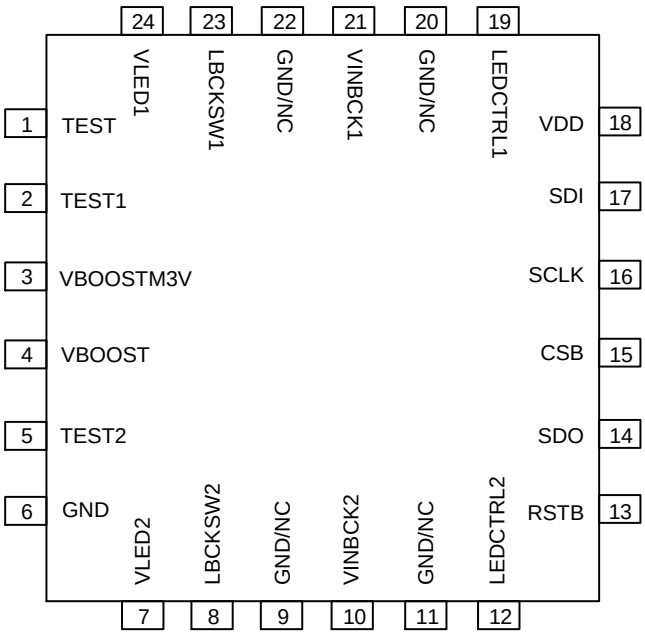
See detailed ordering and shipping information on page 31 of this data sheet.

Publication Order Number:


VDD
Bandgap
Vref
POR
Bias
OSC
Digital control
OTP
VBOOSTM3V
Regulator
VBOOST
VBOOSTM3V
Current
Sense CMP
VINBCK1
CTRL
Predriver
LBCKSW1
LEDCTRL1
LEDCTRL2
RSTB
5 V Input
Current
Sense CMP
VINBCK2
CTRL
Predriver
SDI
SCLK
CSB
SDO
5 V Input/
OD Output
LBCKSW2
TEST
TEST1
TEST2
LV IOs
VLED2
VLED1
ADC
MUX
Temp
Dividers
VBOOST,
VDD,
VLEDx
GND


VLED1
24
NC
23
TEST
1
VBOOSTM3V
3
VBOOST
4
TEST2
5
18
VDD
15
CSB
14
SDO
13
RSTB
VINBCK2



1	TEST	Test Pin	LV In
2	TEST1	Test Pin	LV IN/OUT HV Tolerant
3	VBOOSTM3V	VBOOSTM3V Regulator Output Pin	HV OUT (Supply)
4	VBOOST	Booster Input Voltage Pin	HV Supply
5	TEST2	Test Pin	LV IN/OUT HV Tolerant
6	GND	Ground	Ground
7	VLED2		

VBOOST Supply Voltage	V_{BOOST}	−0.3	+68	V

Thermal Resistance Junction to Exposed Pad (Note 17)	QFN24 5x5	R_{thjp}	−	5	−	°C/W

17. Includes also typical solder thickness under the Exposed Pad (EP).

(All Min and Max parameters are guaranteed over full junction temperature (T_{JP}) range (−40°C; 150°C), unless otherwise specified)

The VDD Current Consumption	I_VDD		−	−	6	mA
POR Toggle Level on VDD Rising	POR_{3V_H}		2.7	−	3.05	V
POR Toggle Level on VDD Falling	POR_{3V_L}		2.45	−	2.8	V
POR Hysteresis	POR_{3V_HYST}		0.01	0.2	0.75	V
OTP UV Toggle Level on VBOOST	OTP_UV		13	−	15	V
OTP UV Toggle Level Hysteresis	OTP_UV_HYST		0.01	0.2	0.75	V

VBSTM3 Regulator Output Voltage	V_{BSTM3}	Referenced to VBOOST	−3.6	−3.3	−3.0	V
DC Output Current Consumption N78723−0 Device N78723−2 Device	M3V_IOUT		 − −	 5 5	 28 (Note 18) 22.5 (Note 19)	mA
Output Current Limitation	M3V_ILIM		−	−	200	mA
VBSTM3 External Decoupling Cap.	$C_{VBSTM3V}$	Referenced to VBOOST	0.3	−	2.2	μF
VBSTM3 Ext. Decoupling Cap. ESR	$C_{VBSTM3V}$_ESR	Referenced to VBOOST	−	−	200	mΩ
VBOOST POR Level on N78723−2 Device (Note 20)	M3V_VBSTPOR		3.5	−	5.5	V

System Oscillator Frequency	FOSC10M		8	10	12	MHz

ADC Resolution	ADC_RES		−	8	−	Bits
Nonlinearity Integral (INL) Differential (DNL)	 ADC_INL ADC_DNL	Best Fitting Straight Line Method	 −1.5 −2.0	 − −	 +1.5 +2.0	LSB
Full Path Gain Error for Measurements of V_{DD}, V_{LEDx}, V_{BOOST}	ADC_GAINER		−3.25	−	3.25	%
Offset at Output of ADC	ADC_OFFSET		−2	−	2	LSB
Time for 1 SAR Conversion	ADC_CONV	Full Conversion of 8 Bits	6.67	8	10	μs
ADC Full Scale for V_{DD} Measurement	ADCFS_VDD		3.87	4	4.13	V

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

18. V_{BOOST} = 68 V, $V_{LED1,2}$ = 34 V, f_{BUCK} = 2 MHz, maximum total gate charge for both activated BUCK channels Q_{GATE} = 14 nC.
19. V_{BOOST} = 68 V, $V_{LED1,2}$ = 34 V, f_{BUCK} = 1.61 MHz, maximum total gate charge for both activated BUCK channels Q_{GATE} = 14 nC.
20. On N78723−2 device, the Buck switch is switched off when VBOOST drops below M3V_VBSTPOR level. When VBOOST returns back above M3V_VBSTPOR level, normal operation is restored.

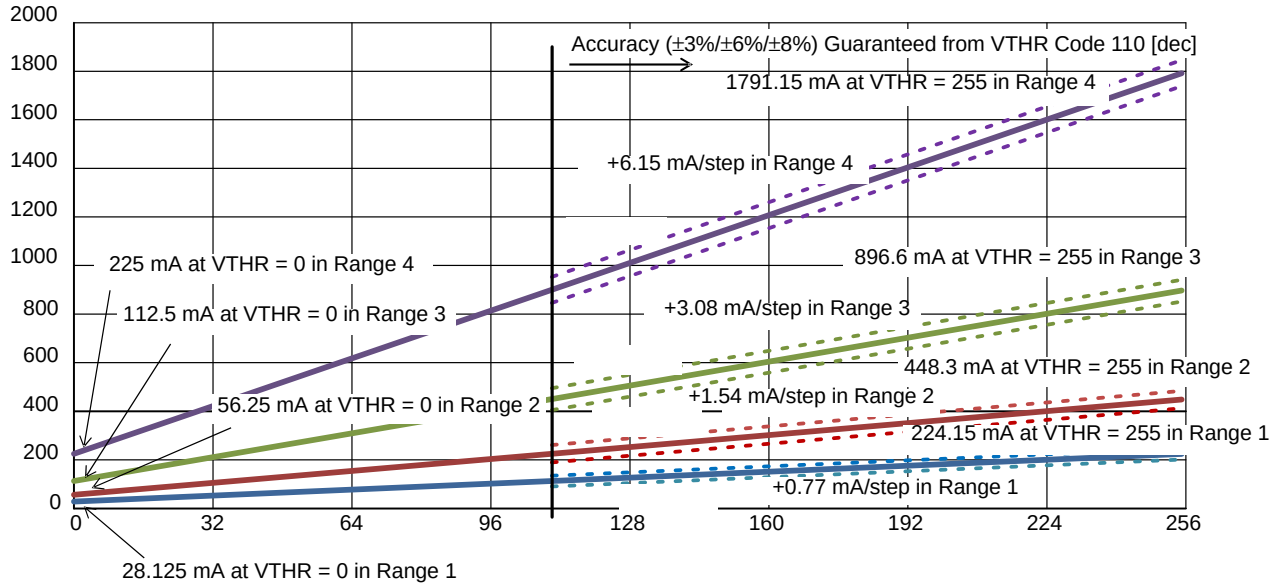
(continued)

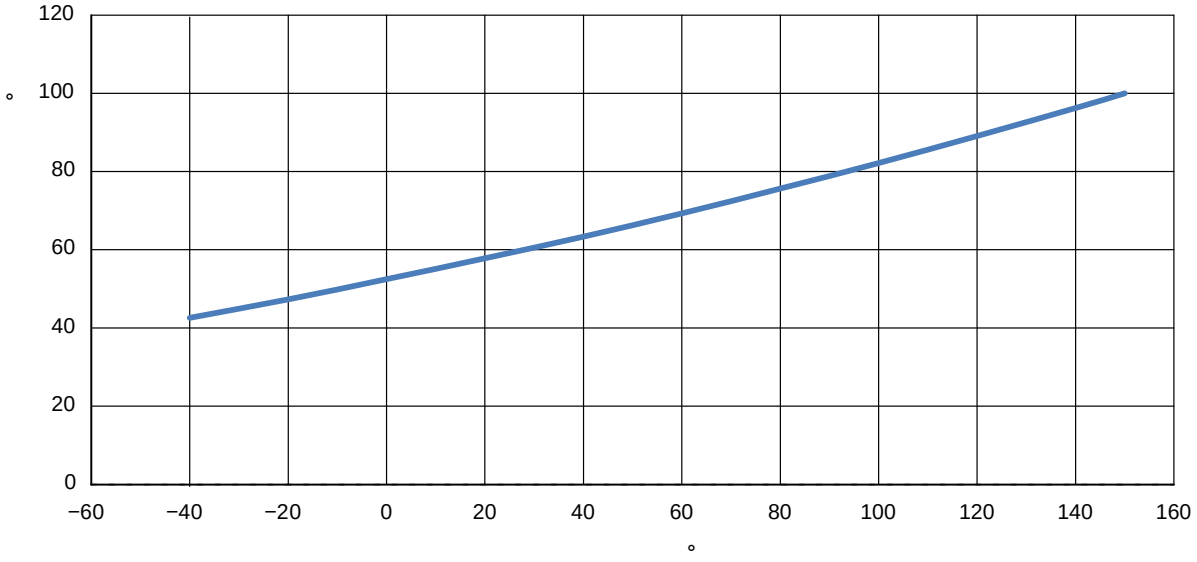
(All Min and Max parameters are guaranteed over full junction temperature (T_{JP}) range (−40°C; 150°C), unless otherwise specified)

ADC Full Scale for V_{LEDx} Measurement	ADCFS_VLED00 ADCFS_VLED01 ADCFS_VLED10 ADCFS_VLED11	The V_{LED} Range Code is “00” The V_{LED} Range Code is “01” The V_{LED} Range Code is “10” The V_{LED} Range Code is “11”	67.725 48.375 38.700 29.025	70 50 40 30	72.275 51.625 41.300 30.975	V
ADC Full Scale for V_{BOOST} Measurement	ADCFS_VBST		67.725	70	72.275	V
ADC Full Scale for Temp. Measurement N78723−0 Device N78723−2 Device	ADCFS_TEMP		 193.5 190	 200 200	 206.5 210	°C
TSD Threshold Level	ADC_TSD	ADC Measurement of Junction Temperature	163	169	175	°C
Temperature Measurement Accuracy at Hot	ADC_TEMPHOT	t = 125°C	−8	−	8	°C
Temperature Measurement Accuracy at Cold	ADC_TEMPCOLD	t = −40°C	−15	−	15	°C
V_{LEDx} Input Impedance N78723−0 Device N78723−2 Device	VLED_RES		 210 280	 − −	 650 790	kΩ
–						
On Resistance, Range 1	Rdson1	At Room-Temperature, I(VINBCKx) = 0.18 A, V(BOOST − VINBCKx) ≤ 0.2 V	−	−	5.2	Ω
On Resistance at Hot, Range 1	Rdson1_hot	At Tj = 150 °C, I(VINBCKx) = 0.18 A, V(BOOST − VINBCKx) ≤ 0.2 V	−	−	7.2	Ω
On Resistance, Range 2	Rdson2	At Room-Temperature, I(VINBCKx) = 0.375 A, V(BOOST − VINBCKx) ≤ 0.2 V	−	−	2.6	Ω
On Resistance at Hot, Range 2	Rdson2_hot	At Tj = 150 °C, I(VINBCKx) = 0.375 A, V(BOOST − VINBCKx) ≤ 0.2 V	−	−	3.6	Ω
On Resistance, Range 3	Rdson3	At Room-Temperature, I(VINBCKx) = 0.75 A, V(BOOST − VINBCKx) ≤ 0.2 V	−	−	1.3	Ω
On Resistance at Hot, Range 3	Rdson3_hot	At Tj = 150 °C, I(VINBCKx) = 0.75 A, V(BOOST − VINBCKx) ≤ 0.2 V	−	−	1.8	Ω
On Resistance, Range 4	Rdson4	At Room-Temperature, I(VINBCKx) = 1.5 A, V(BOOST − VINBCKx) ≤ 0.2 V	−	−	0.65	Ω
On Resistance at Hot, Range 4	Rdson4_hot	At Tj = 150 °C, I(VINBCKx) = 1.5 A, V(BOOST − VINBCKx) ≤ 0.2 V	−	−	0.9	Ω
Switching Slope – ON Phase (Note 21)	T_{RISE}		−	3	−	V/ns
Switching Slope – OFF Phase						

(continued)

(continued)


2000
1800
1600
1400
1200
1000
800
600
400
200
0
0
32
64
96
128
160
192
224
256
Accuracy (±3%/±6%/±8%) Guaranteed from VTHR Code 110 [dec]
1791.15 mA at VTHR = 255 in Range 4
+6.15 mA/step in Range 4
225 mA at VTHR = 0 in Range 4
896.6 mA at VTHR = 255 in Range 3
112.5 mA at VTHR = 0 in Range 3
+3.08 mA/step in Range 3
448.3 mA at VTHR = 255 in Range 2
56.25 mA at VTHR = 0 in Range 2
+1.54 mA/step in Range 2
224.15 mA at VTHR = 255 in Range 1
+0.77 mA/step in Range 1
28.125 mA at VTHR = 0 in Range 1


120
100
80
60
40
20
0
−60
−40
−20
0
20
40
60
80
100
120
140
160


LED current

:

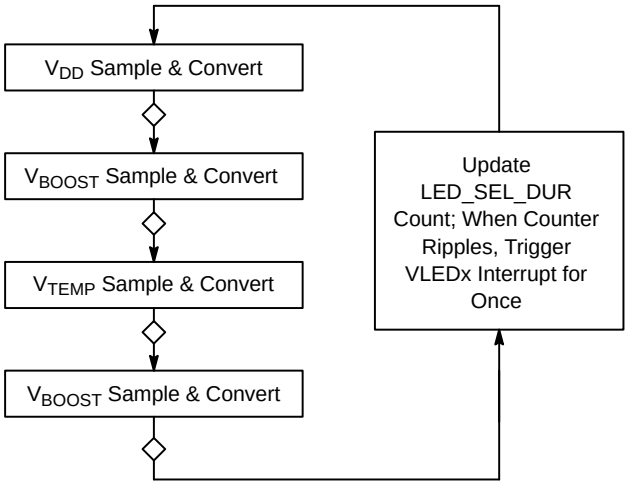
±

δ . . . –

– *Buck Regulator – Current Regulation*

δ –

higher current capability



μ –

μ

μ

$$T_{VLEDx\_INT\_Forced} = LED\_SEL\_DUR[8:0] \cdot T_{ADC\_SEQ} \quad \text{(eq. 4)}$$

digital dimming

thermal warning *thermal shutdown*

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BUCK1_EN **BUCK2_EN**

μ

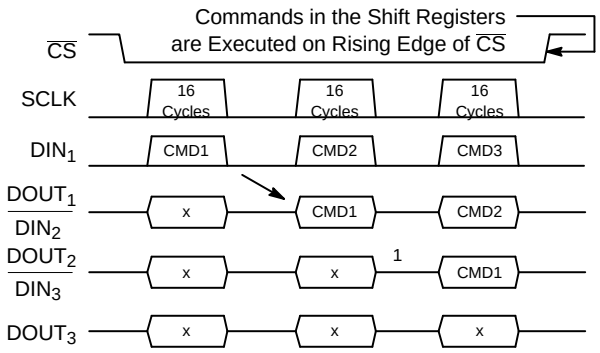
OTP Lock Bit

- **Stand-Alone**

  LEDCTRLx

- **Fail-Safe**

OTP Lock Bit


Commands in the Shift Registers
are Executed on Rising Edge of $\overline{CS}$
$\overline{CS}$
SCLK
16 Cycles
16 Cycles
16 Cycles
DIN_1
CMD1
CMD2
CMD3
$DOUT_1$
$\overline{DIN_2}$
x
CMD1
CMD2
$DOUT_2$
$\overline{DIN_3}$
x
x
1
CMD1
$DOUT_3$
x
x
x

0x00	NA	NOP Register (Read/Write Operation Ignored)									
0x01	R/W	BUCK1_ISENS_THR[1:0]		BUCK1_VTHR[7:0]							
0x02	R/W	BUCK2_ISENS_THR[1:0]		BUCK2_VTHR[7:0]							
0x03	R/W	BUCK1_TOFF[4:0]					BUCK2_TOFF[4:0]				
0x04	R/W	BUCK1_OFF_CMP_DIS (Note 31)	BUCK2_OFF_CMP_DIS (Note 31)	DRV_SLOW_EN (Note 31)	BUCKx_OC_OCCMP_THR[1:0]		FSO_MD[2:0]			BUCK1_EN	BUCK2_EN
0x05	R/W	BUCK1_TSD_AUT_RCVR_EN	BUCK2_TSD_AUT_RCVR_EN	THERMAL_WARNING_THR[7:0]							
0x06	R/W	VTEMP_OFF_COMP ODD PAR (Note 30)	LED_SEL_DUR[8:0]								
0x07	R/W	VTEMP_OFF_COMP[2:0] (Note 30)			BUCK1_ISENS_TRIM[6:0]						
0x08	R/W	VTEMP_OFF_COMP[5:3] (Note 30)			BUCK2_ISENS_TRIM[6:0]						
0x09	R/W	ADC_VLED1_RNG_SEL[1:0]		ADC_VLED2_RNG_SEL[1:0]		OTP_BIAS_H	OTP_BIAS_L	OTP_ADDR[1:0]		OTP_OPERATION[1:0]	
0x0A	R	0x0	ODD PARITY	VLED1ON[7:0]							
0x0B	R	0x0	ODD PARITY	VLED2ON[7:0]							
0x0C	R	0x0	ODD PARITY	VLED1[7:0]							
0x0D	R	0x0	ODD PARITY	VLED2[7:0]							
0x0E	R	0x0	ODD PARITY	VTEMP[7:0]							
0x0F	R	0x0	ODD PARITY	VBOOST[7:0]							
0x10	R	0x0	ODD PARITY	VDD[7:0]							
0x11	R	0x0	ODD PARITY	BUCK1_TON_DUR[7:0]							
0x12	R	0x0	ODD PARITY	BUCK2_TON_DUR[7:0]							
0x13	R	0x0	ODD PARITY	0x0		OPENLED1	SHORTLED1	OCLED1	OPENLED2	SHORTLED2	OCLED2
0x14	R	0x0	ODD PARITY	OTP_FAIL	FSO	HWR	LED1VAL	LED2VAL	SPIERR	TSD	TW
0x15	R	0x0	ODD PARITY	0x0			OTP_ACTIVE	BUCK1_MIN_TON	BUCK2_MIN_TON	BUCK1_STATUS	BUCK2_STATUS
0x16	R	0x0	ODD PARITY	0x0	BUCK1_ISENS_RNG[6:0]						
0x17	R	0x0	ODD PARITY	0x0	BUCK2_ISENS_RNG[6:0]						
0x18	R	0x0	ODD PARITY	BUCK2_ISENS_D1[3:0]				BUCK1_ISENS_D1[3:0]			
0x19	R	0x0	ODD PARITY	BUCK2_ISENS_D2[3:0]				BUCK1_ISENS_D2[3:0]			
0x1A	R	0x0	ODD PARITY	BUCK2_ISENS_D3[3:0]				BUCK1_ISENS_D3[3:0]			
0x1B	R	0x0	ODD PARITY	BUCK_ISENS_TC1[3:0]				BUCK_ISENS_TC0[3:0]			
0x1C	R	0x0	ODD PARITY	BUCK_ISENS_TC3[3:0]				BUCK_ISENS_TC2[3:0]			
0x1D	R	0x0	ODD PARITY	0x0							TC_VERSION
0x1E	R	OTP_DATA[9:0]									
0x1F	R	0x0		REVID[7:0]							
OTHER	R	0x0									

30. Read Only.
31. Available only on N78723−2 device.

NOP	Bits [9:0] – ADDR_0x00	NOP Register (Read/Write Operation Ignored)

BUCK1_ISENS_THR[1:0]	Bits [9:8] – ADDR_0x01	Peak Current: Selection of the Range 1, 2, 3 or 4
BUCK1_VTHR[7:0]	Bits [7:0] – ADDR_0x01	Peak Current Comparator Threshold Value

BUCK2_ISENS_THR[1:0]	Bits [9:8] – ADDR_0x02	Peak Current: Selection of the Range 1, 2, 3 or 4
BUCK2_VTHR[7:0]	Bits [7:0] – ADDR_0x02	Peak Current Comparator Threshold Value

BUCK1_TOFF[4:0]	Bits [9:5] – ADDR_0x03	Buck 1 TOFF·VLED Constant Settings
BUCK2_TOFF[4:0]	Bits [4:0] – ADDR_0x03	Buck 2 TOFF·VLED Constant Settings

BUCK1_OFF_CMP_DIS	Bit 9 – ADDR_0x04	Buck 1 Offset Cancellation Disable
BUCK2_OFF_CMP_DIS	Bit 8 – ADDR_0x04	Buck 2 Offset Cancellation Disable
DRV_SLOW_EN	Bit 7 – ADDR_0x04	Slow Driver Slope Enable
BUCKx_OC_OCCMP_THR[1:0]	Bits [6:5] – ADDR_0x04	Overcurrent Detection Settings
FSO_MD[2:0]	Bits [4:2] – ADDR_0x04	FSO Mode Selection
BUCK1_EN	Bit 1 – ADDR_0x04	Buck Regulator Channel 1 Enable Bit
BUCK2_EN	Bit 0 – ADDR_0x04	Buck Regulator Channel 2 Enable Bit

(continued)

ODD PARITY	Bit 8 – ADDR_0x16	Odd Parity over Data
BUCK1_ISENS_RNG[6:0]	Bits [6:0] – ADDR_0x16	Trimming Constant for Highest Range on Hot for Buck 1 Peak Current

ODD PARITY	Bit 8 – ADDR_0x17	Odd Parity over Data
BUCK2_ISENS_RNG[6:0]	Bits [6:0] – ADDR_0x17	Trimming Constant for Highest Range on Hot for Buck 2 Peak Current

ODD PARITY	Bit 8 – ADDR_0x18	Odd Parity over Data
BUCK2_ISENS_D1[3:0]	Bits [7:4] – ADDR_0x18	Delta Trimming Constant for Buck 2 Peak Current
BUCK1_ISENS_D1[3:0]	Bits [3:0] – ADDR_0x18	Delta Trimming Constant for Buck 1 Peak Current

ODD PARITY	Bit 8 – ADDR_0x19	Odd Parity over Data
BUCK2_ISENS_D2[3:0]	Bits [7:4] – ADDR_0x19	Delta Trimming Constant for Buck 2 Peak Current
BUCK1_ISENS_D2[3:0]	Bits [3:0] – ADDR_0x19	Delta Trimming Constant for Buck 1 Peak Current

ODD PARITY	Bit 8 – ADDR_0x1A	Odd Parity over Data
BUCK2_ISENS_D3[3:0]	Bits [7:4] – ADDR_0x1A	Delta Trimming Constant for Buck 2 Peak Current
BUCK1_ISENS_D3[3:0]	Bits [3:0] – ADDR_0x1A	Delta Trimming Constant for Buck 1 Peak Current

ODD PARITY	Bit 8 – ADDR_0x1B	Odd Parity over Data
BUCK_ISENS_TC1[3:0]	Bits [7:4] – ADDR_0x1B	

			†
NCV78723MW0CR2G	N78723−0	QFN24 5 × 5 with Wettable Flank (Pb-Free)	5,000 / Tape & Reel
NCV78723MW0R2G	N78723−0	QFN24 5 × 5 with Wettable Flank (Pb-Free)	5,000 / Tape & Reel
NCV78723MW2R2G	N78723−2	QFNW24 5 × 5 with Step-cut Wettable Flank (Pb-Free)	5,000 / Tape & Reel
NCV78723MW2AR2G***	N78723−2	QFNW24 5 × 5 with Step-cut Wettable Flank (Pb-Free)	5,000 / Tape & Reel

** NCV78723MW2 & NCV78723MW0 have different package mold compound. Please contact for technical details.
*For additional information on our Pb-Free strategy and soldering details, please download the Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.
*** NCV78723MW2AR2G is recommended for new designs.

QFNW24 5x5, 0.65P