onsemi

High Efficiency Buck Dual LED Driver with Integrated Current Sensing for Automotive Front Lighting NCV78723

The NCV78723 is a single-chip and high efficient Buck Dual LED Driver designed for automotive front lighting applications like high beam, low beam, DRL (daytime running light), turn indicator, fog light, static cornering, etc. The NCV78723 is in particular designed for high current LEDs and provides a complete solution to drive 2 LED strings of up-to 60 V. It includes 2 independent current regulators for the LED strings and required diagnostic features for automotive front lighting with a minimum of external components - the chip doesn't need any external sense resistor for the buck current regulation. The available output current and voltages can be customized per individual LED string. When more than 2 LED channels are required on 1 module, then 2, 3 or more devices NCV 78723 can be combined; also with NCV78713 device - the derivative of the NCV78723 incorporating Buck Single LED Driver. Thanks to the SPI programmability, one single hardware configuration can support various application platforms.

Features

- Single Chip
- Buck Topology
- 2 LED Strings up-to 60 V
- High Current Capability up to 1.6 A DC per Output
- High Overall Efficiency
- Minimum of External Components
- Integrated High Accuracy Current Sensing
- Integrated Switched Mode Buck Current Regulator
- Average Current Regulation through the LEDs
- High Operating Frequencies to Reduce Inductor Sizes
- Low EMC Emission for LED Switching and Dimming
- SPI Interface for Dynamic Control of System Parameters
- Fail Safe Operating (FSO) Mode, Stand-Alone Mode
- These Devices are Pb–Free, Halogen Free/BFR Free and are RoHS Compliant

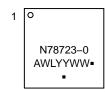
Typical Applications

- High Beam
- Low Beam
- DRL
- Position or Park Light
- Turn Indicator
- Fog
- Static Cornering



QFN24 CASE 485CS

MARKING DIAGRAMS



ORDERING INFORMATION

See detailed ordering and shipping information on page 31 of this data sheet.



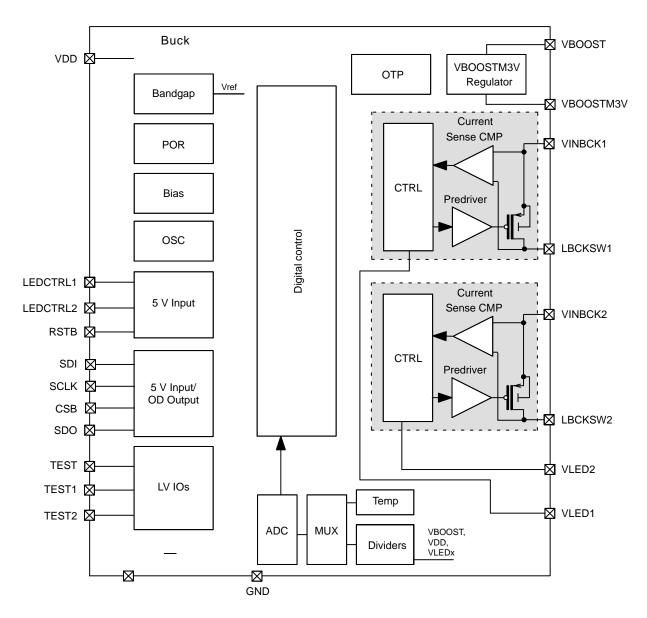


Figure 2. Block Diagram



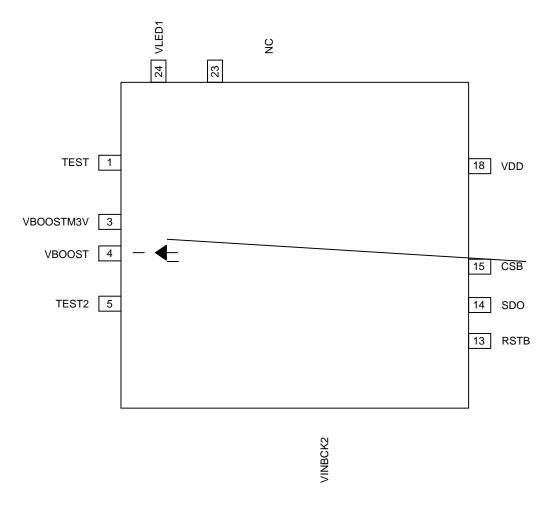
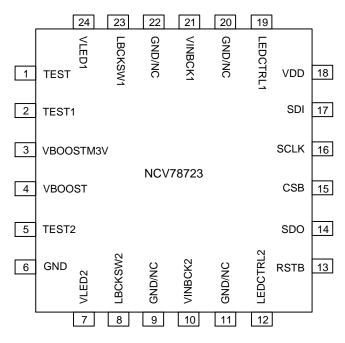


Figure 3. ESD Schematic

PACKAGE AND PIN DESCRIPTION



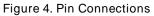


Table 2. PIN DESCRIPTION

Pin No.	Pin Name	Description	I/O Type
1	TEST	Test Pin	LV In
2	TEST1	Test Pin	LV IN/OUT HV Tolerant
3	VBOOSTM3V	VBOOSTM3V Regulator Output Pin	HV OUT (Supply)
4	VBOOST	Booster Input Voltage Pin	HV Supply
5	TEST2	Test Pin	LV IN/OUT HV Tolerant
6	GND	Ground	Ground
7	VLED2		

Table 3. ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Minimum	Maximum	Unit
VBOOST Supply Voltage	V _{BOOST}	-0.3	+68	V

Table 5. THERMAL RESISTANCE

Characteristic	Package	Symbol	Min	Тур	Max	Unit
Thermal Resistance Junction to Exposed Pad (Note 17)	QFN24 5x5	R _{thjp}	_	5	-	°C/W

17. Includes also typical solder thickness under the Exposed Pad (EP).

Table 6. ELECTRICAL CHARACTERISTICS

(All Min and Max parameters are guaranteed over full junction temperature (T_{JP}) range (-40°C; 150°C), unless otherwise specified)

Characteristic	Symbol	Condition	Min	Тур	Max	Unit
VDD: 3 V LOW VOLTAGE ANAL	OG AND DIGITAL SUP	PLY	•			•
The VDD Current Consumption	I_VDD		-	-	6	mA
POR Toggle Level on VDD Rising	POR _{3V_H}		2.7	-	3.05	V
POR Toggle Level on VDD Falling	POR _{3V_L}		2.45	-	2.8	V
POR Hysteresis	POR _{3V_HYST}		0.01	0.2	0.75	V
OTP UV Toggle Level on VBOOST	OTP_UV		13	-	15	V
OTP UV Toggle Level Hysteresis	OTP_UV_HYST		0.01	0.2	0.75	V
VBOOSTM3V: HIGH SIDE AUXIL	IARY SUPPLY					
VBSTM3 Regulator Output Voltage	V _{BSTM3}	Referenced to VBOOST	-3.6	-3.3	-3.0	V
DC Output Current Consumption N78723–0 Device	M3V_IOUT		_	5	28	mA
N78723–2 Device			-	5	(Note 18) 22.5 (Note 19)	
Output Current Limitation	M3V_ILIM		-	-	200	mA
VBSTM3 External Decoupling Cap.	C _{VBSTM3V}	Referenced to VBOOST	0.3	-	2.2	μF
VBSTM3 Ext. Decoupling Cap. ESR	C _{VBSTM3V} _ESR	Referenced to VBOOST	-	-	200	mΩ
VBOOST POR Level on N78723–2 Device (Note 20)	M3V_VBSTPOR		3.5	-	5.5	V
OSC10M: SYSTEM OSCILLATOR	R CLOCK					
System Oscillator Frequency	FOSC10M		8	10	12	MHz
ADC FOR MEASURING V _{BOOST} ,	V _{DD} , V _{LED1} , V _{LED2} , TE	MP				
ADC Resolution	ADC_RES		-	8	-	Bits
Nonlinearity Integral (INL) Differential (DNL)	ADC_INL ADC_DNL	Best Fitting Straight Line Method	-1.5 -2.0		+1.5 +2.0	LSB
Full Path Gain Error for Measurements of V _{DD} , V _{LEDx} , V _{BOOST}	ADC_GAINER		-3.25	-	3.25	%
Offset at Output of ADC	ADC_OFFSET		-2	-	2	LSB
Time for 1 SAR Conversion	ADC_CONV	Full Conversion of 8 Bits	6.67	8	10	μS
ADC Full Scale for V _{DD} Measurement	ADCFS_VDD		3.87	4	4.13	V

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.
18. V_{BOOST} = 68 V, V_{LED1,2} = 34 V, f_{BUCK} = 2 MHz, maximum total gate charge for both activated BUCK channels Q_{GATE} = 14 nC.
19. V_{BOOST} = 68 V, V_{LED1,2} = 34 V, f_{BUCK} = 1.61 MHz, maximum total gate charge for both activated BUCK channels Q_{GATE} = 14 nC.
20. On N78723–2 device, the Buck switch is switched off when VBOOST drops below M3V_VBSTPOR level. When VBOOST returns back above M3V_VBSTPOR level, normal operation is restored.

Table 6. ELECTRICAL CHARACTERISTICS (continued)

(All Min and Max parameters are guaranteed over full junction temperature (T_{JP}) range (-40°C; 150°C), unless otherwise specified)

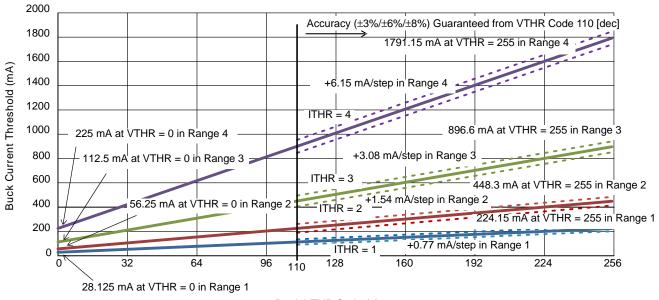
Characteristic	Symbol	Condition	Min	Тур	Max	Unit
DC FOR MEASURING VBOOST	, V _{DD} , V _{LED1} , V _{LED2} , TE	MP				
ADC Full Scale for V _{LEDx} Measurement	ADCFS_VLED00 ADCFS_VLED01 ADCFS_VLED10 ADCFS_VLED11	The V _{LED} Range Code is "00" The V _{LED} Range Code is "01" The V _{LED} Range Code is "10" The V _{LED} Range Code is "11"	67.725 48.375 38.700 29.025	70 50 40 30	72.275 51.625 41.300 30.975	V
ADC Full Scale for V _{BOOST} Measurement	ADCFS_VBST		67.725	70	72.275	V
ADC Full Scale for Temp. Measurement N78723–0 Device N78723–2 Device	ADCFS_TEMP		193.5 190	200 200	206.5 210	°C
TSD Threshold Level	ADC_TSD	ADC Measurement of Junction Temperature	163	169	175	°C
Temperature Measurement Accuracy at Hot	ADC_TEMPHOT	t = 125°C	-8	-	8	°C
Temperature Measurement Accuracy at Cold	ADC_TEMPCOLD	t = -40°C	-15	-	15	°C
V _{LEDx} Input Impedance N78723–0 Device N78723–2 Device	VLED_RES		210 280		650 790	kΩ
UCK REGULATOR - SWITCH						
On Resistance, Range 1	Rdson1	At Room-Temperature, I(VINBCKx) = 0.18 A , V(BOOST – VINBCKx) $\leq 0.2 \text{ V}$	-	-	5.2	Ω
On Resistance at Hot, Range 1	Rdson1_hot	At Tj = 150 °C, I(VINBCKx) = 0.18 A, V(BOOST – VINBCKx) ≤ 0.2 V	-	-	7.2	Ω
On Resistance, Range 2	Rdson2	At Room-Temperature, I(VINBCKx) = 0.375 A, V(BOOST – VINBCKx) ≤ 0.2 V	-	_	2.6	Ω
On Resistance at Hot, Range 2	Rdson2_hot	At Tj = 150 °C, I(VINBCKx) = 0.375 A, V(BOOST – VINBCKx) ≤ 0.2 V	-	_	3.6	Ω
On Resistance, Range 3	Rdson3	At Room-Temperature, I(VINBCKx) = 0.75 A, V(BOOST – VINBCKx) \leq 0.2 V	-	_	1.3	Ω
On Resistance at Hot, Range 3	Rdson3_hot	At Tj = 150 °C, I(VINBCKx) = 0.75 A, V(BOOST – VINBCKx) ≤ 0.2 V	-	_	1.8	Ω
On Resistance, Range 4	Rdson4	At Room-Temperature, I(VINBCKx) = 1.5 A, V(BOOST – VINBCKx) ≤ 0.2 V	-	-	0.65	Ω
On Resistance at Hot, Range 4	Rdson4_hot	At Tj = 150 °C, I(VINBCKx) = 1.5 A, V(BOOST – VINBCKx) ≤ 0.2 V	-	-	0.9	Ω
Switching Slope – ON Phase (Note 21)	T _{RISE}		-	3	-	V/ns

Switching Slope – OFF Phase

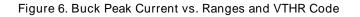
Table 6. ELECTRICAL CHARACTERISTICS (continued)

Table 6. ELECTRICAL CHARACTERISTICS (continued)





Buck VTHR Code (-)



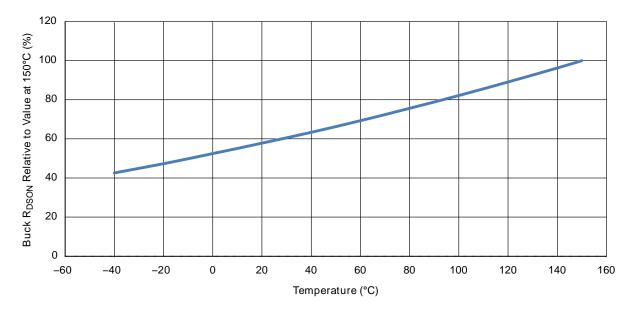


Figure 7. Typical Temperature Behavior of Buck Switch R_{DSON} Relative to the Value at 150°C

TYPICAL CHARACTERISTICS

Figure 8. Typical Temperature Dependency of $T_{OFF} \cdot V_{LED}$ Constant (Shortest $T_{OFF} \cdot V_{LED} = 5 \ \mu s \cdot V$ and Longest $T_{OFF} \cdot V_{LED} = 50 \ \mu s \cdot V$)

The LED average current in time (DC) is equal to the buck time average current. Therefore, to achieve a given LED current target, it is sufficient to know the buck peak current and the buck current ripple. A rule of thumb is to count a minimum of 50% ripple reduction by means of the capacitor C_{BUCK} and this is normally obtained with a low cost ceramic component ranging from 100 nF to 470 nF (such values are typically used at connector sides anyway, so this is included in a standard BOM). The following figure reports a typical example waveform:



Figure 11. LED Current AC Components Filtered Out by Output Impedance (Oscilloscope Snapshot)

The use of C_{BUCK}

SW Compensation of the Buck Current Accuracy

In order to ensure buck current accuracy as specified in Table 6 – Buck Regulator – Current Regulation, set of constants trimmed during manufacturing process is available. Microcontroller should use them in the following way:

To Reach ±8% (

Calculated trimming constant has to be then written into trimming SPI register: BUCKx_ISENS_TRIM[6:0] = BUCKx_Ry_trim

<u>Note</u>: The BUCKx_ISENS_TRIM[6:0] SPI register allows compensation of the peak current app. in range ±40 % from actual value according to the following equation:

 $\mathsf{IBUCKx} = (\mathsf{ITHRx}_{000} + \delta \mathsf{ITHRx} \cdot \mathsf{BUCKx}_{V} \mathsf{THR}[7:0]) \cdot (1 + 0.4 \cdot ((\mathsf{BUCKx}_{I}\mathsf{SENS}_{TRIM}[6:0] - 63)/63)),$

where:

ITHRx_000 is current for VTHR code 0 in ITHRx range (see Table 6 – Buck Regulator – Current Regulation), δ ITHRx code step in range ITHRx (see Table 6 – Buck Regulator – Current Regulation).

Paralleling the Bucks for Higher Current Capability

Different buck channels can be paralleled at the module output (after the buck inductors) for *higher current capability* on a unique channel, summing up together the individual DC currents.

Buck Overcurrent Protection

Being a current regulator, the NCV78723 buck is by nature preventing overcurrent in all normal situations. However, in order to protect the system from overcurrent even in case of failures, protection mechanism is available.

This protection is based on internal sensing over the buck

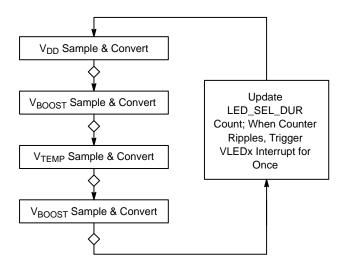


Figure 15. ADC Sample and Conversion Main Sequence

Referring to the figure above, the typical rate for a full SAR plus digital conversion per channel is 8 μ s (Table 6 – ADC for Measuring VBOOST, VDD, VLED1, VLED2, TEMP). For instance, each new VBOOST ADC converted sample occurs at 16 μ s typical rate, whereas for both the VDD and VTEMP channel the sampling rate is typically 32 μ s, that is to say a complete cycle of the depicted sequence. This time is referred to as TADC_SEQ.

If the SPI setting LED_SEL_DUR[8:0] is not zero, then interrupts for the VLEDx measurements are allowed at the points marked with a rhombus, with a minimum cadence corresponding to the number of the elapsed ADC sequences (forced interrupt). In formulas:

 $T_{VLEDx_INT_Forced} = LED_SEL_DUR[8:0] \cdot T_{ADC_SEQ}$ (eq. 4)

In general, prior to the forced interrupt status, the VLEDx_{ON} ADC interrupts are generated when a falling edge on the control line for the buck channel "x" is detected by the device. In case of *digital dimming*, this interrupt start signal corresponds to the LEDCTRLx falling edge together with a controlled phase delay (T VTEMP[7:0] is the value read out directly from the related 8bit-SPI register (please refer to the SPI map). The value is also used internally by the device for the *thermal warning* and *thermal shutdown* functions. More details on these two can be found in the dedicated sections in this document. The value is protected by ODD parity bit.

LED String Voltages ADC: VLEDx, VLEDxON

The voltage at the pins VLEDx (1, 2) is measured. There are 4 ranges available, that can be selected by means of ADC_VLEDx_RNG_SEL[1:0] register, to obtain higher resolution for LED voltage measurement.

Conversion ratios in dependency on selected range are:

0x0: 70/255 (V/dec) = 0.274 (V/dec); 0x1: 50/255 (V/dec) = 0.196 (V/dec); 0x2: 40/255 (V/dec) = 0.157 (V/dec); 0x3: 30/255 (V/dec) = 0.118 (V/dec).

This information, found in registers VLEDxON[7:0] and VLEDx[7:0], can be used by the MCU to infer about the LED string status, for example, individual shorted LEDs. As for the other ADC registers, the values are protected by ODD parity.

Please behavioruasuse573sex74tha-.8s07 93e1.6PpixNI06 29rol38 w46.9103g(19381(NCV 78/21 TTf 299 9 2 10 68.71328 T252 533cm072g

Functional Mode Description Overview

Reset

A synchronous reset is caused either by POR (POR always causes asynchronous reset – transition to reset state) or by falling edge on RSTB pin (in normal/stand-alone mode, when FSO_MD[2:0] = 000 or 001 or 110 or 111).

Init and Normal Mode

Normal mode is entered through Init state after internal delay of 150 μ s. In Init state, OTP refresh is performed. If OTP bits for FSO_MD[2:0] register and *OTP Lock Bit* are programmed, transition to FSO/SA mode is possible.

FSO/Stand-Alone Mode

FSO (Fail-Safe Operation)/Stand-Alone modes can be used for two main purposes:

- Default power-up operation of the chip (Stand-Alone functionality without external microcontroller or preloading of the registers with default content for default operation before microcontroller starts sending SPI commands for chip settings)
- Fail-Safe functionality (chip functionality definition in fail-safe mode when the external microcontroller functionality is not guaranteed)

FSO/stand-alone function is controlled according to Table 8. Entrance into FSO/Stand-alone mode is possible only after customer OTP zapping when *OTP Lock Bit* is set. After FSO mode activation, the FSO bit in status register is set. FSO register is cleared by read register.

When FSO/Stand-Alone mode is activated, content of the following SPI registers is preloaded from OTP memory:

BUCK1_VTHR[7:0], BUCK1_ISENS_THR[1:0], BUCK2_VTHR[7:0], BUCK2_ISENS_THR[1:0], BUCK1_TOFF[4:0], BUCK2_TOFF[4:0], BUCK1_EN, BUCK2_EN, FSO_MD[2:0], BUCK1_TSD_AUT_RCVR_EN, BUCK2_TSD_AUT_RCVR_EN, BUCK2_TSD_AUT_RCVR_EN, BUCK2_OC_OCCMP_THR[1:0]]. BUCKx_ISENS_TRIM[6:0] register is preloaded from corresponding BUCKx_ISENS_RNG[6:0] register.

In FSO (entered via falling edge on RSTB pin) and Stand-Alone modes, **BUCK1_EN & BUCK2_EN** are controlled from SPI register map (SPI registers are updated from OTP's after entrance into these modes).

BUCK1_EN and BUCK2_EN are supposed to be set '1' for the BUCKx operation in the FSO/stand-alone mode.

When control registers are pre-loaded from OTP's after POR and FSO mode is not entered (valid for FSO_MD[2:0] = 100 or 101), BUCK1_EN and BUCK2_EN are kept inactive ('0') until the first valid SPI operation is finished to avoid potential activation of buck regulators immediately after POR (to prevent undefined state of LEDCTRLx pins in case MCU leaves POR later than NCV78723).

In FSO and Stand-Alone modes, the logic level at **LEDCTRL**x pins is ignored and digital PWM dimming with LEDCTRLx pins is not available. The outputs can be dimmed only by means of BUCKx_EN register.

A falling edge on RSTB pin may trigger either entrance into FSO mode or reset in dependency on FSO_MD[2:0] register value. Please refer to Table 8 and Figure 18 for more details.

Once FSO mode is entered via falling edge on RSTB pin, reset function of RSTB pin is blocked until FSO mode is exited. FSO mode can be exited by the rising edge on RSTB pin or by writing FSO_MD[2:0] = 000 or 001 (possible only in FSO modes, where SPI control register update is allowed: FSO_MD[2:0] = 011 or 101).

In stand-alone mode (FSO_MD[2:0] = 110 or 111), RSTB has always reset functionality.

During entrance into FSO mode, value of FSO_MD[2:0] SPI register (preloaded from OTP at power-up only) is latched into internal register and all FSO related functions are then controlled according to it. Purpose is to avoid the reset of the device when FSO mode is active and FSO_MD[2:0] is changed to value corresponding to stand-alone mode, where RSTB pin has reset functionality. The internal register is cleared after POR or when FSO mode is exited.

the 16-bit command frame on the data input line transmitted by the Master, shifting via the chips' shift registers through the daisy chain. The chips interpret the command once the chip select line rises.

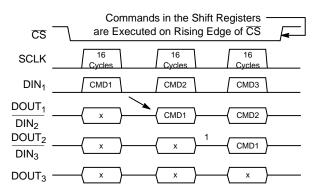


Figure 21. SPI Daisy Chain Data Shift between Slaves. The Symbol 'x' Represents the Previous Content of the SPI Shift Register Buffer

SPI ADDRESS MAP

Table 9. NCV78723 SPI ADDRESS MAP

		0120 01 11									
ADDR	R/W	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x00	NA				NOP Register (Read/Write Operation Ignored)						
0x01	R/W	BUCK1_ISEI	NS_THR[1:0]		BUCK1_VTHR[7:0]						
0x02	R/W	BUCK2_ISEI	NS_THR[1:0]		BUCK2_VTHR[7:0]						
0x03	R/W		В	UCK1_TOFF[4:0	0]			В	UCK2_TOFF[4:	0]	
0x04	R/W	BUCK1_OFF_ CMP_DIS (Note 31)	BUCK2_OFF_ CMP_DIS (Note 31)	DRV_ SLOW_EN (Note 31)	LOW_EN THR[1:0]				BUCK1_EN	BUCK2_EN	
0x05	R/W	BUCK1_ TSD_AUT_ RCVR_EN	BUCK2_ TSD_AUT_ RCVR_EN				THERMAL_WAR	NING_THR[7:0]		·	
0x06	R/W	VTEMP_ OFF_COMP ODD PAR (Note 30)				LE	D_SEL_DUR[8:	0]			
0x07	R/W	VTEMP_C	OFF_COMP[2:0]	(Note 30)			BUC	(1_ISENS_TRIN	/[6:0]		
0x08	R/W	VTEMP_C	OFF_COMP[5:3]	(Note 30)			BUCK	(2_ISENS_TRIN	/[6:0]		
0x09	R/W	ADC_VLE SEL	D1_RNG_ [1:0]	ADC_VLE SEL		OTP_BIAS_H	OTP_BIAS_L	OTP_A	DDR[1:0]	OTP_OPER	RATION[1:0]
0x0A	R	0x0	ODD PARITY				VLED10	ON[7:0]			
0x0B	R	0x0	ODD PARITY		VLED2ON[7:0]						
0x0C	R	0x0	ODD PARITY	VLED1[7:0]							
0x0D	R	0x0	ODD PARITY	VLED2[7:0]							
0x0E	R	0x0	ODD PARITY	VTEMP[7:0]							
0x0F	R	0x0	ODD PARITY		VBOOST[7:0]						
0x10	R	0x0	ODD PARITY				VDD	[7:0]			
0x11	R	0x0	ODD PARITY				BUCK1_TO	N_DUR[7:0]			
0x12	R	0x0	ODD PARITY				BUCK2_TO	N_DUR[7:0]			
0x13	R	0x0	ODD PARITY	0>	« 0	OPENLED1	SHORTLED1	OCLED1	OPENLED2	SHORTLED2	OCLED2
0x14	R	0x0	ODD PARITY	OTP_FAIL	FSO	HWR	LED1VAL	LED2VAL	SPIERR	TSD	TW
0x15	R	0x0	ODD PARITY		0x0		OTP_ ACTIVE	BUCK1_ MIN_TON	BUCK2_ MIN_TON	BUCK1_ STATUS	BUCK2_ STATUS
0x16	R	0x0	ODD PARITY	0x0			BUCI	K1_ISENS_RNG	6:0]		
0x17	R	0x0	ODD PARITY	0x0			BUCI	K2_ISENS_RNG	6:0]		
0x18	R	0x0	ODD PARITY		BUCK2_ISE	NS_D1[3:0]			BUCK1_ISE	ENS_D1[3:0]	
0x19	R	0x0	ODD PARITY	BUCK2_ISENS_D2[3:0] BUCK1_ISENS_D2[3:0]							
0x1A	R	0x0	ODD PARITY		BUCK2_ISE	NS_D3[3:0]			BUCK1_ISE	ENS_D3[3:0]	
0x1B	R	0x0	ODD PARITY	BUCK_ISENS_TC1[3:0] BUCK_ISENS_TC0[3:0]							
0x1C	R	0x0	ODD PARITY		BUCK_ISEN	IS_TC3[3:0]			BUCK_ISEI	NS_TC2[3:0]	
0x1D	R	0x0	ODD PARITY				0x0				TC_VERSIO
0x1E	R					OTP_D	ATA[9:0]				
0x1F	R	0)	(0				REVI	D[7:0]			
OTHER	R					0)	(0				

30. Read Only. 31. Available only on N78723–2 device.

Table 10. BIT DEFINITION

Symbol	MAP Position	Description			
REGISTER 0X00 (CR): NOP REGISTER, RESET VALUE (POR) = 00000000002					
NOP	Bits [9:0] – ADDR_0x00	NOP Register (Read/Write Operation Ignored)			
REGISTER 0X01 (CR): BUCK 1 PE	AK CURRENT SETTINGS, RE	ESET VALUE (POR) = 00000000002			
BUCK1_ISENS_THR[1:0]	Bits [9:8] – ADDR_0x01	Peak Current: Selection of the Range 1, 2, 3 or 4			
BUCK1_VTHR[7:0]	Bits [7:0] – ADDR_0x01	Peak Current Comparator Threshold Value			
REGISTER 0X02 (CR): BUCK 2 PE	AK CURRENT SETTINGS, RE	ESET VALUE (POR) = 00000000002			
BUCK2_ISENS_THR[1:0]	Bits [9:8] – ADDR_0x02	Peak Current: Selection of the Range 1, 2, 3 or 4			
BUCK2_VTHR[7:0]	Bits [7:0] – ADDR_0x02	Peak Current Comparator Threshold Value			
REGISTER 0X03 (CR): BUCK 1 AN	ID 2 TOFF SETTINGS, RESET	VALUE (POR) = 00000000002			
BUCK1_TOFF[4:0]	Bits [9:5] – ADDR_0x03	Buck 1 TOFF-VLED Constant Settings			
BUCK2_TOFF[4:0]	Bits [4:0] – ADDR_0x03	Buck 2 TOFF-VLED Constant Settings			
REGISTER 0X04 (CR): BUCK SET	TINGS, RESET VALUE (POR)	= 000000000 ₂			
BUCK1_OFF_CMP_DIS	Bit 9 – ADDR_0x04	Buck 1 Offset Cancellation Disable			
BUCK2_OFF_CMP_DIS	Bit 8 – ADDR_0x04	Buck 2 Offset Cancellation Disable			
DRV_SLOW_EN	Bit 7 – ADDR_0x04	Slow Driver Slope Enable			
BUCKx_OC_OCCMP_THR[1:0]	Bits [6:5] – ADDR_0x04	Overcurrent Detection Settings			
FSO_MD[2:0]	Bits [4:2] – ADDR_0x04	FSO Mode Selection			
BUCK1_EN	Bit 1 – ADDR_0x04	Buck Regulator Channel 1 Enable Bit			
BUCK2_EN	Bit 0 – ADDR_0x04	Buck Regulator Channel 2 Enable Bit			

REGISTER 0X05 (CR): BUCK SETTINGS, RESET VALUE (POR) = 0010110011

Symbol	MAP Position	Description
REGISTER 0X16: BUCK TRIM	MING, RESET VALUE (POR) = 0	(0XXXXXX ₂
ODD PARITY	Bit 8 – ADDR_0x16	Odd Parity over Data
BUCK1_ISENS_RNG[6:0]	Bits [6:0] – ADDR_0x16	Trimming Constant for Highest Range on Hot for Buck 1 Peak Current
REGISTER 0X17: BUCK TRIMM	MING, RESET VALUE (POR) = 0>	X0XXXXXX ₂
ODD PARITY	Bit 8 – ADDR_0x17	Odd Parity over Data
BUCK2_ISENS_RNG[6:0]	Bits [6:0] – ADDR_0x17	Trimming Constant for Highest Range on Hot for Buck 2 Peak Current
REGISTER 0X18: BUCK TRIM	MING, RESET VALUE (POR) = 0	XXXXXXXX ₂
ODD PARITY	Bit 8 – ADDR_0x18	Odd Parity over Data
BUCK2_ISENS_D1[3:0]	Bits [7:4] – ADDR_0x18	Delta Trimming Constant for Buck 2 Peak Current
BUCK1_ISENS_D1[3:0]	Bits [3:0] – ADDR_0x18	Delta Trimming Constant for Buck 1 Peak Current
REGISTER 0X19: BUCK TRIMM	MING, RESET VALUE (POR) = 0>	XXXXXXXX ₂
ODD PARITY	Bit 8 – ADDR_0x19	Odd Parity over Data
BUCK2_ISENS_D2[3:0]	Bits [7:4] – ADDR_0x19	Delta Trimming Constant for Buck 2 Peak Current
BUCK1_ISENS_D2[3:0]	Bits [3:0] – ADDR_0x19	Delta Trimming Constant for Buck 1 Peak Current
REGISTER 0X1A: BUCK TRIMI	MING, RESET VALUE (POR) = 02	XXXXXXXX ₂
ODD PARITY	Bit 8 – ADDR_0x1A	Odd Parity over Data
BUCK2_ISENS_D3[3:0]	Bits [7:4] – ADDR_0x1A	Delta Trimming Constant for Buck 2 Peak Current
BUCK1_ISENS_D3[3:0]	Bits [3:0] – ADDR_0x1A	Delta Trimming Constant for Buck 1 Peak Current
REGISTER 0X1B: BUCK TRIMI	MING, RESET VALUE (POR) = 0	XXXXXXXX ₂
ODD PARITY	Bit 8 – ADDR_0x1B	Odd Parity over Data
BUCK_ISENS_TC1[3:0]	Bits [7:4] – ADDR_0x1B	-

Table 10. BIT DEFINITION (continued)

Table 12. ORDERING INFORMATION

Device**	Marking	Package*	Shipping [†]
NCV78723MW0CR2G	N78723-0	QFN24 5 \times 5 with Wettable Flank (Pb-Free)	5,000 / Tape & Reel
NCV78723MW0R2G	N78723-0	QFN24 5 \times 5 with Wettable Flank (Pb-Free)	5,000 / Tape & Reel
NCV78723MW2R2G	N78723-2	QFNW24 5 × 5 with Step-cut Wettable Flank (Pb-Free)	5,000 / Tape & Reel
NCV78723MW2AR2G***	N78723–2	QFNW24 5 × 5 with Step-cut Wettable Flank (Pb-Free)	5,000 / Tape & Reel

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 *** NCV78723MW2 & NCV78723MW0 have different package mold compound. Please contact onsemi for technical details.
 *For additional information on our Pb-Free strategy and soldering details, please download the onsemi Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.
 **** NCV78723MW2AR2G is recommended for new designs.

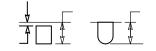
QFNW24 5x5, 0.65P

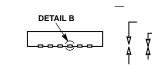


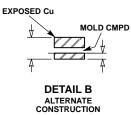


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L1 --- 0.15





XXXXX = Specific Device Code

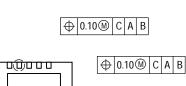
- A = Assembly Location
- WL = Wafer Lot
- YY = Year
- WW = Work Week
- = Pb–Free Package

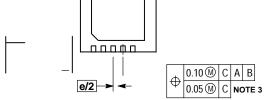
(Note: Microdot may be in either location)

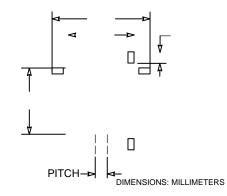
*This information is generic. Please refer to device data sheet for actual part marking.

Pb-Free indicator, "G" or microdot "•", may or may not be present.









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