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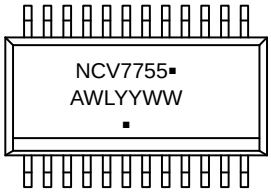
The NCV7755 is an automotive grade integrated driver with eight high−side switches. The device provides drive capability up to 700 mA per channel and is protected for overload and overtemperature conditions. All the channels have integrated output clamps for switching inductive loads, multiple start pulses for bulbs, and can be mapped to two internal PWM generators for LED loads. The output control and diagnostic reporting is via SPI. Additionally, INx pins can be mapped to any of the outputs for direct control.

A dedicated limp−home mode enables operational control of two high−side drivers via logic input pins.

The NCV7755 is available in a SSOP−24 exposed pad package for optimal thermal performance.



NCV7755 = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

NCV7755DQR2G	SSOP24−EP (Pb−Free)	2500 Units/Rail

- 8 High−Side Channels
  - For Relays (Flyback Clamps)
  - Bulbs (Multiple Pulse in−rush Scheme)
  - LEDs (Internal PWM Generator)
  - 2.3 A Peak Current (Max)
  - $R_{DS(on)}$ 0.9 Ω (Typ), 1.8 Ω (Max)
  - Paralleling of Two Output Pair is Allowed
- SPI Control (16 Bit)
  - Frame Error Detection (16 Bits + 8*n Bits)
  - Daisy Chain Capable
- Two Input Pins with Mapping for PWM Operation
- Low Quiescent Current in Sleep Mode
- Limp Home Mode with Auto−retry
- Supports Cranking Voltage of 3 V Minimum on VS
- 3.3 V & 5 V Compatible Digital Input Supply Range
- Fault Reporting
  - Openload (OFF or ON)
  - Overload
  - Overtemperature
  - Power Supply Fail (VS, VDD Undervoltage)
  - Output Short to GND and Battery
- Reverse Polarity Protection
- Loss of Ground Protection
- Power−on Reset (VDD)
- SSOP−24 with an Exposed Pad
- NCV Prefix for Automotive
  - Site and Change Control
  - AEC−Q100 Qualified

- Automotive Body Control Unit
- Automotive Engine Control Unit
- Relay Drive
- Bulb Drive
- LED Drive

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Publication Order Number:

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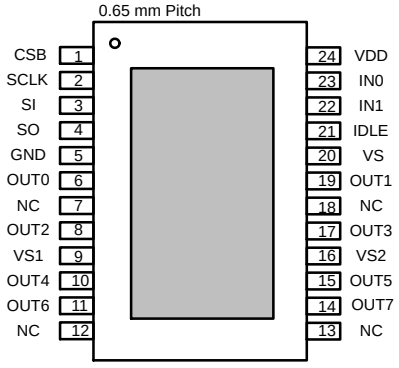
1	CSB	SPI Chip Select “Bar” (120 kΩ pull−up resistor to VDD)
2	SCLK	SPI Clock (120 kΩ pull−down resistor)
3	SI	SPI Serial Data Input (120 kΩ pull−down resistor)
4	SO	SPI Serial Data Output. Tri−state when CSB is high
5	GND	Ground
6	OUT0	High−side driver output. Requires an external pull−down component for operation
7	NC	No connection. Internally not bonded
8	OUT2	High−side driver output. Requires an external pull−down component for operation
9	VS1	Power supply input for High−side drivers channels 0, 2, 4, and 6
10	OUT4	High−side driver output. Requires an external pull−down component for operation
11	OUT6	High−side driver output. Requires an external pull−down component for operation
12	NC	No connection. Internally not bonded
13	NC	No connection. Internally not bonded
14	OUT7	High−side driver output. Requires an external pull−down component for operation
15	OUT5	High−side driver output. Requires an external pull−down component for operation
16	VS2	Power supply input for High−side drivers channels 1, 3, 5, and 7
17	OUT3	High−side driver output. Requires an external pull−down component for operation
18	NC	No connection. Internally not bonded
19	OUT1	High−side driver output. Requires an external pull−down component for operation
20	VS	Power supply input for output power switches gate control
21	IDLE	High activates low Iq Idle mode (120 kΩ pull−down resistor) Low with IN0 = IN1 = low puts device in sleep mode. Low puts all SPI registers in reset Low with INx = high puts device in limp home mode
22	IN1*	Input pin 1. Controls channel 3 (default) and in Limp Home Mode (with IDLE = low). Outputs can be mapped to this pin. (120 kΩ pull−down resistor)
23	IN0*	Input pin 0. Controls channel 2 (default) and in Limp Home Mode (with IDLE = low). Outputs can be mapped to this pin. (120 kΩ pull−down resistor)
24	VDD	Digital power supply input for SPI and support interface to VS
EPAD	Exposed Pad	Connect to GND for best thermal performance or leave unconnected. Internally, the EPAD is isolated from the GND signal

*Ground if not used for best EMI performance.
Alternatively keep open and internal pull−down will hold the input low through a 120 kΩ pull down resistor.

Battery supply input voltage (VS) DC Positive Transient input supply voltage (Note 1)	 VsMax VsacMax	 −0.3 –	 36 42	 V V
Battery supply input voltage (VS1, VS2) DC input supply voltage with short circuit Positive Transient input supply voltage (Note 1)	 VsdcscMax VsxacMax	 0 –	 36 42	 V V
Logic Supply Input Voltage (VDD) DC	 VddMax	 −0.3	 5.5	 V
Output Voltage (OUTx)	VoutMax	−25	VSx+0.3	V
Output Current (OUTx) Specified is the maximum overload detection threshold.	 IoutMax	 –	 2.3	 A
Digital I/O pin voltage (IDLE, IN0, IN1, CSB, SCLK, SI,) (SO)	 VioMax ViosoMax	 −0.3 −0.3	 5.5 VDD+0.3V	 V V
Digital I/O input current (IDLE, IN0, IN1, CSB, SCLK, SI, SO)	 IioMax	 −10.0	 2.0	 mA
Clamping Energy Maximum (single pulse) (Tj = 25°C, Iout = 440 mA) (Tj = 150°C, Iout = 400 mA) Repetitive (multiple pulse)	 VclpDc25Max VclpDc150Max VclpAcMax	 – – –	 50 25 Note 2	 mJ mJ mJ
Operating Junction Temperature Range	Tj	−40	150	°C
Storage Temperature Range	Tstr	−65	150	°C
ESD Capability (AEC−Q100−002, AEC−Q100−011) Human body model (100 pF, 1.5 kΩ) (VSx, OUTx pins) Human body model (100 pF, 1.5 kΩ) (all other pins) Charged Device Model (corner pins) Charged Device Model (all other pins)	 Vesd4k Vesd2k Vesd750 Vesd500	 −4000 −2000 −750 −500	 4000 2000 750 500	 V V V V
AECQ10x−12 Short Circuit Reliability Characterization	 AECQ10x	 Grade A	 –	

1. Ton = 400 ms; ton/toff = 10%, 100 pulse limit.
2. 2 M pulses (triangular), VS = 15 V, 63 Ω, 390 mH, T_A = 25°C.



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Moisture Sensitivity Level	MSL	2		––
Lead Temperature Soldering: SMD style only, Reflow (Note 3) Lead – Free Part 60 – 150 sec above 217°C, 40 sec max at peak	Treflow		265 peak	°C
Package Thermal Resistance and Characterization Parameter SSOP−24 EPAD Junction−to−Ambient (Note 4) Junction−to−pin (exposed pad)	 $R_{\theta JA}$ Ψ_{JB}	 	 35.1 24.3	 °C/W °C/W

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

3. For additional information, see or download ’s Soldering and Mounting Techniques Reference Manual, SOLDERRM/D and Application Note AND8083/D.
4. Per JEDEC JESD51−7 at natural convection on FR4 2s2p board (76.2 mm x 114.3 mm x 1.5 mm) with 2 inner copper layers.

Digital Supply Input Voltage (VDD)	VDDRec	3.00	5.5	V
Battery Supply Input Voltage (VS, VS1, VS2)	VSRec	7.0*	18**	V
DC Output Current (OUTx), (T_A = 85°C, all channels)	IoutRec	–––	330	mA
Junction Temperature	T_J	−40	150	°C

*Extended operation down to 3 V with possible parameter shift. **Extended operation up to 28 V with possible parameter shift.

(−40°C < T_J < 150°C, 3.0 V < VDD < 5.5 V, 7 V < VS = VS1 = VS2 < 18 V,
IDLE = high unless otherwise specified)

Operating Current (VS) Active Mode	Set to Active Mode via SPI HWCR.ACT (bit 7) = 1 IDLE = CSB = VDD SCLK=0V No Open Circuit Diag Current					
Channels Off	7 V < VS < 18 V, IN0 = IN1 = 0	VSactOFF1	–	–	7.7	mA
	VS < VDD−1 V, IN0 = IN1 = 0	VSactOFF2	–	–	5.0	mA
Channels On	7 V < VS < 18 V, IN0 = IN1 = VDD	VSactON1	–	–	8.7	mA
	VS < VDD−1 V, IN0 = IN1 = VDD	VSactON2	–	2.3	5.0	mA
Operating Current (VS) Idle Mode	IDLE = CSB = VDD IN0 = IN1 = SCLK = 0 V All Channels Off					
	7 V < VS < 18 V	VSidl1	–	–	2.2	mA
	VS < VDD−1 V	VSidl2	–	–	0.3	mA
Operating Current (VS) Sleep Mode	CSB = VDD IDLE = IN0 = IN1 = 0 V					
	T_J = 85ºC	VSslp85	–	0.1	3	μA
	T_J = 150ºC	VSslp150	–	0.1	20	μA

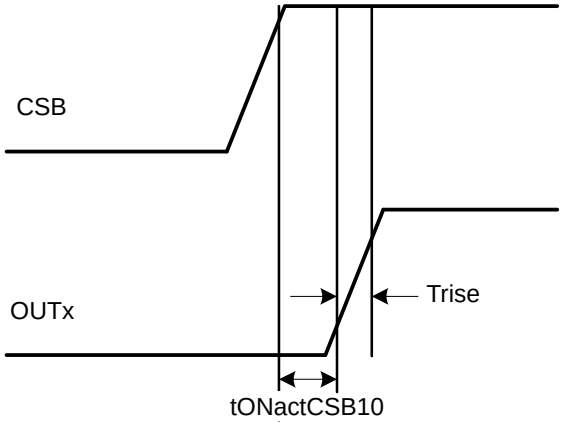
(–40°C < T_J < 150°C, 3.0 V < VDD < 5.5 V, 7 V < VS = VS1 = VS2 < 18 V, IDLE = high unless otherwise specified)

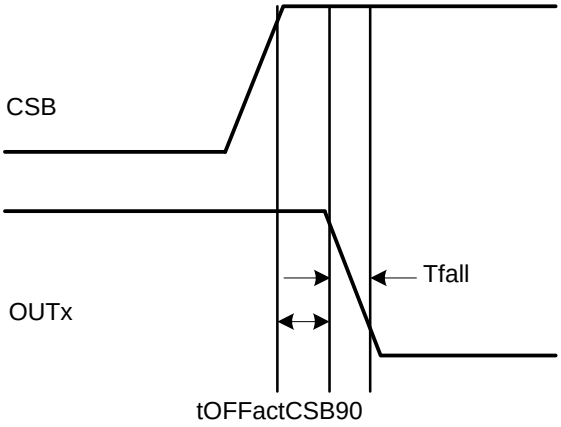
Operating Current (VDD) Active Mode	Set to Active Mode via SPI HWCR.ACT (bit 7) = 1 IDLE = CSB = VDD SCLK = 0 V No Open Circuit DIAG current					
Channels Off	7 V < VS < 18 V, IN0 = IN1 = 0	VDDactOFF1	–	–	0.3	mA
	VS < VDD−1 V, IN0 = IN1 = 0	VDDactOFF2	–	–	2.7	mA
Channels On	7 V < VS <18 V, IN0 = IN1 = VDD	VDDactON1	–	–	0.3	mA
	VS < VDD−1 V, IN0 = IN1 = VDD	VDDactON2	–	–	3.5	mA
Operating Current (VDD) Idle Mode	IDLE = CSB = VDD, IN0 = IN1 = SCLK = 0 V All Channels Off					
	7 V < VS < 18 V	VDDidl1	–	–	0.3	mA
	VS < VDD−1 V	VDDidl2	–	–	2.2	mA
Operating Current (VDD) Sleep Mode	CSB = VDD IDLE = IN0 = IN1 = 0 V T_J					

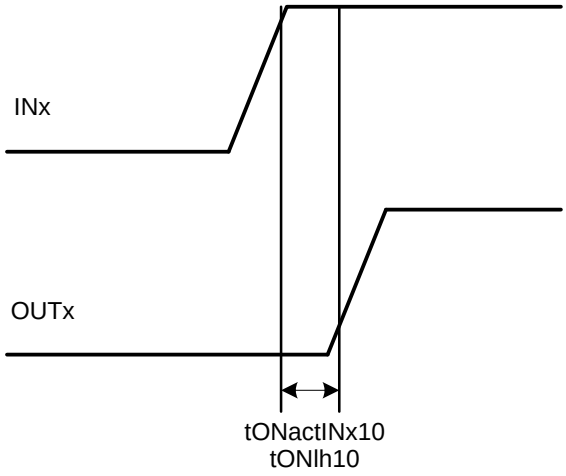
(–40°C < T_J < 150°C, 3.0 V < VDD < 5.5 V, 7 V < VS = VS1 = VS2 < 18 V, IDLE = high unless otherwise specified)

Active to Idle Delay	INx going low to MODE = 11_B	Act2idlINx
	From CSB going high To MODE = 11_B	Act2idlCSB

(−40°C < T_J < 150°


CSB
OUTx
Trise
tONactCSB10


CSB
OUTx
Tfall
tOFFactCSB90


INx
OUTx
tONactINx10
tONlh10

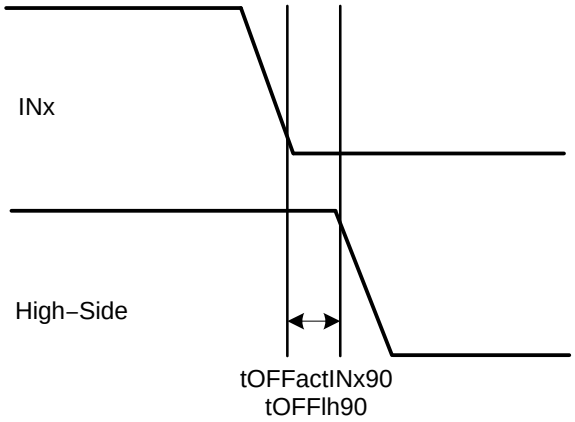
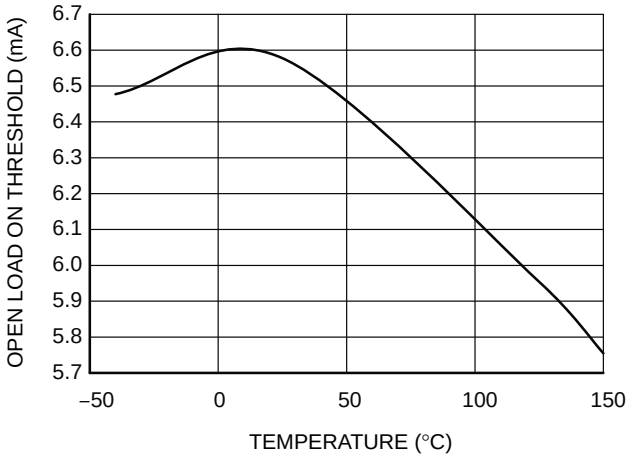
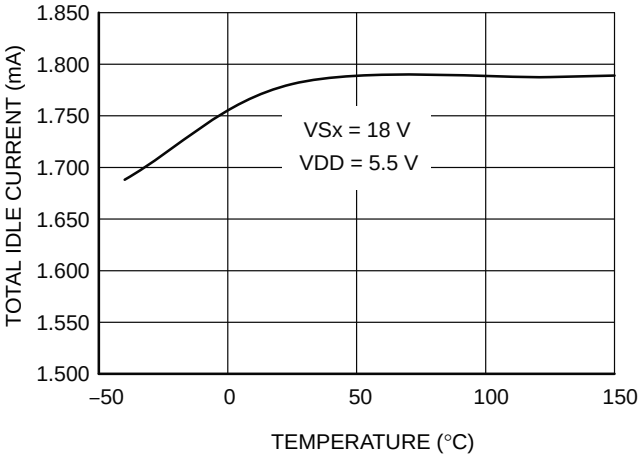
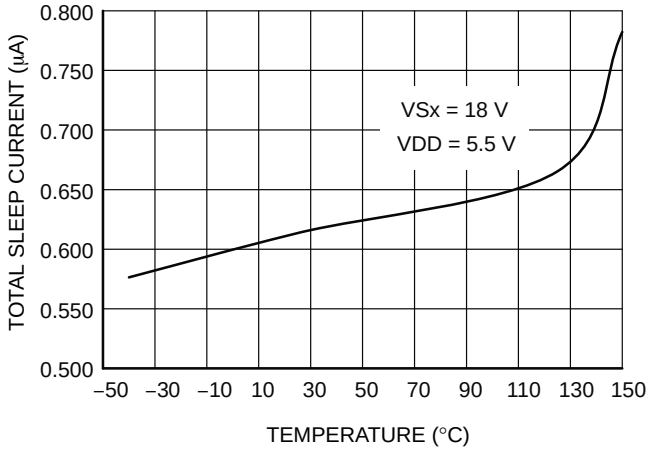
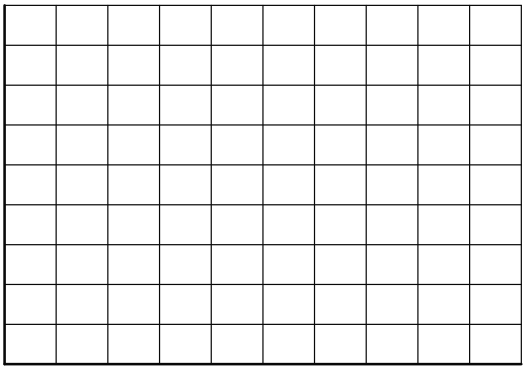

INx
High−Side
tOFFactINx90
tOFFlh90

Figure 8. Serial Peripheral Interface Detailed Timing


OPEN LOAD ON THRESHOLD (mA)
6.7
6.6
6.5
6.4
6.3
6.2
6.1
6.0
5.9
5.8
5.7
−50
0
50
100
150
TEMPERATURE (°C)


TOTAL IDLE CURRENT (mA)
1.850
1.800
1.750
1.700
1.650
1.600
1.550
1.500
VSx = 18 V
VDD = 5.5 V
−50
0
50
100
150
TEMPERATURE (°C)


TOTAL SLEEP CURRENT (µA)
0.800
0.750
0.700
0.650
0.600
0.550
0.500
VSx = 18 V
VDD = 5.5 V
−50
−30
−10
10
30
50
70
90
110
130
150
TEMPERATURE (°C)



The NCV7755 is comprised of eight DMOS high−side power drivers. There are two connection pins (VS1, VS2) for the drain of each output driver with 4 common drivers per pin. Communication to the device is through a 16−bit SPI port for output control, programming, and fault reporting. The device also features a limp home mode with an IDLE control pin for limp home entry and two input control pins (IN0 & IN1) for output engagement.

Output loads can be varied from inductive loads, bulb loads, or LED loads. Special features for each load type include output clamps, in−rush design considerations, and two on−chip PWM generators.

The NCV7755 allows independent mapping of the INx pins to the outputs and independent mapping of the two PWM generators to the outputs.

The device is capable of running down to VS = 3 V for automotive cranking events.

There are four power supply input requirements. The descriptions of their internal connections are listed below.

- VS − Analog Supply Input – Battery input for all internal analog circuitry. The maximum current drain is 8.7 mA over temperature
- VS1 – Output Driver Drain connection for OUT0, OUT2, OUT4, OUT6. The maximum current is internally limited by the maximum overload detection threshold of 2.3 A (each channel)
- VS2 − Output Driver Drain connection for OUT1, OUT3, OUT5, OUT7. The maximum current is internally limited by the maximum overload detection threshold of 2.3 A (each channel)
- VDD – Digital Supply Input – Internal logic supply input. Runs from 3.3 V input or 5 V input. The maximum current drain is 3.5 mA over temperature

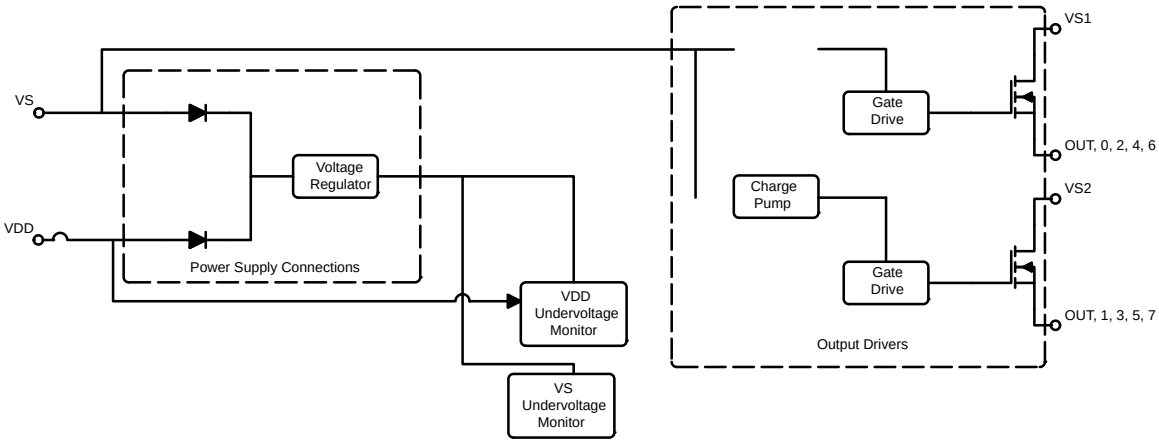
It's important to note the maximum combined current drain of both VS and VDD is specified at 9 mA with the channels on.

Sleep mode current for VS is 3 μA at 85°C and the maximum combination of VS+VDD is 5 μA at 85°C.

The exposed pad connection should be connected to ground with as large a pc board metal connection as possible for best thermal performance and EMC considerations. However this is not a ground connection for IC ground currents.

Load Dump– During a peak transient event such as automotive load dump the outputs maintain their operation up to the maximum rating for Positive Transient input supply voltage of 42 V as programmed via SPI or the input control pins IN0 and IN1.

Cranking Conditions– Automotive cranking conditions can cause the battery (aka VS) to dip to low levels. In order to maintain circuit operation down to the lowest possible levels the battery connection is OR'd with the logic supply voltage (VDD). Diodes D1 and D2 provide the OR'd condition into the voltage regulator. The reduction or removal of current into D1 from VS will cause the current into D2 from VDD to increase to keep the voltage regulator alive. Additional current can also come from SO.



Power−Up/Power−Down Control

VDD and VS each has their own Power−On reset monitors which serve to hold off proper operation until sufficient voltage is present to control the output device. The device powers up with sufficient voltage on either or both VDD or VS, and INx or IDLE pin are high. The Standard Diagnostic Register initially reports both VS Undervoltage (Monitor) and VDD Lower Operating Range (Monitor).

SPI communication is present with sufficient voltage on VDD. An undervoltage on VDD resets all the registers to their default values and no SPI communication is available, although memory of Overload / Overtemperature conditions is maintained in ERR of the Standard Diagnostics Register and can be retrieved when VDD is present. If VS is present with VDD undervoltage, Limp Home mode control is possible.

Sufficient voltage on VS allows for output turn−on. During cranking conditions as VS dips, the diode OR'd circuit described in the previous section allows for the IC to maintain current into the logic solely from VDD. All channels which are on keep their state during cranking unless commanded to turn off. Channel turn−on may not be possible during cranking.

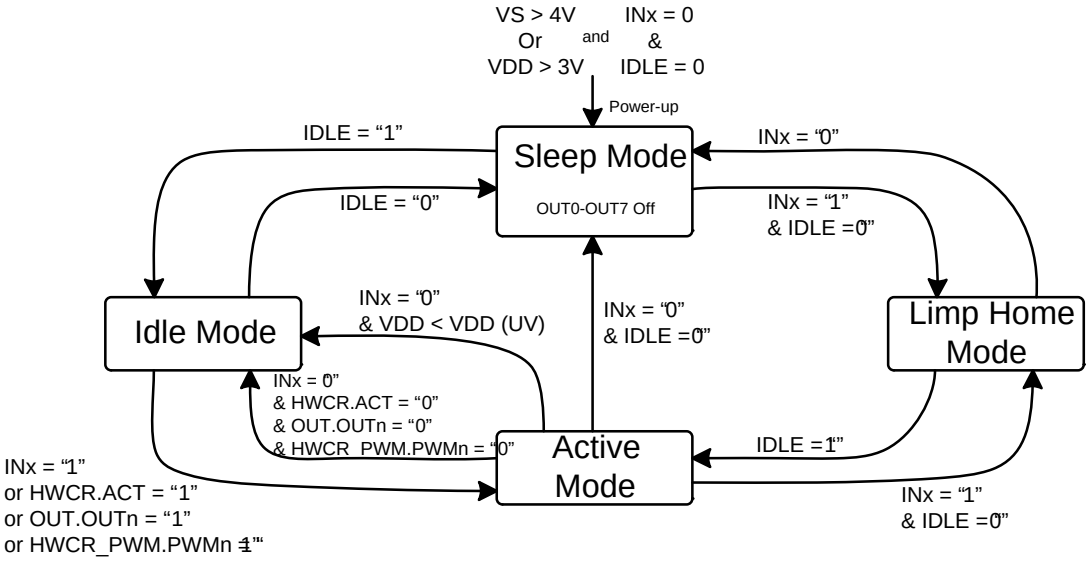
VDD Low Operation Voltage − VDD is monitored and its status is reported in the Diagnostic Register as bit 13 (LOPVDD). The default value is set to a "1" during power up and is continuously monitored for the electrical parameter VDD Lower Operating Voltage (between 3.0 V and 4.5 V). Because of this threshold, operation for VDD with a 3.3 V supply will continuously report a "1" in this register. The LOPVDD bit can only be reset by reading the Standard Diagnostic Register.

OUT	Output is off
BIM	Output latches off with overload
MAPIN0	IN0 is mapped to OUT2
MAPIN1	IN1 is mapped to OUT3
INST	Previous transmission failed. Input pins are set low
DIAG_IOL	Diagnostic current is not enabled
DIAG_OSM	Voutx is less than the Output Monitor Threshold
DIAG_OLON	Normal operation
DIAG_OLONEN	Open Load ON not active
HWCR	Normal operation, no reset command, no parallel combinations
HWCR_OCL	Normal operation, no latch clear
HWCR_PWM	

	(Note 15)	(Note 16)	(Note 17)
(Note 12)	Channels – Cannot be controlled	Channels – Cannot be controlled	Channels – Cannot be controlled
	SPI registers – Reset	SPI registers – Available	SPI registers – Available
	SPI communication – Not available	SPI communication – Possible (fsclk = 1 MHz)	SPI communication – Possible (fsclk = 5 MHz)
	Limp Home Mode – Not available	Limp Home Mode – Available (channels are off)	Limp Home Mode – Available (channels are off)
(Note 13)	Channels – Cannot be controlled by SPI	Channels – Can be controlled by SPI (Rdson deviations possible).	Channels – Can be controlled by SPI

There are 4 modes of operation. Each is presented in the state diagram below.

1. Sleep Mode
2. Idle Mode
3. Active Mode
4. Limp Home Mode



	Channels	Channels not available no SPI communication SPI Register Reset	Channels not available no SPI communication SPI Register Reset		
	SPI Communication				
	SPI Registers				
	Channels		x		x
	SPI Communication			x	
	SPI Registers			reset	
	Channels		x	(INx pins only)	
	SPI Communication			x	
	SPI Registers			reset	
	Channels		x	(INx pins only)	(INx pins only)
	SPI Communication		(read only)	x	(read only)
	SPI Registers		(read only)	reset	(read only)

–

The power−up condition for the NCV7755 is an OR'd condition between the VS battery input and the VDD logic input. Either of the supplies exceeding their minimum operative voltage (4.0 V max for VS) or (3.0 V for VDD) will initiate the internal power−on sequence. In addition to these

Only Channel 2 and 3 are controlled (via IN0 and IN1) during Limp Home Mode. Limp Home mode requires only VS and VSx for driver turn−on. VDD is not required. The device enters Limp Home Mode when the IDLE pin is low and IN0 and/or IN1 are high. When IN0 is high, channel 2 turns on. When IN1 is high, channel 3 turns on. These two input control pins and corresponding channels are also active after a power up condition.

SPI communication is active (with VDD>VDDUVLO) in read−only mode only and reports Overload and Overtemperature faults, and will also continue to monitor for Output Status Monitor conditions (on all channels), but Open Load Diagnostic Current is inactive (on all channels).

When entering Limp Home Mode, the Undervoltage Monitor (UVRVS) and Lower Operating Range Monitor (LOPVDD) bits are set to 1_B while the Open Load ON (OLON) State and Open Load OFF (OLOFF) State are set to 0_B. The Transmission Error bit (TER) is set to “1” for the first SPI command which is sent back with the INST register returned with the first SPI command, and will act normally afterwards.

The NCV7755 incorporates an auto−retry function for highly capacitive loads in Limp Home Mode. In normal operation (Active Mode), the device can compensate for capacitive loads (in case of Overload, Short Circuit or Overtemperature) with the external microprocessor drive control time, but when in Limp Home Mode this is not possible. Attempted tries to turn on an output with a constant input high control when exposed to Overload (Ilovl0), Short Circuit or Overtemperature will occur with the following characteristics.

- 10 ms (8 retries)
- 20 ms (8 retries)
- 40 ms (8 retries)
- 80 ms (continuously)

It is important to note the 8 counts do not include the initial turn−on attempt of the device.

A reset to the initial 8 retries at 10 ms can be realized with a low on the input of 2 times the Internal Frequency Synchronization Time (typically 2 x 5 μs).

The 8 outputs can be controlled via 4 ways which are listed below.

1. Output Control via SPI. Commands to turn a device on are input through the SPI interface.
2. Output Control via IN0 and/or IN1. To activate this, a SPI command must be sent to map the control to either IN0 (MAPIN0) or IN1 (MAPIN1). By default, mapping of IN0 and IN1 are set to OUT2 (IN0) and OUT3 (IN1) after power−up.
3. Limp Home Mode – A low on IDLE will allow control of OUT2 (IN0) and OUT3 (IN1).

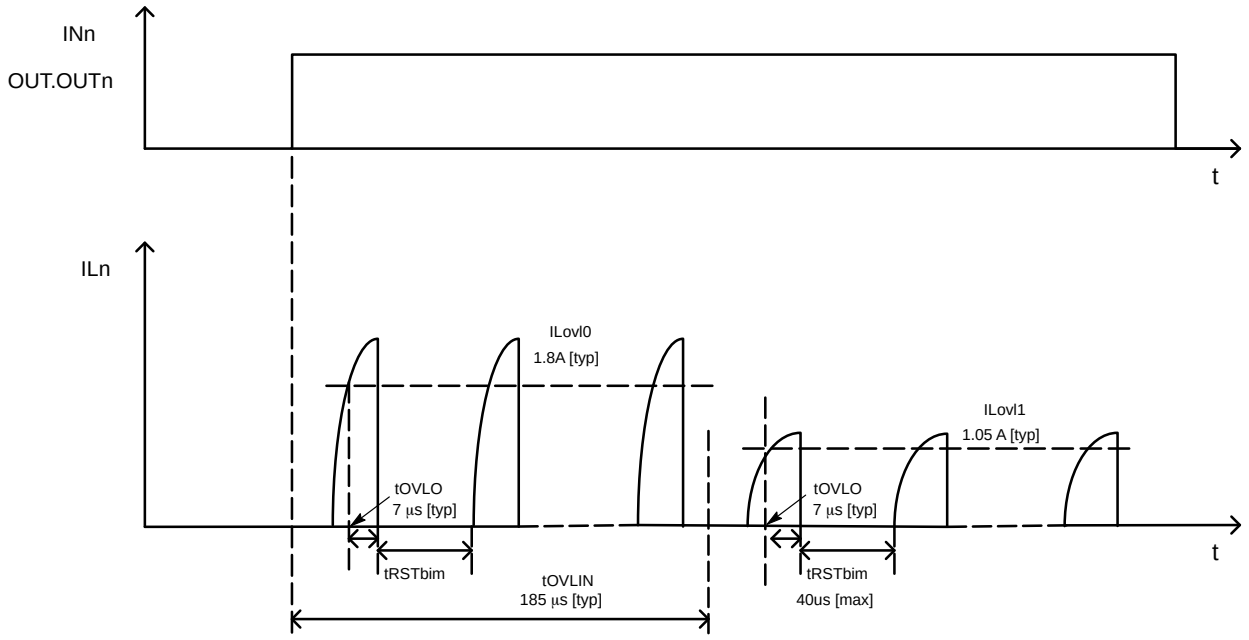
The 8 outputs of the NCV7755 are designed to work with multiple types of loads and with the capability of paralleling two paired channels.

Resistive loads are primarily concerned with output current, switching delays, and slew rates. The NCV7755 has two overload thresholds. The 1st overload threshold is 1.3 A (min) and has an overload current switch threshold delay time (tOVLIN) of 110 μs (min) triggered by OUT.OUTn. Once this delay time has been exceeded, the overload threshold reduces to 0.7 A (min). Turn−on delay time is 8 us (max) and turn−off delay time is 12 μs (max). Rise and fall times are both 2.8 μs (min).

A turn off time longer than 2 x Internal Frequency Synchronization Time will reset the overload threshold back to the 1st level.

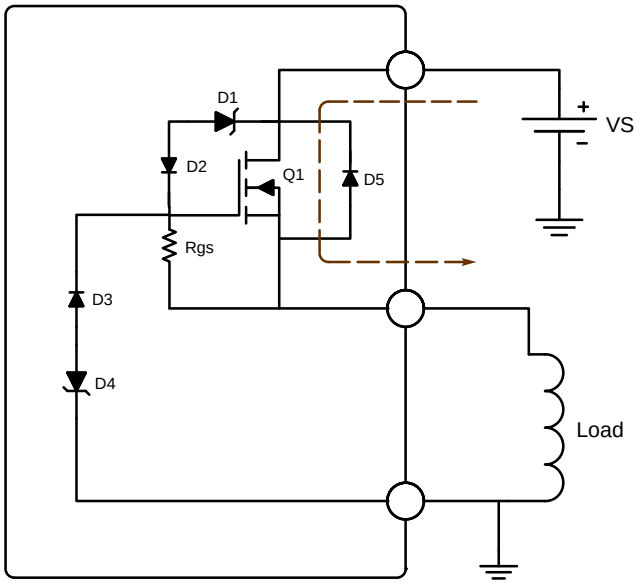
Relay loads are supported using an internal inductive clamp on the output driver to protect the driver. The negative transients seen when turning off an inductive load are internally limited on the output drivers with a clamp voltage minimum of −25 V. Paired output drivers are permissible with the use of the paired channel synchronization handling of overload and overtemperature conditions.

The NCV7755 is designed to drive 2 W lamps or 5 W lamps (using two channels in parallel) with its Bulb Inrush feature. Incandescent bulb in−rush characteristics are exhibited as a high current event due to the bulb filament initial low resistance. As the bulb heats up the resistance increases. Initial high currents could trigger an overload condition latching off the output. Setting a bit in the Bulb Inrush Mode register (BIM) allows the device to latch off (and report ERRn during that time [tRSTbim]) and automatically restart after the Bulb Inrush Mode Restart Time of 40 μs (max). Overtemperature conditions can also trigger a latch off event and auto−restart. The auto−restart helps to increase the bulb resistance putting the overload threshold out of range. Bulb Inrush Mode continues until the bulb is illuminated (not in overload) or the Bulb Inrush Mode reset time is reached (typically 40 ms). Dual Overload Detection Current thresholds continue to be valid in Bulb Inrush Mode.



BIM Continues for tBIM (40ms) [typ] provided OUT.OUTn=1 or bulb is illuminated.

Internal protection is provided for the output drivers for the maximum drain to source voltage and the absolute maximum voltage from the output to negative voltages which occurs on OUTx when inductive loads are turned off.



Protection for Q1 drain to source is provided by D1, D2, and Rgs.

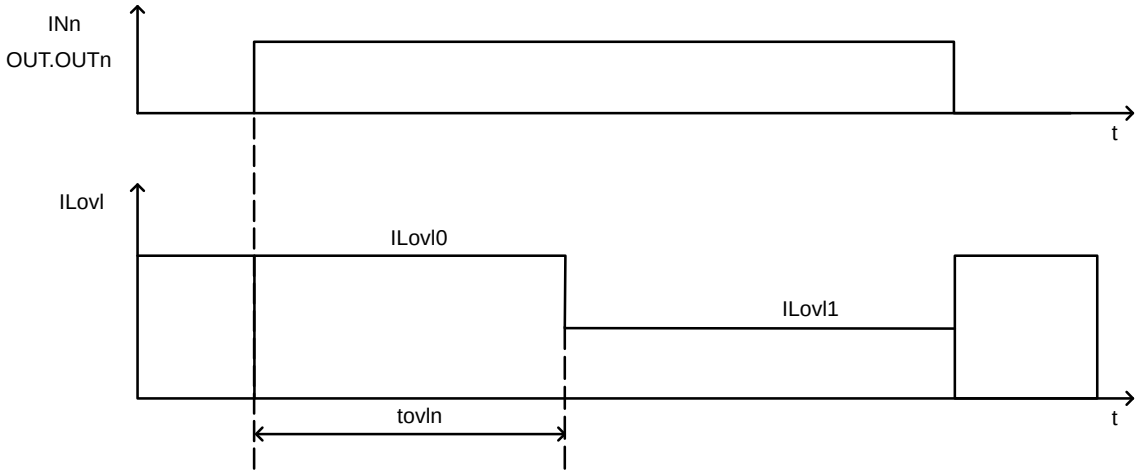
Protection for negative clamp voltages is provided by Rgs, D3, and D4.

Overload

Two overload current thresholds (ILovl0 & ILovl1) triggered by a turn−on command support the designer in driving highly capacitive loads. A higher initial current threshold (ILovl0) ignores potential in−rush events caused by high capacitance. The 2nd level supports maintenance of lower IC temperature levels during any shorted events while still providing proper operation.

This multi−level threshold strategy is implemented whenever the driver is active on. When operating in Bulb−Inrush mode (BIM), the auto−restart feature will also be active.

Overload detection conditions are latched off and require a SPI command to reactivate the effected output.



Thermal Shutdown− Individual thermal sensors are provided for each channel. A breach of the thermal shutdown threshold will latch the channel off and set the diagnostic bit ERRn for the channel. Clearing the error bit is done by setting the corresponding HWCR_OCL.OUTn bit to “1”. HWCR_OCL.OUTn is cleared after the error bit is cleared and the channel will accept commands to turn on.

During Bulb Inrush Mode, the output is “latched” off when the thermal threshold is breached, and will auto−restart once the thermal sensor no longer detects a fault.

Short to Ground – Overload conditions or Overtemperature conditions latch off the affected channel

Open Load at ON is controlled by the DIAG_OLONEN.MUX bits in the DIAG_OLONEN register. The default setting after reset is not active. DIAG_OLON.OUTn is set and mirrored into the Standard Diagnostic (bit OLON) if the output current is less than the Open Load ON Threshold Current. This is synonymous to an under load condition.

DIAG_OLONEN.MUX can be commanded on for a direct channel diagnostic or a diagnostic loop. Direct Channel diagnostic uses direct drive and is defined as control via SPI (Power output control register or control is mapped to IN0 (MAPIN0.outn) or IN1 (MAPIN1.outn). Diagnostic loop is programmed via SPI to the DIAG_OLONEN register (DIAG_OLONEN.MUX = 1010_B).

When operating in a direct channel mode, a detected open load will set the corresponding DIAG_OLON.OUTn bit and reset all the other bits in the DIAG_OLON register. Bits are updated upon register reading.

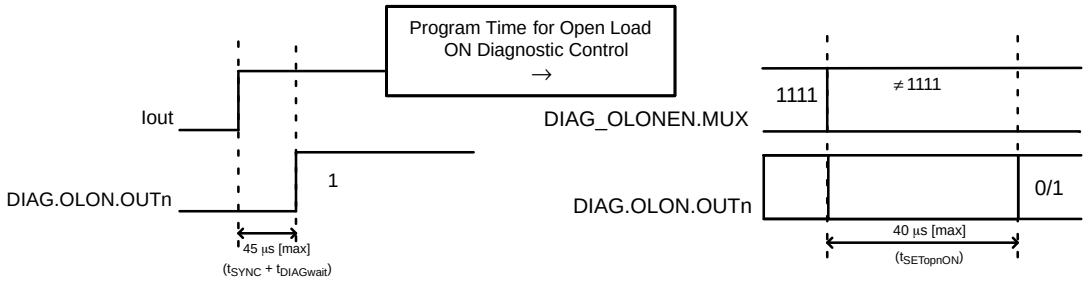
For operation in a diagnostic loop, DIAG_OLEN.MUX should be programmed with the value 1010_B. All channels are checked for Open Load at ON when operating in this mode. DIAG_OLON.OUTn is updated upon completion of each channel diagnostic. Value 1111_B (default) is set back in DIAG_OLONEN after the last channel is evaluated.

Direct Channel Diagnostic

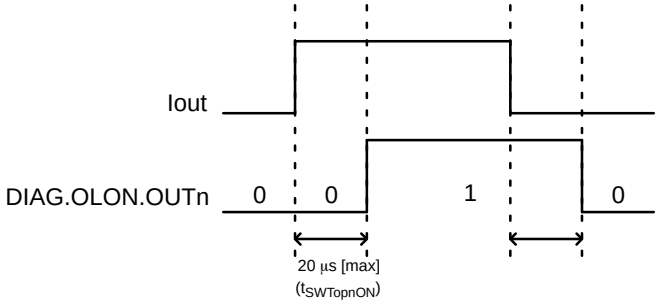
For Direct Channel Diagnostic, the device requires:

1. Time for the Internal Frequency Sync (10 µs [max]) (t_{SYNC})
2. Time for the output to turn on (tDIAGwait) (35 µs [max]). ($t_{DIAGwait}$)
   Open Load Monitor is now active.
3. Programming time for Open Load ON Diagnostic Control (DIAG_OLONEN.mux).
   (Time not specified here as this involves external control times)
4. Once step #3 is performed some Settling Time (tSETopnON) is required for the Open Load at ON Monitor (DIAG_OLON.OUT) to be available (40 µs [max] ($t_{SETopnON}$)

Once available, an Open Load at ON corresponding to a channel in the Open Load at ON Diagnostic Control Register (DIAG_OLONEN.MUX) will be reported upon request. Only one channel is available at a time. All other channels will report “0”.



When operated with the output previously commanded on, the time delay from fault occurrence to report in the register is the Open Load ON Channel Switching Time (20 µs [max]) ($t_{SWTopnON}$).



Channel Switching Delays ($t_{SWTopnON}$) (20 µs [max]) are linked to all the subsequent channel diagnostic for Open

Reverse Protection

In reverse polarity (OUTx > VSx), each channel will be on at nearly the forward Rdson for both VS operational (Figure 31 when commanded on) and at ground (Figure 32) or will conduct through the body diode (Figure 31 when commanded off).

VS Powered

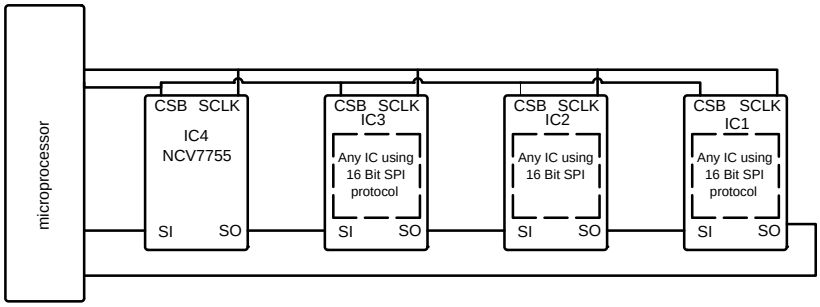
Parametric deviations, but no functional deviations of unaffected channels are possible during the reverse polarity event with VS Powered.

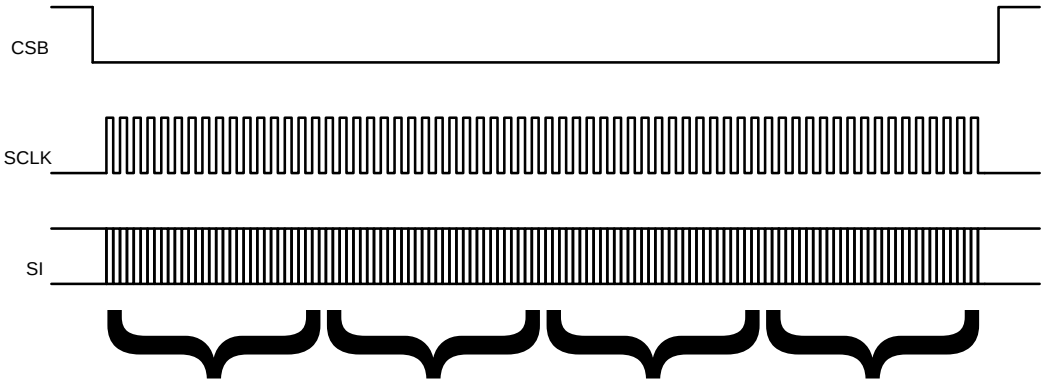
The reverse polarity channel stays in the ON (output = Rdson) or OFF (output = body diode) state as programmed before reverse polarity with VS powered (Figure 31). ON / OFF state (Rdson or body diode) is still programmable while

All channels are guaranteed off during a loss of ground

The NCV7755 is capable of being daisy chain connected using the SPI connectivity. While the NCV7755 is a 16−bit device, it can be coupled with other 8−bit SPI devices. It is important to note compatible SPI devices must clock data in on the negative edge of the clock. Reference the SPI diagram.

Daisy chain setups are possible with the NCV7755. The serial setup shown in Figure 33 highlights the NCV7755 along with any 16 bit device using a similar SPI protocol. Particular attention should be focused on the fact that the first 16 bits which are clocked out of the SO pin when the CSB pin transitions from a high to a low will be as per the SPI Protocol table. Additional programming bits should be clocked in which follow this. The timing diagram shows a typical transfer of data from the microprocessor to the SPI connected IC's.

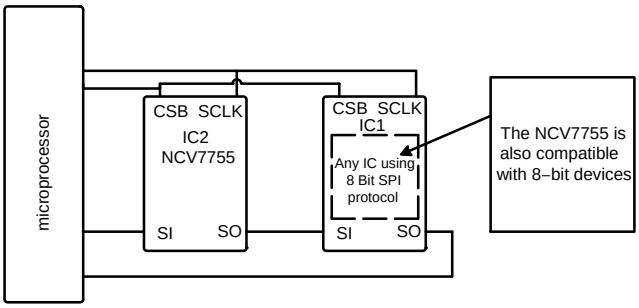




IC4	1st CMD	2nd CMD	3rd CMD	4th CMD
IC3	IC4 DIAG	1st CMD	2nd CMD	3rd CMD
IC2	IC3 DIAG	IC4 DIAG	1st CMD	2nd CMD
IC1	IC2 DIAG	IC3 DIAG	IC4 DIAG	1st CMD
microprocessor	IC1 DIAG	IC2 DIAG	IC3 DIAG	IC4 DIAG

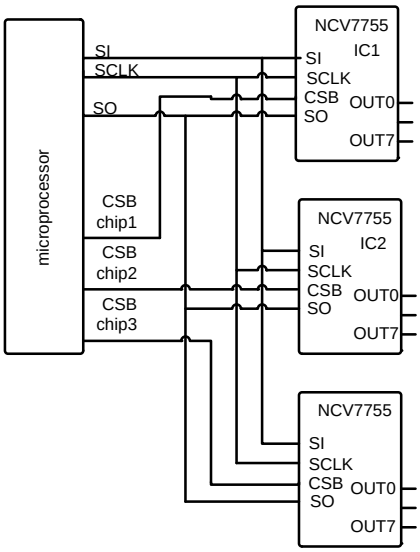
Table 4 refers to the transition of data over time of the Serial Daisy Chain setup of Figure 33 as word bits are shifted through the system. 64 bits are needed for complete transport of data in the example system. Each column of the table displays the status after transmittal of each word (in 16 bit increments) and the location of each word packet along the way.

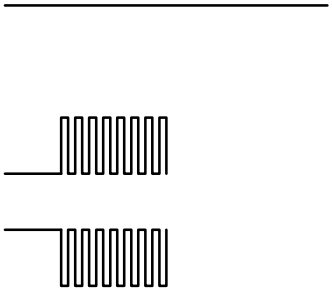
The NCV7755 is also compatible with 8 bit devices due to the features of the frame detection circuitry. The internal bit counter of the NCV7755 starts counting clock pulses when CSB goes low. The 1st valid word consists of 16 bits and each subsequent word must be comprised of just 8 bits (reference the Frame Detection Section).



NOTE: *Compatibility* Note the SCLK timing requirements of the NCV7755. Data is sampled from SI on the falling edge of SCLK. Data is shifted out of SO on the rising edge of SCLK. Devices with similar characteristics are required for operation in a daisy chain setup.

A more efficient way (time focused) to control multiple SPI compatible devices is to connect them in a parallel fashion and allow each device to be controlled in a multiplex mode. The Figure below shows a typical connection between the microprocessor or microcontroller and multiple SPI compatible devices. In a serial daisy chain configuration, the programming information for the last device in the serial string must first pass through all the previous devices. The parallel control setup eliminates that requirement, but at the cost of additional control pins from the microprocessor for each individual CSB (chip select bar) pin for each controllable device. Serial data is only recognized by the device that is activated through its respective CSB pin. The Figure below shows the waveforms for typical operation when addressing IC1.

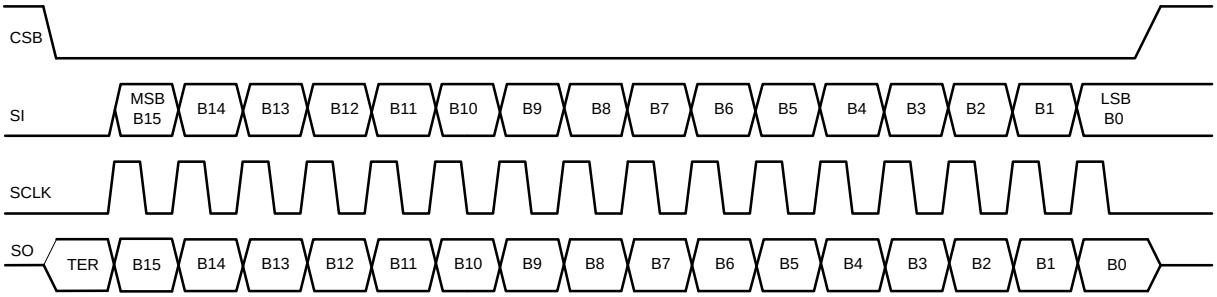




The SPI protocol works in conjunction with the 4 SPI pins, CSB, SCLK, SI, & SO.

- CSB – Chip Select Bar
  A high to low transition signals the IC that data is about to be clocked into the IC. Data is then clocked in via the SCLK and SI pins. Data completion is signaled by a low to high transition on the CSB pin
- SCLK – Serial clock input pin. Data bits from SI are shifted into the IC on the falling edge of SCLK. Data bits are shifted out of SO at the same time data bits are shifted into the IC. SCLK must be low when CSB makes a transition
- SI – Serial input pin. Data is shifted into the IC via the SI pin with the SCLK pin. The MSB (most significant pin) data is shifted in first. The Register Structure is composed of address and data bits with read/write designators
- SO – Serial output pin. The Diagnostics Register is clocked out of SO at the same time SI is input into the SI pin. The exception here is when operating in a daisy chain configuration when the 16−bit word clocked out the intended data for the next serial device

All 16 bit words from the SPI Diagnostics are read only bits. The SPI Diagnostics are returned following a received command.



The timing diagram highlighted above shows the SPI interface communication.

TER information retrieval is as simple as bringing CSB high−to−low. No clock signals are required although SI must be low when reading TER.

NOTES:

1. The MSB (most significant bit) is the first transmitted bit
2. Data is sampled from SI on the falling edge of SCLK
3. Data is shifted out from SO on the rising edge of

	Frame A	Previous response
	Frame B	Response to Frame A
	Frame C	Response to Frame B
	Write Register A	Previous response
	Read Register A	Standard Diagnostic
	New command	Register A content
	Frame A (error in transmission)	Previous response
	New command	Standard Diagnostic +TER
	Frame A	SO = hi impedance
	Frame B	INST Register +TER (8680h)
	Frame C	Response to Frame B
	Frame A (error)	Previous Response
	New command	Standard Diagnostic

The following will reset the SPI registers.
Device transitions to Sleep Mode.
This includes both of the conditions:

a. INx and IDLE are all = “0”
b. Both VDD and VS are in undervoltage

NOTE: Execution of a reset command (HWCR.RST = “1”) will clear (turn off) the outputs, but the ERR bits will not be cleared for safety reasons.

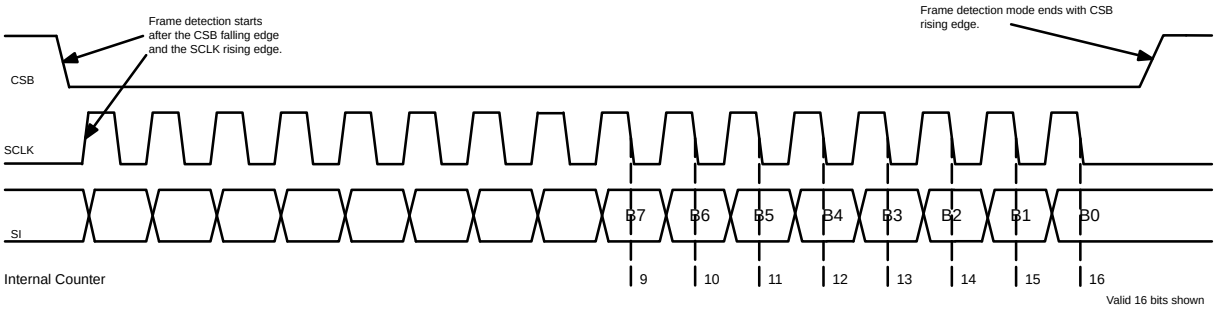
The NCV7755 detects the number of bits transmitted after CSB goes low for verification of word integrity. Bit counts not a multiple of 8 (16 bit minimum) are reported as a fault on the TER bit. The transmission error information (TER) is available on SO after CSB goes low until the first rising SCLK edge in the INST register, and the Standard Diagnostics Register.

In addition to unqualified bit counts setting TER = 1, the bit will also be set by

1. Coming out of UVLO for VDD
2. Transitioning from Limp Home Mode to Active Mode
3. Transitioning from Sleep Mode to Idle Mode

The TER bit is cleared by sending any valid SPI command.

The TER bit is multiplexed with the SPI SO data and OR'd with the SI input to allow for reporting in a serial daisy chain configuration. A TER error bit as a “1” automatically propagates through the serial daisy chain circuitry from the SO output of one device to the SI input of the next.


Frame detection starts
after the CSB falling edge
and the SCLK rising edge.
Frame detection mode ends with CSB
rising edge.
CSB
SCLK
SI
B7
B6
B5
B4
B3
B2
B1
B0
Internal Counter
9
10
11
12
13
14
15
16
Valid 16 bits shown

Read Standard Diagnostics	$0xxxxxxxxxxxxx01_B$	$0ddddddddddddddd_B$
Write 8−bit register	$10aaaabbcccccccc_B$	$0ddddddddddddddd_B$
Read 8−bit register	$01aaaabbxxxxxx10_B$	$10aaaabbcccccccc_B$
Write 10−bit register	$10aaaaccccccccc_B$	$0ddddddddddddddd_B$
Read 10−bit register	$01aaaaxxxxxxxx10_B$	$10aaaaccccccccc_B$

x = don't care
a = ADDR0 field
b = ADDR1 field

c = register content
d = diagnostic bit

OUT	4002_H	$80XX_H$	$XX_H = xxxxxxxx_B$
BIM	4102_H	$81XX_H$	$XX_H = xxxxxxxx_B$
MAPIN0	4402_H	$84XX_H$	$XX_H = xxxxxxxx_B$
MAPIN1	4502_H	$85XX_H$	$XX_H = xxxxxxxx_B$
INST	4602_H	(read only)	–
DIAG_IOL	4802_H	$88XX_H$	$XX_H = xxxxxxxx_B$
DIAG_OSM	4902_H	(read only)	$XX_H = xxxxxxxx_B$
DIAG_OLON	$4A02_H$	$8AXX_H$	–
DIAG_OLONEN	$4B02_H$	$8BXX_H$	$XX_H = xxxxxxxx_B$
HWCR	$4C02_H$	$8CXX_H$	$XX_H = xxxxxxxx_B$
HWCR_OCL	$4D02_H$	$8DXX_H$	$XX_H = xxxxxxxx_B$
HWCR_PWM	$4E02_H$	$8EXX_H$	$XX_H = xxxxxxxx_B$
PWM_CR0	5002_H	$90XX_H$ $91XX_H$ $92XX_H$ $93XX_H$	$0XX_H = 00xxxxxxx_B$ $1XX_H = 01xxxxxxx_B$ $2XX_H = 10xxxxxxx_B$ $3XX_H = 11xxxxxxx_B$
PWM_CR1	5402_H	$94XX_H$ 95XX	

SPI STANDARD DIAGNOSTICS

A Read Standard diagnostics command provides a response with a snapshot of the status of all the monitored faults on the IC. Further fault details (channel fault number etc…) can be reviewed in the subsequent register structure banks.

All 16 bit words from the SPI Diagnostics are read only bits. The SPI Diagnostics are returned with the next command after a Read Standard Diagnostics Command 0xxxxxxxxxxxxxx01b where x = don't care.

Table 5. SPI DIAGNOSTIC TABLE

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	UVRVS														

(PWM_CR0/1 registers)(10 bit DATA register)

R=0 W=1	R=1 W=0	ADDR0				DATA									

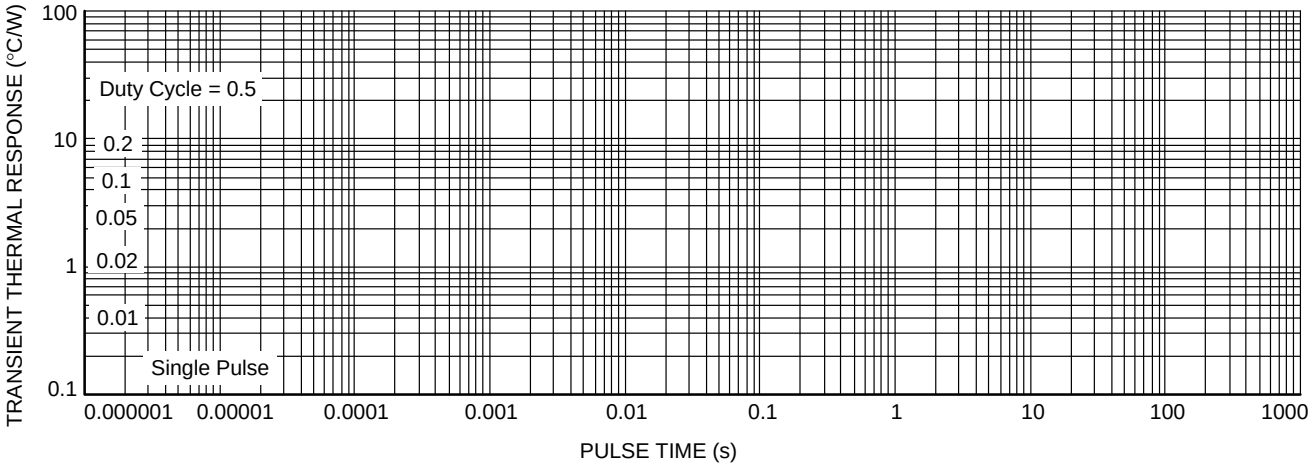
20. Read and Write designators require two bits (14 and 15)(r = read, w = write).

OUT	0000_B	00_B	r/w	0000BB

DIAG_OLONEN	0010_B			

Table 7. DETAILED REGISTER STRUCTURE

Register Name	ADDR0	ADDR1	Type	Purpose
				PWM1 Active bits (HWCR_PWM.PWM1) (1) 0_B (default) PWM Generator 1 not active 1_B PWM Generator 1 active
				PWM0 Active (HWCR_PWM.PWM0) (0) 0_B (default) PWM Generator 0 not active 1_B PWM Generator 0 active
PWM_CR0	0100_B	ïïï	r/w	PWM Generator 0 Configuration
				CR0 Frequency (PWM_CR0.FREQ) (9:8) 00_B Internal clock divided by 1024 (100 Hz) (default) 01_B Internal clock divided by 512 (200 Hz) 10_B Internal clock divided by 256 (400 Hz) 11_B 100% Duty Cycle.
				CR0 generator on/off control (PWM_CRO.DC) (7:0) 00000000_B PWM generator is off. (default) 11111111_B PWM generator is On (99.61% DC).
PWM_CR1	0101_B	ïïï	r/w	PWM Generator 1 Configuration
				CR1 Frequency(PWM_CR1.FREQ) (9:8) 00_B Internal clock divided by 1024 (100Hz) (default) 01_B Internal clock divided by 512 (200 Hz) 10_B Internal clock divided by 256 (400 Hz) 11_B 100% Duty Cycle
				CR1 generator on/off control (PWM_CR1.DC) (7:0) 00000000_B PWM generator is off. (default) 11111111_B PWM generator is On (99.61% DC)
PWM_OUT	1001_B	00_B	r/w	PWM Generator Output Control (PWM_OUT.OUTn) 0_B (default) The selected ouput is not driven by one of the two PWM generators 1_B The selected output is connected to a PWM generator DATA = Channel number 0 to 7
PWM_MAP	1001_B	01_B	r/w	PWM Generator Output Mapping (PWM_MAP.OUTn) 0_B (default) The selected output is connected to PWM Generator 0 1_B The selected output is connected to PWM Generator 1 DATA = Channel number 0 to 7 Works in conjunction with PWM_OUT


TRANSIENT THERMAL RESPONSE (°C/W)
100
10
1
0.1
Duty Cycle = 0.5
0.2
0.1
0.05
0.02
0.01
Single Pulse
0.000001
0.00001
0.0001
0.001
0.01
0.1
1
10
100
1000
PULSE TIME (s)

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