1	VBB	Battery supply input	Battery connection
2	LIN	LIN bus interface	LIN bus pin, low in dominant state
3	GND (Note 1)	Ground	Ground connection
4	OUT5	LS driver	Channel 5 Low−side drive output, Ron = 1.5 Ω (typ)
5	OUT6	LS driver	Channel 6 Low−side drive output, Ron = 1.5 Ω (typ)
6	OUT7	LS driver	Channel 7 Low−side drive output, Ron = 1.5 Ω (typ)
7	OUT8	LS driver	Channel 8 Low−side drive output, Ron = 0.8 Ω (typ)
8	OUT4	LS driver	Channel 4 Low−side drive output, Ron = 0.8 Ω (typ)
9	OUT3	LS driver	Channel 3 Low−side drive output, Ron = 1.5 Ω (typ)
10	OUT2	LS driver	Channel 2 Low−side drive output, Ron = 1.5 Ω (typ)
11	OUT1	LS driver	Channel 1 Low−side drive output, Ron = 1.5 Ω (typ)
12	GND (Note 1)	Ground	Ground connection
13	NAD	LV analog input/output	Node Addressing via external resistor (NAD selection)
14	CONF	LV analog input/output	Defines virtual node configuration position via external resistor

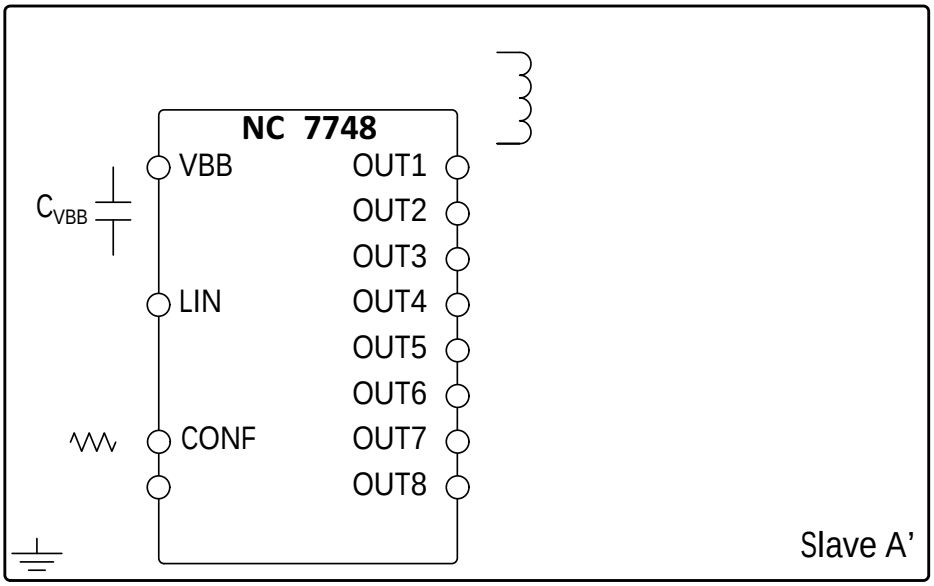
NOTE: (LV = Low Voltage)

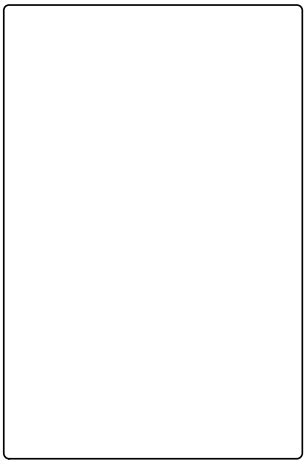
1. Pins 3 and 12 must be shorted externally.

(See Figure 2)

C_{VBB}	Decoupling capacitor on battery line, ceramic (X7R)	100	nF	20%
C_{Bulk}	Bulk capacitor (energy storage)	Depends on minimum battery voltage profile requirements		
R_{NAD}	Resistor for defining NAD of device	475 (Note 2)	Ω	1% (Note 5)
R_{CONF1}	Resistor for defining device's position in virtual node	10.0 (Note 3)	kΩ	1% (Note 5)
R_{CONF2}	Resistor for defining device's position in virtual node	1.00 (Note 4)	kΩ	1% (Note 5)
D1 – D2	Power supply diode for relays and NCV7748	e.g. MRA4003T3G		
D_{ESD}	Optional LIN ESD protection diode	e.g. NUP1105LT1G or MMBZ27x		

2. Node Address = 0x60
3. Position of device in the virtual node = A′
4. Position of device in the virtual node = B
5. This tolerance is required for every value of used resistors on NAD and CONF pins selected according to Table 6 and Table 7. The initial 1% tolerance of resistors must not get worse than 3% over the application life time.


NC 7748
VBB
OUT1
OUT2
OUT3
LIN
OUT4
OUT5
OUT6
CONF
OUT7
OUT8
C_{VBB}
Slave A'



Vmax_VBB	Power supply voltage	−0.3	+40	V
Vmax_LIN	DC voltage on LIN pin	−40	+40	V
Vmax_OUTx	OUT pins voltage range DC (voltage internally limited during flyback)	−0.3	38	V
Vmax_OUTx_peak	OUT pins peak voltage range Internally limited. Applies to VBB range from 0 V to Vmax_VBB (powered and unpowered modes)		45	V
Imax_OUT4,8	Maximum OUT4,8 pin current	−0.2	1.3	A
Imax_OUT1−3,5−7	Maximum OUT1−3, 5−7 pin current	−0.2	1.2	A
Clmp_sing Clmp_rep	Clamping energy Maximum (single pulse) OUT1−3, 5−7 (IOUT = 300 mA, T_A = 150°C) OUT4,8 (IOUT = 400 mA, T_A = 150°C) Repetitive (multiple) 2M pulses, VBB = 15 V, 63 Ω, 390 mH, T_A = 25°C	 − −	 40 65	mJ
Vmax_CONF	CONF pin DC maximum voltage	−0.3	3.6	V
Vmax_NAD	NAD pin DC maximum voltage	−0.3	3.6	V
RSC_level	AEC Q100−012 Short Circuit Reliability Characterization	Grade A (minimum of 1 million of cycles)		
ESD Human Body Model (100 pF, 1500 Ω)	All pins	−2	+2	kV
	Pin LIN to GND	−6	+6	
ESD following IEC 61000−4−2 (150 pF, 330 Ω)	Valid for pins VBB to GND and LIN to GND VBB pin with reverse−protection and filtering capacitor	−6	+6	kV
Tj_mr	Junction temperature	−40	+150	°C
Tstg	Storage Temperature Range	−55	+150	°C
MSL	Moisture Sensitivity Level (max. 260°C processing)	3		

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

6 V ≤ V_{BB} ≤ 18 V, −40°C ≤ Tj ≤ 150°C; unless otherwise specified; $R_{L(LIN-VBB)}$ = 500 Ω, unless otherwise specified. Typical values are given at V(V_{BB}) = 12 V and T_J = 25°C, unless otherwise specified.

VBB	Supply Voltage	Functional (Note 8)	4	−	38	V
		Parameter specification	6	−	18	
VBB_PORH	VBB POR threshold	VBB rising	3.2	−	4	V
VBB_PORL	VBB POR threshold	VBB falling	3	−	3.7	V
VBB_UV_H	UV−threshold voltage high level	VBB rising (Note 8)	4	−	5	V
VBB_UV_L	UV−threshold voltage low level	VBB falling (Note 8)	3.8	−	4.7	V

8. Below 5 V on VBB in normal mode, the LIN bus will either stay recessive or comply with the voltage level specifications and transition time pir togg2.85) but p68.951 6(BB)Tnot gu68.nte0.044 ..09 lt754 .737 77.72l_3.60 sta04 ref59.754 340ef044 77.7223.988.743 refBT5 3017V

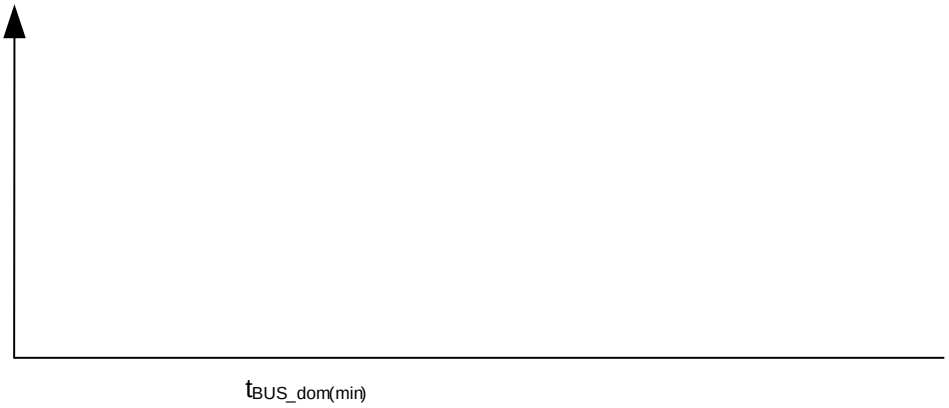
6 V ≤ V_{BB} ≤ 18 V, −40°C ≤ Tj ≤ 150°C; unless otherwise specified; $R_{L(LIN-VBB)}$ = 500 Ω, unless otherwise specified. Typical values are given at V(V_{BB}) = 12 V and T_J = 25°C, unless otherwise specified.

T_OC_del	Overcurrent Shut−Down Delay Time on OUTx pins	OUTx shorted to VBB	3	15	50	µs
T_OL_det	Open Load Detection Time OUT4, OUT8		30	115	200	µs

T_{jsd}	Global Thermal shut−down level	Guaranteed by design and prototype evaluations, not tested in production	150	175	190	°C
$T_{jsd\_hys\_global}$	Thermal shut−down hysteresis	Guaranteed by design and prototype evaluations, not tested in production	−			

6 V ≤ V_{BB} ≤ 18 V, −40°C ≤ Tj ≤ 150°C; unless otherwise specified; $R_{L(LIN-VBB)}$ = 500 Ω, unless otherwise specified. Typical values are given at V(V_{BB}) = 12 V and T_J = 25°C, unless otherwise specified.

		(The following bus loads are considered: BL1 = 1 kΩ / 1 nF; BL2 = 660 Ω / 6.8 nF; BL3 = 500 Ω / 10 nF)(Resistor = Vbat to LIN, Capacitor = LIN to GND)				
D1	Duty Cycle 1 = $t_{BUS\_rec(min)}$ / (2 x TBit) (see Figure 3)	$TH_{Rec(max)}$ = 0.744 x VBB, $TH_{Dom(max)}$ = 0.581 x VBB, Tbit = 50 µs, VBB = 7 V to 18 V, BL1, BL2, BL3	0.396		0.5	
D2	Duty Cycle 2 = $t_{BUS\_rec(max)}$ / (2 x TBit) (see Figure 3)	$TH_{Rec(min)}$ = 0.422 x VBB, $TH_{Dom(min)}$ = 0.284 x VBB, Tbit = 50 µs, VBB = 7.6 V to 18 V, BL1, BL2, BL3	0.5		0.581	
D3	Duty Cycle 3 = $t_{BUS\_rec(min)}$ / (2 x TBit) (see Figure 3)	$TH_{Rec(max)}$ = 0.788 x VBB, $TH_{Dom(max)}$ = 0.616 x VBB, Tbit = 96 µs, VBB = 7 V to 18 V BL1, BL2, BL3	0.417		0.5	
D4	Duty Cycle 4 = $t_{BUS\_rec(max)}$ / (2 x TBit) (see Figure 3)	$TH_{Rec(min)}$ = 0.389 x VBB, $TH_{Dom(min)}$ = 0.251 x VBB, Tbit = 96 µs VBB = 7.6 V to 18 V, BL1, BL2, BL3	0.5		0.59	
T_fall_LIN	LIN falling edge (see Figure 4) BL1,BL2	VBB = 12 V; BL1, BL2 40% to 60% measurements extrapolated to 0% to 100%			22.5	µs
T_rise_LIN	LIN rising edge (see Figure 4) BL1,BL2	VBB = 12 V; BL1, BL2 40% to 60% measurements extrapolated to 0% to 100%			22.5	µs
T_sym_LIN	LIN slope symmetry BL1,BL2	Normal mode VBB = 12 V; BL1, BL2	−6	0	6	µs
T_fall_LIN_L3	LIN falling edge (see Figure 4) BL3	VBB = 12 V; BL3 40% to 60% measurements extrapolated to 0% to 100%				


tBUS_dom(min)

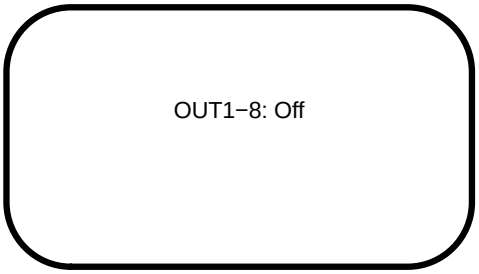
two BASIC modes

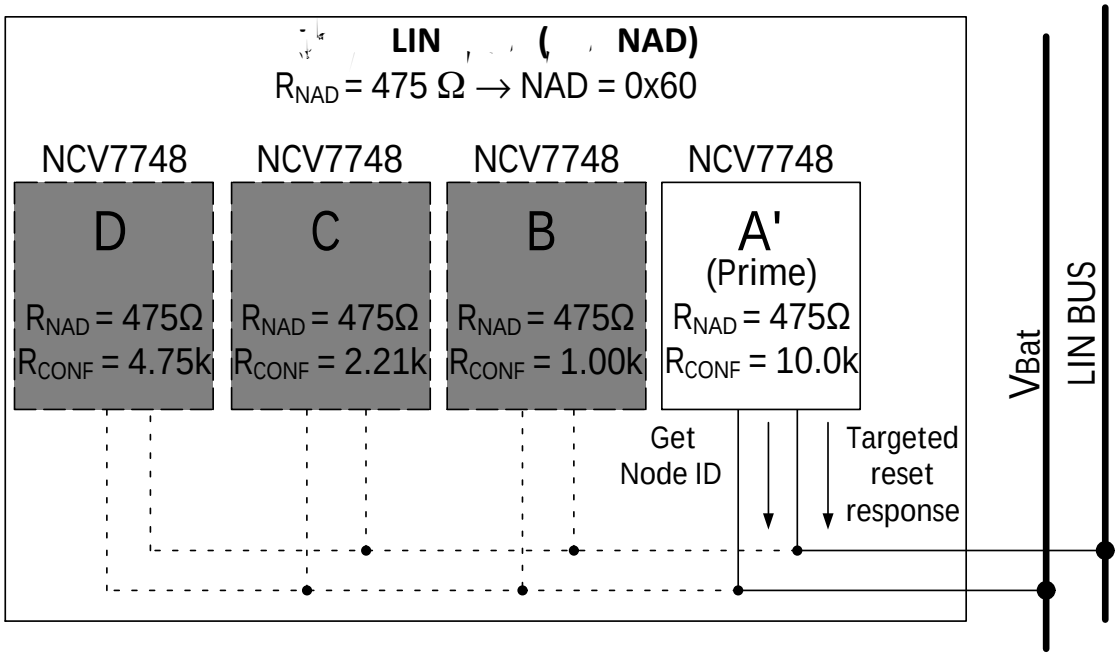
Normal mode
Sleep mode

$$\frac{(14\ V - 2.5\ V)}{140\ \mu A}$$

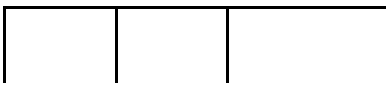
$$\frac{(VS - OpenLoadDetectionThresholdvoltage)}{OpenLoadDiagnosticSinkCurrent} = \text{OpenLoad Impedance}$$

Local Thermal Shutdown Overcurrent Detection


OUT1−8: Off



Output Control	Sets all outputs in one virtual node	8	Depends on NAD (See Table 12)	N/A
	Reads identity of prime device in virtual node. (In frame slave Response)	8	Depends on NAD (See Table 23)	N/A
	Reads diagnostics of one device (LS driver). (In frame slave Response)	8	Depends on CONF (See Table 7) and NAD (See Table 18)	N/A
	Re−initialization of one virtual node. This includes all devices on the virtual node.	8	0x3C	J2602− ï ï



Master	0	Identifier	PID						
Slave	1	Data 1	ERR2	ERR1	ERR0	APPINFO			
	2	Data 2	OUT4 STATUS		OUT3 STATUS		OUT2 STATUS	OUT1 STATUS	
	3	Data 3	OUT8 STATUS		OUT7 STATUS		OUT6 STATUS	OUT5 STATUS	
	4	Data 4	0x00 (NULL)						
	5	Data 5	0x00 (NULL)						
	6	Data 6	0x00 (NULL)						
	7	Data 7	0x00 (NULL)						
	8	Data 8	0x00 (NULL)						
	9	Checksum	Enhanced Checksum						

00b	OFF	Open Load Fault (non−latching)	Only OUT4/8
01b	OFF	Per setting or active Global TSD	All OUTx, Default after reset
10b	ON	Per setting	All OUTx
11b	ON	Latched OFF from ON state due to TSD/OC	TSD / OUT4/8; OC on all OUTx

0	0	0	No Error	0 (lowest)
0	0	1	Reset	1
0	1	0	Reserved	2
0	1	1	Reserved	3
1	0	0	Data Error	4
1	0	1	Data Checksum	5
1	1	0	Byte Field Framing Error	6
1	1	1	ID Parity Error	7 (highest)

00000b	Default − No Failure to Report

No Failure to Report

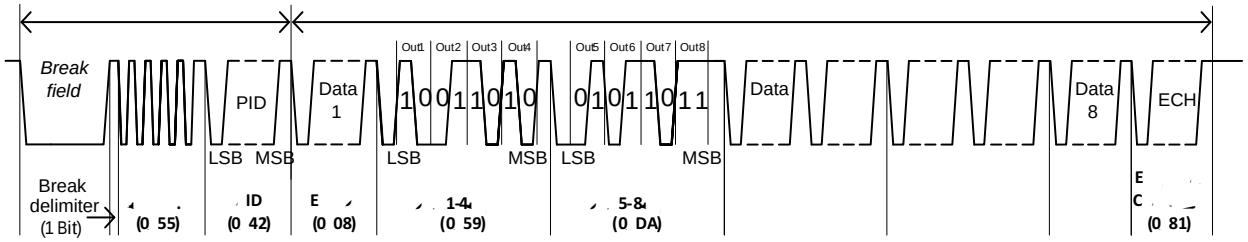
```
ID = 0x02 [Table ID] => PID = 0x42 [LIN2.2]
(Reference Table 19)

Data1 = 0x08 => OUT4,OUT8 TSD / OC
(0b 000 01000)

Data2 = 0x59 =>  OUT1 : Off (01)
(0b 01 01 10 01) OUT2 : ON  (10)
                 OUT3 : Off (01)
                 OUT4 : Off (01)

Data3 = 0xDA =>  OUT5 : ON  (10)
(0b 11 01 10 10) OUT6 : ON  (10)
                 OUT7 : Off (01)
                 OUT8 : Off (11)Latched Off due to TSD/OC
```

			1	2	3	4	
OUT1−4	0x59	LSB	10	01	10	10	MSB
OUT5−8	0xDA	LSB	01	01	10	11	MSB



$60	$0	0x80	$64	$10	0x50	$68	$20	0x20	$6C	$30	0xF0
	$1			$11			$21			$31	
	$2			$12			$22			$32	
	$3			$13			$23			$33	
	$4			$14			$24			$34	
	$5			$15			$25			$35	
	$6			$16			$26			$36	
	$7			$17			$27			$37	
$62	$8	0x08	$66	$18	0xD8	$6A	$28	0xA8	$6E	No Message IDs defined	
	$9			$19			$29				
	$0A			$1A			$2A				
	$0B			$1B			$2B				
	$0C			$1C			$2C		$6F	No Message IDs defined	
	$0D			$1D			$2D				
	$0E			$1E			$2E				
	$0F			$1F			$2F				

Master	0	Identifier	0x00 (Parity)		0x3C (ID)					
	1	Data 1	NAD or 0x7F (Wildcard NAD)							
	2	Data 2	0x06 (PCI)							
	3	Data 3	0xB2 (SID)							
	4	Data 4	Node Identifier (see Node Identification Table 28)							
	5	Data 5	Supplier ID LSB (0x24) or 0xFF (Wildcard Supplier ID)							
	6	Data 6	Supplier ID MSB (0x00) or 0x7F (Wildcard Supplier ID)							
	7	Data 7	Function ID LSB (0x48/0x44) or 0xFF (Wildcard Function ID)							
	8	Data 8	Function ID MSB (0x60) or 0xFF (Wildcard Function ID)							
	9	Checksum	Classic Checksum							

Master	0	Identifier	0x01 (Parity)		0x3D (ID)					
Slave	1	Data 1	NAD							
	2	Data 2	0x06 (PCI)							
	3	Data 3	0xF2 (RSID)							
	4	Data 4	Supplier ID LSB (0x24)							
	5	Data 5	Supplier ID MSB (0x00)							
	6	Data 6	Function ID LSB (0x48/0x44)							
	7	Data 7	Function ID MSB (0x60)							
	8	Data 8	Silicon Version							
	9	Checksum	Classic Checksum							

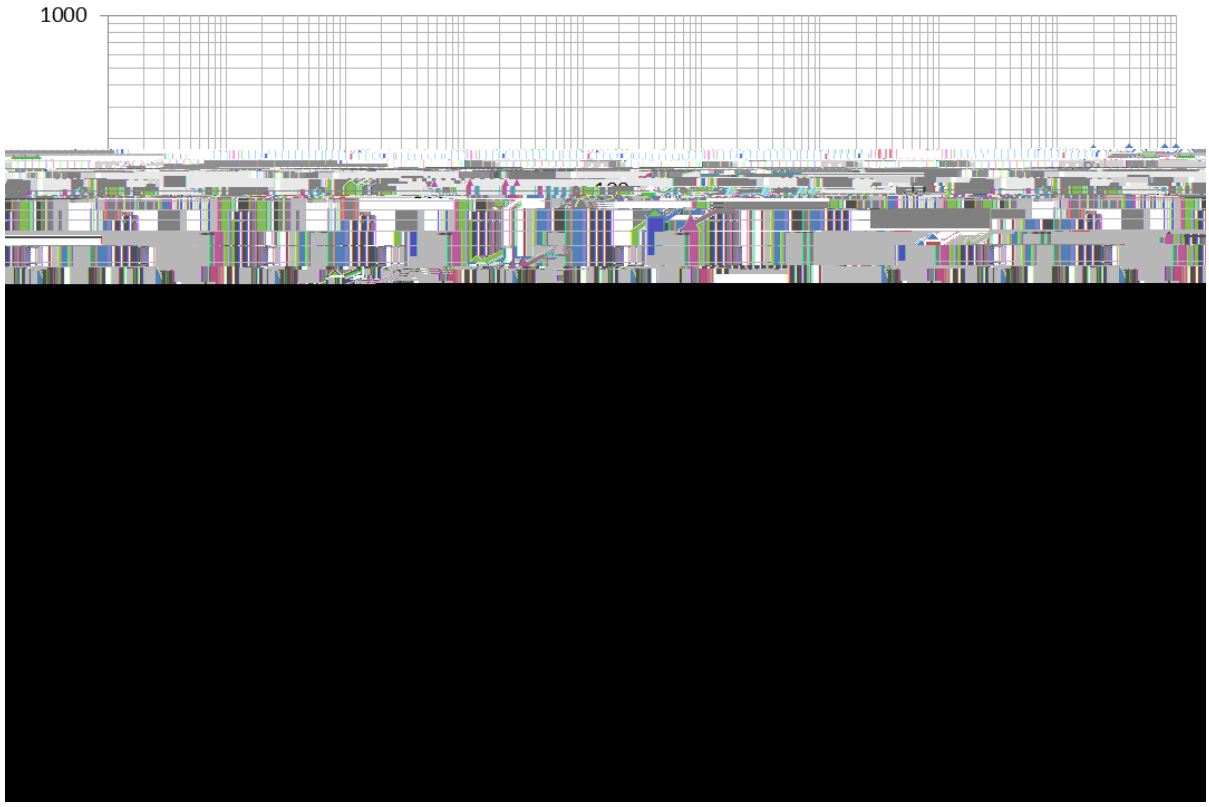
Master	0	Identifier	0x01 (Parity)		0x3D (ID)					
Slave	1	Data 1	NAD							
	2	Data 2	0x03 (PCI)							
	3	Data 3	0x7F (RSID)							
	4	Data 4	0xB2 (Requested SID)							
	5	Data 5	0x12 (Error Code)							
	6	Data 6	0xFF							
	7	Data 7	0xFF							
	8	Data 8	0xFF							
	9	Checksum	Classic Checksum							

Master	0	Identifier	0x00 (Parity)						0x3C (ID)	
	1	Data 1	NAD							
	2	Data 2	0x01							
	3	Data 3	0xB5							
	4	Data 4	0xFF							
	5	Data 5	0xFF							
	6	Data 6	0xFF							
	7	Data 7	0xFF							
	8	Data 8	0xFF							
	9	Checksum	Classic Checksum							

Master	0	Identifier	0x01 (Parity)						0x3D (ID)	
Slave	1	Data 1	NAD							
	2	Data 2	0x06							
	3	Data 3	0xF5							
	4	Data 4	Supplier ID LSB (0x24)							
	5	Data 5	Supplier ID MSB (0x00)							
	6	Data 6	Function ID LSB (0x48/0x44)							
	7	Data 7	Function ID MSB (0x60)							
	8	Data 8	Silicon Version							
	9	Checksum	Classic Checksum							

Master	0	Identifier	0x00 (Parity)						0x3C (ID)	
	1	Data 1	0x00							
	2	Data 2	0xXX							
	3	Data 3	0xXX							
	4	Data 4	0xXX							
	5	Data 5	0xXX							
	6	Data 6	0xXX							
	7	Data 7	0xXX							
	8	Data 8	0xXX							
	9	Checksum	Classic Checksum							

Open load (OUT4 and OUT8)	Not signaled.	Signaled in OFF Mode	Per setting	Driver in Normal operation	Load re−connected	NA
Overcurrent	Latched	latched				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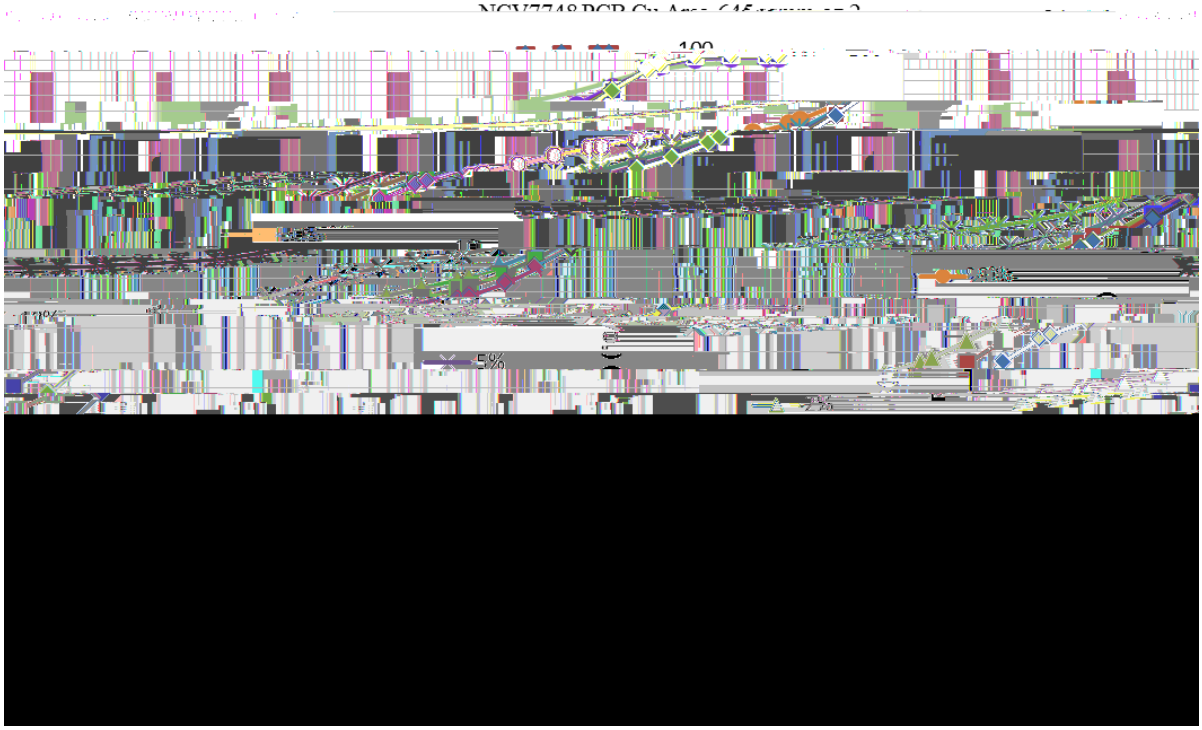
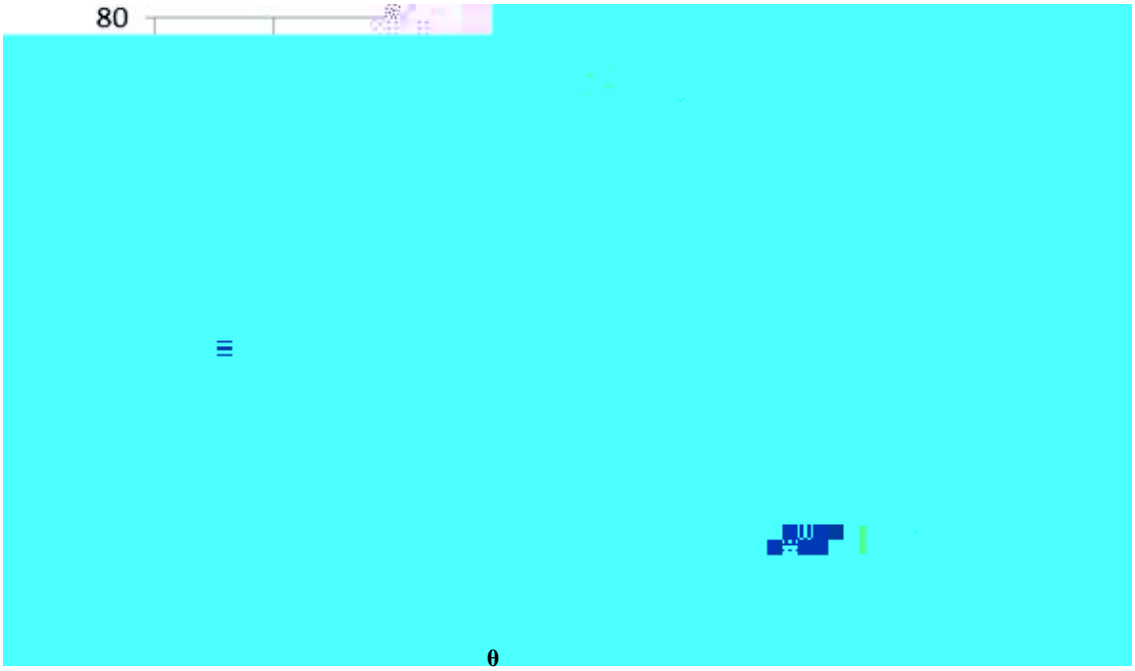
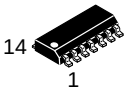

100
10%
5%


80
θ

			†
NCV7748D2R2G	8	SOIC−14 (Pb−Free)	2500 / Tape & Reel

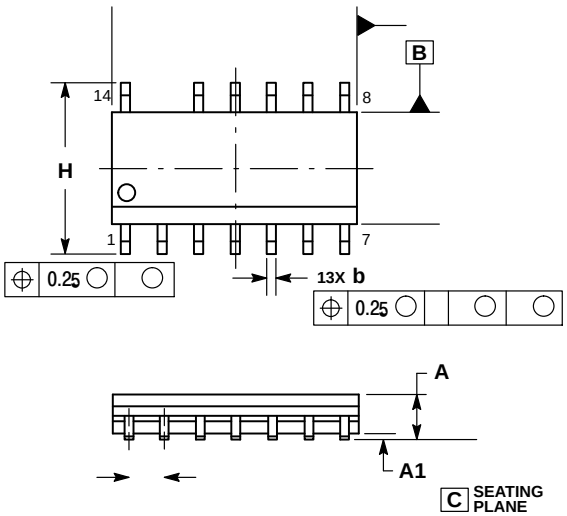
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.



SCALE 1:1

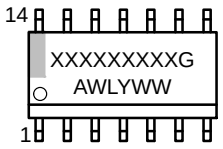
SOIC 14 NB
CASE 751A−03
ISSUE L

DATE 03 FEB 2016



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF AT MAXIMUM MATERIAL CONDITION.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSIONS.
5. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.

GENERIC
MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week
G = Pb−Free Package

STYLES ON PAGE 2

SOIC 14
CASE 751A−03
ISSUE L

DATE 03 FEB 2016

STYLE 7:
PIN 1. ANODE/CATHODE
2. COMMON ANODE
3. COMMON CATHODE
4. ANODE/CATHODE
5. ANODE/CATHODE