Table 1. PIN FUNCTION DESCRIPTION, NCV7748

Pin No.	Pin Name	Pin Type	Description
1	VBB	Battery supply input	Battery connection
2	LIN	LIN bus interface	LIN bus pin, low in dominant state
3	GND (Note 1)	Ground	Ground connection
4	OUT5	LS driver	Channel 5 Low-side drive output, Ron = 1.5 Ω (typ)
5	OUT6	LS driver	Channel 6 Low–side drive output, Ron = 1.5 Ω (typ)
6	OUT7	LS driver	Channel 7 Low-side drive output, Ron = 1.5 Ω (typ)
7	OUT8	LS driver	Channel 8 Low–side drive output, Ron = 0.8 Ω (typ)
8	OUT4	LS driver	Channel 4 Low-side drive output, Ron = 0.8 Ω (typ)
9	OUT3	LS driver	Channel 3 Low–side drive output, Ron = 1.5 Ω (typ)
10	OUT2	LS driver	Channel 2 Low-side drive output, Ron = 1.5 Ω (typ)
11	OUT1	LS driver	Channel 1 Low-side drive output, Ron = 1.5 Ω (typ)
12	GND (Note 1)	Ground	Ground connection
13	NAD	LV analog input/output	Node Addressing via external resistor (NAD selection)
14	CONF	LV analog input/output	Defines virtual node configuration position via external resistor

NOTE: (LV = Low Voltage)

1. Pins 3 and 12 must be shorted externally.

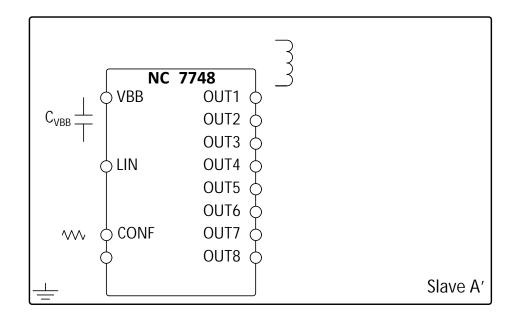
Table 2. EXTERNAL COMPONENTS SPECIFICATION (See Figure 2)

Component	Function	Value	Unit	Tolerance	
C _{VBB}	Decoupling capacitor on battery line, ceramic (X7R)	100	nF	20%	
C _{Bulk}	Bulk capacitor (energy storage)	Depends on minimum battery voltage profile requirements			
R _{NAD}	Resistor for defining NAD of device	475 (Note 2)	Ω	1% (Note 5)	
R _{CONF1}	Resistor for defining device's position in virtual node	10.0 (Note 3)	kΩ	1% (Note 5)	
R _{CONF2}	Resistor for defining device's position in virtual node	1.00 (Note 4)	kΩ	1% (Note 5)	
D1 – D2	Power supply diode for relays and NCV7748	e.g. MRA4003T3G			
D _{ESD}	Optional LIN ESD protection diode	e.g. NUP1105LT1G or MMBZ27x			

Node Address = 0x60
 Position of device in the virtual node = A'

4. Position of device in the virtual node = B

5. This tolerance is required for every value of used resistors on NAD and CONF pins selected according to Table 6 and Table 7. The initial 1% tolerance of resistors must not get worse than 3% over the application life time.



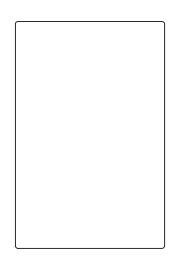


Table 3. ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Min	Max	Unit
Vmax_VBB	Power supply voltage	-0.3	+40	V
Vmax_LIN	DC voltage on LIN pin	-40	+40	V
Vmax_OUTx	OUT pins voltage range DC (voltage internally limited during flyback)	-0.3	38	V
Vmax_OUTx_peak	OUT pins peak voltage range Internally limited. Applies to VBB range from 0 V to Vmax_VBB (powered and unpowered modes)		45	V
Imax_OUT4,8	Maximum OUT4,8 pin current	-0.2	1.3	А
lmax_OUT1-3,5-7	Maximum OUT1-3, 5-7 pin current	-0.2	1.2	А
Clmp_sing Clmp_rep	Clamping energy Maximum (single pulse)			mJ
	OUT1–3, 5–7 (IOUT = 300 mA, T _A = 150°C) OUT4,8 (IOUT = 400 mA, T _A = 150°C) Repetitive (multiple) 2M pulses, VBB = 15 V, 63 Ω, 390 mH, T _A = 25°C	-	40 65	
Vmax_CONF	CONF pin DC maximum voltage	-0.3	3.6	V
Vmax_NAD	NAD pin DC maximum voltage	-0.3	3.6	V
RSC_level	AEC Q100–012 Short Circuit Reliability Characterization	Grade A (minimum of 1 million of cycles)		
ESD Human Body Model	All pins	-2	+2	kV
(100 pF, 1500 Ω)	Pin LIN to GND	-6	+6	
ESD following IECValid for pins VBB to GND and LIN to GND61000-4-2 (150 pF, 330 Ω)VBB pin with reverse-protection and filtering capacitor		-6	+6	kV
Tj_mr	Junction temperature	-40	+150	°C
Tstg	Storage Temperature Range	-55	+150	°C
MSL	Moisture Sensitivity Level (max. 260°C processing)	:	3	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

Table 4. THERMAL CHARACTERISTICS

Symbol

Parameter

Table 5. ELECTRICAL CHARACTERISTICS 6 V \leq V _{BB} \leq 18 V, -40°C \leq Tj \leq 150°C; unless otherwise specified; R _{L(LIN-VBB)} =
500 Ω, unless otherwise specified. Typical values are given at V(V _{BB}) = 12 V and T _J = 25°C, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
VBB SUPPLY						
VBB	Supply Voltage	Functional (Note 8)	4	-	38	V
		Parameter specification	6	-	18	
VBB_PORH	VBB POR threshold	VBB rising	3.2	-	4	V
VBB_PORL	VBB POR threshold	VBB falling	3	-	3.7	V
VBB_UV_H	UV-threshold voltage high level	VBB rising (Note 8)	4	-	5	V
VBB_UV_L	UV-threshold voltage low level	VBB falling (Note 8)	3.8	-	4.7	V

8. Below 5 V on VBB in normal mode, the LIN bus will either stay recessive or comply with the voltage level specifications and transition time pir togg2.85) but p68.951 6(BB)Tnot gu68.nte0.044 ..09 lt754 .737 77.72I_3.60 sta04 ref59.754 340ef044 77.7223.988.743 refBT5 3017V

Table 5. ELECTRICAL CHARACTERISTICS 6 V ≤ V _{BB} ≤ 18 V, −40°C ≤ Tj ≤ 150°C; unless otherwise specified; R _{L(LIN-VBB)} =	
500 Ω, unless otherwise specified. Typical values are given at $V(V_{BB}) = 12$ V and $T_J = 25$ °C, unless otherwise specified.	

				•		
Symbol	Parameter	Conditions	Min	Тур	Max	Unit
MODE TRANSITIO	NS AND TIMEOUTS					
T_OC_del	Overcurrent Shut–Down Delay Time on OUTx pins	OUTx shorted to VBB	3	15	50	μs
T_OL_det	Open Load Detection Time OUT4, OUT8		30	115	200	μs
THERMAL PROTE	CTION					
T _{jsd}	Global Thermal shut-down level	Guaranteed by design and prototype evaluations, not tested in production	150	175	190	°C
T _{jsd_hys_global}	Thermal shut-down hysteresis	Guaranteed by design and prototype	1 -	-	-	-

Guaranteed by design and prototype evaluations, not tested in production Thermal shut-down hysteresis

Table 5. ELECTRICAL CHARACTERISTICS 6 V \leq V _{BB} \leq 18 V, -40°C \leq Tj \leq 150°C; unless otherwise specified; R _{L(LIN-VBB)} =
500 Ω, unless otherwise specified. Typical values are given at V(V _{BB}) = 12 V and T _J = 25°C, unless otherwise specified.

SymbolParameterConditionsMinTypMaxUnitLIN TRANSMITTER DYNAMIC CHARACTERISTICS (The following bus loads are considered: $BL1 = 1 \text{ k}\Omega / 1 \text{ nF}$; $BL2 = 660 \Omega / 6.8 \text{ nF}$;
 $BL3 = 500 \Omega / 10 \text{ nF}$)(Resistor = Vbat to LIN, Capacitor = LIN to GND)MinTypMaxUnit

D1	Duty Cycle 1 = t _{BUS_rec(min)} / (2 x TBit) (see Figure 3)	$\begin{array}{l} \text{TH}_{\text{Rec}(\text{max})} = 0.744 \text{ x VBB}, \\ \text{TH}_{\text{Dom}(\text{max})} = 0.581 \text{ x VBB}, \\ \text{Tbit} = 50 \ \mu\text{s}, \\ \text{VBB} = 7 \ \text{V} \text{ to } 18 \ \text{V}, \ \text{BL1}, \ \text{BL2}, \ \text{BL3} \end{array}$	0.396		0.5	
D2	Duty Cycle 2 = t _{BUS_rec(max)} / (2 x TBit) (see Figure 3)	$\begin{array}{l} TH_{Rec(min)} = 0.422 \ x \ VBB, \\ TH_{Dom(min)} = 0.284 \ x \ VBB, \\ Tbit = 50 \ \mu s, \\ VBB = 7.6 \ V \ to \ 18 \ V, \ BL1, \ BL2, \ BL3 \end{array}$	0.5		0.581	
D3	Duty Cycle 3 = t _{BUS_rec(min)} / (2 x TBit) (see Figure 3)	$\begin{array}{l} TH_{Rec(max)} = 0.788 \ x \ VBB, \\ TH_{Dom(max)} = 0.616 \ x \ VBB, \\ Tbit = 96 \ \mu s, \\ VBB = 7 \ V \ to \ 18 \ V \ BL1, \ BL2, \ BL3 \end{array}$	0.417		0.5	
D4	Duty Cycle 4 = t _{BUS_rec(max)} / (2 x TBit) (see Figure 3)	$\begin{array}{l} TH_{Rec(min)} = 0.389 \ x \ VBB, \\ TH_{Dom(min)} = 0.251 \ x \ VBB, \\ Tbit = 96 \ \mu s \\ VBB = 7.6 \ V \ to \ 18 \ V, \ BL1, \ BL2, \ BL3 \end{array}$	0.5		0.59	
T_fall_LIN	LIN falling edge (see Figure 4) BL1,BL2	VBB = 12 V; BL1, BL2 40% to 60% measurements extrapolated to 0% to 100%			22.5	μs
T_rise_LIN	LIN rising edge (see Figure 4) BL1,BL2	VBB = 12 V; BL1, BL2 40% to 60% measurements extrapolated to 0% to 100%			22.5	μs
T_sym_LIN	LIN slope symmetry BL1,BL2	Normal mode VBB = 12 V; BL1, BL2	-6	0	6	μs
T_fall_LIN_L3	LIN falling edge (see Figure 4) BL3	VBB = 12 V; BL3 40% to 60% measurements extrapolated to 0% to 100%	-		-	•

 $t_{\text{BUS_dom(min)}}$

Functional Description

The NCV7748 is an automotive eight channel low side driver providing drive capability up to 0.75 A or 0.6 A per channel depending on channel selection. Output control is via a LIN bus with an optimized LIN command set allowing high flexibility while still maintaining compliance to the SAE J2602 LIN specification. Use of a virtual LIN node concept allows driving up to 32 channels with one LIN command.

Each output driver includes an output clamp for inductive loads.

All output drivers have overcurrent detection implemented. Select low side driver(s) offer additional fault reporting of open load (or short to ground) and local over temperature conditions which allows connection to a wiring harness outside of the module.

Operating Modes

The NCV7748 integrated circuit has <u>two BASIC modes</u> of operation:

- 1. Normal mode Fully functional.
- 2. <u>Sleep mode</u> Low quiescent current. Device is inactive waiting for LIN bus wake up.

The principal operating modes of the NCV7748 are shown in Figure 7.

There are also additional transition modes of operation: Un powered, INIT, Reset and Undervoltage mode. Global thermal shutdown mode is shown in Figure 8. Within normal mode as shown in Figure 10, the device can transition into overcurrent mode (driver 1 to 3 and 5 to 7) or as shown in Figure 9 overcurrent/local thermal shutdown mode on drivers four and eight.

Un Powered and INIT Mode

The device is held in power on reset when VBB is below the VBB_POR level. All outputs are in HiZ state and LIN is disabled. Note: While LIN is disabled the weak pull up is activated (See ILIN_off_dom_slp parameter)

As soon as the VBB main supply exceeds the power on reset level, the device enters the INIT Mode and begins an initialization sequence. ERR.0 bit is set high after the power on reset. (See Table 15)

All the registers are set to their default values.

The device is reading the configuration resistors on the NAD and CONF pins. (Details of the device configuration based on NAD and CONF pins are in the Supported LIN commands chapter)

If the NAD and CONF pins are successfully read, the device enters normal mode. Otherwise (e.g. NAD, CONF pins shorted to ground, open or short between these pins) the device will enter Sleep mode. LIN is disabled during INIT mode and all OUTx outputs are in HiZ state.

The device stays in the INIT mode for a maximum time of T_init.

Sleep Mode

Sleep mode is entered from Normal mode or Undervoltage mode if there is no activity on the bus for longer time than limited by the T_go_to_sleep parameter. No activity is defined as no transition from recessive to dominant.

Another way to enter the Sleep mode from the Normal mode is successful reception of the Go to sleep command. (See Supported LIN commands chapter).

In Sleep Mode all outputs are off, the device is in Wake up mode and there is no change in the state of the ERR bits.

If a valid LIN wake up (See T_LIN_wake) is detected, the Sleep mode transitions to INIT mode.

Internal LIN Transceiver Modes

Within the NCV7748, the LIN transceiver has three internal modes of operation, normal active mode (On), Disabled mode (OFF), and within the NCV7748 sleep mode the LIN transceiver is powered down waiting to be woken up and is said to be in Wake Up Mode.

LIN is active (On) during Normal Mode.

LIN is disabled (Off) during Un Powered mode, Reset, and INIT mode.

In Sleep Mode, the internal LIN transceiver is in Wake Up Mode waiting for a dominant signal (low) with a minimum continuous duration of T_LIN_wake. A remote wake up occurs after T_LIN_wake and the return of LIN to a high (60% VS) (Figure 5).

When a

During normal operation, the open circuit impedance (Roc) is zero ohms (Figure 6). This sets the voltage on OUT4 or OUT8 to VS volts. As long as VS is above V_th_open no open circuit fault will be recognized. The voltage appearing on OUT4 or OUT8 is a result of VS and the voltage drop across Roc realized by the current flow created by I_th_open.

The NCV7748 voltage level trip points are referenced to ground. The threshold range is between 1.0 V and 2.5 V.

With a nominal battery voltage (VS) of 14 V, the resultant worst case thresholds of detection are as follows.

 $\frac{(\mathsf{VS}-\mathsf{OpenLoadDetectionThresholdvoltage})}{\mathsf{OpenLoadDiagnosticSinkCurrent}} = \begin{array}{l} \mathsf{OpenLoad}\\ \mathsf{Impedance} \end{array}$

(14 V - 2.5 V)140 µA

Dual Reporting APPINFO 01000b

Both Local Thermal Shutdown and Overcurrent Detection are reported in the APPINFO register (01000b) as an OR'd bit. Either or both of these conditions will be reported as a "1". (See Table 17)

Local Thermal Shutdown

Output 4 and 8 have local thermal shutdown sensors protecting the drivers. If OUT4/8 thermal shutdown threshold (Tjsd_OUT4,8) is reached, the corresponding driver is latched off and fault flags are set. The local thermal shutdown on OUT4 and OUT8 is latched in the OUT Status readout register (See Table 16) as well as in the APPINFO register. (See Table 17, APPINFO.3 bit).

The only way to leave the overcurrent / local thermal shutdown state and at the same time clear out the output status and APPINFO register is to command OFF the affected driver.

The overcurrent /local thermal shutdown info in the APPINFO register is only kept high if Global thermal shutdown is not activated. Global thermal shutdown has higher priority and masks APPINFO.3 to low as long as Global thermal shutdown is active. This is to avoid having both APPINFO.2 and APPINFO.3 bits high at the same time as this combination is reserved in some systems for ECU fault diagnostics.

Overcurrent Detection

All eight drivers have overcurrent detection implemented. Drivers are latched off if the load current exceeds I_det_OUTx level for the time longer than T_OC_del (see Figures 9 and 10).

The overcurrent status on OUT4 and OUT8 is latched in the OUT Status readout register (See Table 16) as well as in the APPINFO register. (See Table 17, APPINFO.3 bit). On OUT1 3 and OUT5 7 the overcurrent status is latched in the OUT status register but not in the APPINFO register.

The only way to leave the overcurrent / local thermal shutdown state and at the same time clear out the output status and APPINFO register is to command OFF the affected driver.

The overcurrent / local thermal shutdown info in the APPINFO register is only kept high if Global thermal shutdown is not activated. Global thermal shutdown has higher priority and masks APPINFO.3 to low as long as Global thermal shutdown is active. This is to avoid having both APPINFO.2 and APPINFO.3 bits high at the same time as this combination is reserved in some systems for ECU fault diagnostics.

Global Thermal Shutdown Mode

The device junction temperature is monitored in order to avoid permanent degradation or damage of the chip. Junction temperature exceeding the Shutdown level T_{J_SD} puts the chip into Thermal Shutdown mode. (See Figure 8)

In Global thermal Shutdown mode, all OUTx drivers are deactivated, LIN transceiver remains active. APPINFO.2 bit is set high and APPINFO.3 as mentioned above is

masked to low (00100b). The mode is automatically exited if the junction cools down below the T_{J_SD} minus hysteresis $T_{jsd_hys_global}$ threshold. APPINFO.2 is not latched and is cleared when mode is exited.

Undervoltage Mode

If the voltage on the battery pin VBB goes below VBB_UV_L, the device enters Undervoltage mode. LIN is disabled (both transmitter and receiver) but drivers' status remains unchanged.

The device returns to Normal mode if the battery voltage goes above VBB_UV_H level. Un powered mode is entered if VBB voltage drops below VBB_POR_L level.

As LIN timeout counter is running during the Undervoltage mode as well, the device is suspended to the Sleep mode when the timeout of T_go_to_sleep elapses.

Error Field (ERR [2:0]) & APPINFO (J2602 STATUS BYTE)

The NCV7748 uses a 3 bit error field (ERR[2:0]) as specified in SAE J2602 for LIN Protocol Error reporting and

Global Thermal Shutdown OUT1-8: Off LIN Physical Layer

NCV7748 integrates an on chip LIN transceiver interface between the physical LIN bus and the integrated LIN protocol controller. (See Supported LIN Commands)

This LIN physical layer is compatible to LIN2.x and J2602 specifications.

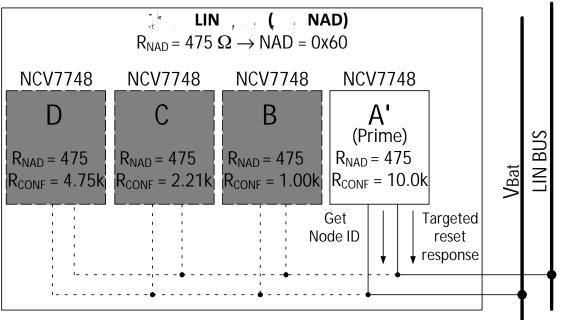


Figure 11. Virtual LIN Node Concept

Table 9. SUMMARY OF SUPPORTED LIN COMMANDS

rame Type	Description	Data Length	PID[7:0]	Spec
utput Control	Sets all outputs in one virtual node	8	Depends on NAD (See Table 12)	N/A
	Reads identity of prime device in virtual node. (In frame slave Response)	8	Depends on NAD (See Table 23)	N/A
	Reads diagnostics of one device (LS driver). (In frame slave Response)	8	Depends on CONF (See Table 7) and NAD (See Table 18)	N/A
	Re–initialization of one virtual node. This includes all devices on the virtual node.	8	0x3C	J2602–

ï

OUTPUT CONTROL FRAME Table 10. OUTPUT CONTROL COMMAND

Byte Content

GET STATUS AND DIAGNOSTIC

Table 14. GET STATUS REQUEST

				_	_	Struc	cture	_	_	
	Byte	Content	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Master	0	Identifier		PID						
	1	Data 1	ERR2	ERR2 ERR1 ERR0 APPINFO						
	2	Data 2	OUT4 S	STATUS	OUT3 S	TATUS	S OUT2 STATUS OUT1 STATUS			STATUS
	3	Data 3	OUT8 S	STATUS	OUT7 S	OUT7 STATUS OUT6 STATUS OUT			OUT5 S	STATUS
	4	Data 4	0x00 (NULL)							
Slave	5	Data 5				0x00 (NULL)			
	6	Data 6				0x00 (NULL)			
	7	Data 7	0x00 (NULL)							
	8	Data 8	0x00 (NULL)							
	9	Checksum				Enhanced	Checksum			

GET STATUS COMMAND

The Get Status Request frame (see Table 14) is issued by the master to receive application specific diagnostics.

The error bits decrypted from Data1 of this command are as per SA EJ2602 in Table 15.

The ERR.[2:0] bits are cleared by readout. That means every command response containing ERR.[2:0] clears the error register.

Every driver status (Data 2 and 3) is stored in two bits of information. Only drivers OUT4 and OUT8 allow readout of open load fault (OL) and local TSD. All drivers flag overcurrent info. (See Table 16)

Table 17 describes APPINFO register content.

Table 15. J2602 1 ERROR FIELD

ERR2	ERR1	ERR0	Error States	Priority
0	0	0	No Error	0 (lowest)
0	0	1	Reset	1
0	1	0	Reserved	2
0	1	1	Reserved	3
1	0	0	Data Error	4
1	0	1	Data Checksum	5
1	1	0	Byte Field Framing Error	6
1	1	1	ID Parity Error	7 (highest)

Table 16. OUT STATUS READOUT

STATUS	Output Command	Description	Note
00b	OFF	Open Load Fault (non–latching)	Only OUT4/8
01b	OFF	Per setting or active Global TSD	All OUTx, Default after reset
10b	ON	Per setting	All OUTx
11b	ON	Latched OFF from ON state due to TSD/OC	TSD / OUT4/8; OC on all OUTx

Table 17. APPINFO REGISTER

APPINFO	Error States			
00000b	Defaualt – No Failure to Report			
	ailure to Report			

Example of the Get Status command Reference Figure 12 for bit sequencing.

ID = 0x02 [Table ID] => PID = 0x42 [LIN2.2]
(Reference Table 19)
Data1 = 0x08 => OUT4,OUT8 TSD / OC
(0b 000 01000)
Data2 = 0x59 => OUT1 : Off (01)
(0b 01 01 10 01) OUT2 : ON (10)
OUT3 : Off (01)
OUT4 : Off (01)
Data3 = 0xDA => OUT5 : ON (10)
(0b 11 01 10 10) OUT6 : ON (10)
OUT7 : Off (01)
OUT8 : Off (11)Latched Off due to TSD/OC

Note the placement of the bits for LSB and MSB! It is not intuitive. LSB is sent first.

Table 20. GET STATUS EXAMPLE HEX RESPONSE

Status	Hex Response			OUT N	umber		
			1	2	3	4	
OUT1-4	0x59	LSB	10	01	10	10	MSB
OUT5-8	0xDA	LSB	01	01	10	11	MSB

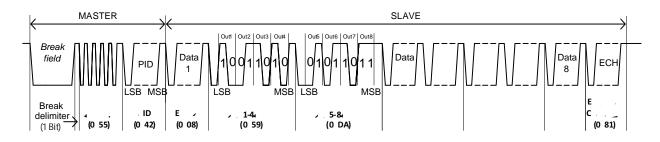


Table 24 shows get status ID to NAD and node position within virtual node in context of the SAEJ2602 spec. Table 24. GET NODE ID COMMAND MAPPING LINKED TO SAEJ2602 SPEC

NAD	Message ID	PID	NAD	Message ID	PID	NAD	Message ID	PID	NAD	Message ID	PID
\$60	\$0	0x80	\$64	\$10	0x50	\$68	\$20	0x20	\$6C	\$30	0xF0
	\$1		1	\$11			\$21			\$31	
	\$2		1	\$12			\$22			\$32	
	\$3		1	\$13			\$23			\$33	
	\$4		1	\$14			\$24			\$34	
	\$5		1	\$15			\$25			\$35	
	\$6		1	\$16			\$26			\$36	
	\$7		1	\$17			\$27			\$37	
\$62	\$8	0x08	\$66	\$18	0xD8	\$6A	\$28	0xA8	\$6E	No	
	\$9		1	\$19			\$29			Message IDs defined	
	\$0A		1	\$1A			\$2A				
	\$0B		1	\$1B			\$2B				
	\$0C		1	\$1C			\$2C		\$6F	No	
	\$0D		1	\$1D		1	\$2D			Message IDs defined	
	\$0E		1	\$1E		1	\$2E		1		
	\$0F		1	\$1F		1	\$2F				

READ BY IDENTIFIER COMMAND

Table 25. READ BY IDENTIFIER

						Struc	cture			
	Byte	Content	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	0	Identifier	0x00 (0x00 (Parity) 0x3C (ID)						
	1	Data 1			NA	D or 0x7F (Wildcard NA	D)		
	2	Data 2		0x06 (PCI)						
	3	Data 3		0xB2 (SID)						
Maataa	4	Data 4			Node Identif	ier (see Nod	e Identificatio	on Table 28)		
Master	5	Data 5		Su	upplier ID LS	B (0x24) or 0	xFF (Wildca	rd Supplier I	D)	
	6	Data 6		Su	pplier ID MS	B (0x00) or (0x7F (Wildca	ard Supplier	ID)	
	7	Data 7	Function ID LSB (0x48/0x44) or 0xFF (Wildcard Function ID)							
	8	Data 8	Function ID MSB (0x60) or 0xFF (Wildcard Function ID)							
	9	Checksum		Classic Checksum						

Table 26. POSITIVE RESPONSE FOR READ BY IDENTIFIER

						Struc	cture			
	Byte	Content	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Master	0	Identifier	0x01 (0x01 (Parity) 0x3D (ID)						
	1	Data 1				NA	D			
	2	Data 2		0x06 (PCI)						
	3	Data 3		0xF2 (RSID)						
	4	Data 4				Supplier ID	LSB (0x24)			
Slave	5	Data 5				Supplier ID	MSB (0x00)			
	6	Data 6			Fu	Inction ID LS	B (0x48/0x4	4)		
	7	Data 7	Function ID MSB (0x60)							
	8	Data 8	Silicon Version							
	9	Checksum				Classic C	hecksum			

Table 27. NEGATIVE RESPONSE FOR READ BY IDENTIFIER

						Struc	cture			
	Byte	Content	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Master	0	Identifier	0x01 (0x01 (Parity) 0x3D (ID)						
	1	Data 1				NA	١D			
	2	Data 2		0x03 (PCI)						
	3	Data 3		0x7F (RSID)						
	4	Data 4		0xB2 (Requested SID)						
Slave	5	Data 5				0x12 (Err	or Code)			
	6	Data 6				0x	FF			
	7	Data 7	0xFF							
	8	Data 8	0xFF							
	9	Checksum				Classic C	hecksum			

TARGETED RESET COMMAND

Table 30. TARGETED RESET REQUEST COMMAND

						Struc	cture			
	Byte	Content	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	0	Identifier	0x00 (0x00 (Parity) 0x3C (ID)						
	1	Data 1				NA	٨D			
	2	Data 2		0x01						
	3	Data 3		0xB5						
Maatan	4	Data 4				0x	FF			
Master	5	Data 5				0x	FF			
	6	Data 6				0x	FF			
	7	Data 7	0xFF							
	8	Data 8	0xFF							
	9	Checksum		Classic Checksum						

Table 31. TARGETED RESET POSITIVE RESPONSE

						Struc	cture			
	Byte	Content	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Master	0	Identifier	0x01 (l	0x01 (Parity) 0x3D (ID)						
	1	Data 1		NAD						
	2	Data 2		0x06						
	3	Data 3		0xF5						
	4	Data 4		Supplier ID LSB (0x24)						
Slave	5	Data 5				Supplier ID	MSB (0x00)			
	6	Data 6			Fu	inction ID LS	B (0x48/0x4	4)		
	7	Data 7		Function ID MSB (0x60)						
	8	Data 8	Silicon Version							
	9	Checksum		Classic Checksum						

Targeted reset (See Table 30) puts all the outputs into the off state (Table 11, OUTx Off), resets the error flags ERR.1,2 and sets the ERR.0 = 1 in the ERR status byte (Table 15).

Targeted reset puts all outputs for all devices in a virtual node in the off state.

The node giving positive response (prime node) within the virtual node is defined by Table 31.

GO TO SLEEP COMMAND

Table 32. GO TO SLEEP COMMAND

						Struc	cture			
	Byte	Content	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	0	Identifier	0x00 (0x00 (Parity) 0x3C (ID)						
	1	Data 1				0x	00			
	2	Data 2		0xXX						
	3	Data 3		0xXX						
Martin	4	Data 4				0x)	XX			
Master	5	Data 5				0x)	XX			
	6	Data 6				0x)	XX			
	7	Data 7	0xXX							
	8	Data 8	0xXX							
	9	Checksum		Classic Checksum						

The Go to sleep command (see Table 32) deactivates all the drivers and puts all the slave nodes connected to the LIN bus into the Sleep mode. In 0xXX, XX stands for don't care.

Output Driver Fault Handling

A summary of output driver device performance under fault conditions is summarized below. This includes reporting to the APPINFO register, the driver condition both during and after fault conditions, and what is required to clear reported faults.

Table 33. FAULT HANDLING

Fault	APPINFO Register	OUTPUT Register	Drivers Condition during Fault	Drivers Condition after Parameters within Specified Limits	Output Register clearing Requirement	APPINFO Register Clearing Requirement
Open load (OUT4 and OUT8)	Not signaled.	Signaled in OFF Mode	Per setting	Driver in Normal operation	Load re-connected	NA
Overcurrent	Latched	latched	-	-	-	

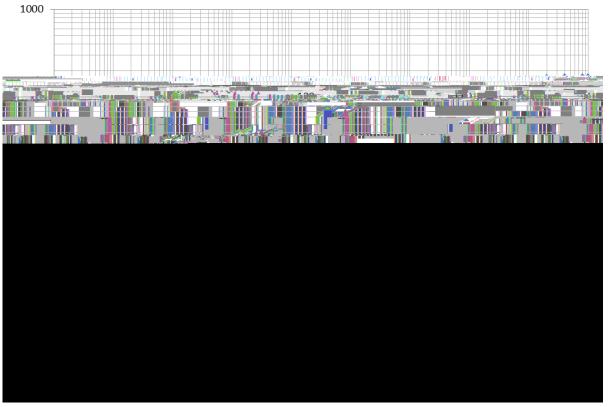


Figure 15. SOIC 14 Single Pulse Heating Curve (1s0p)

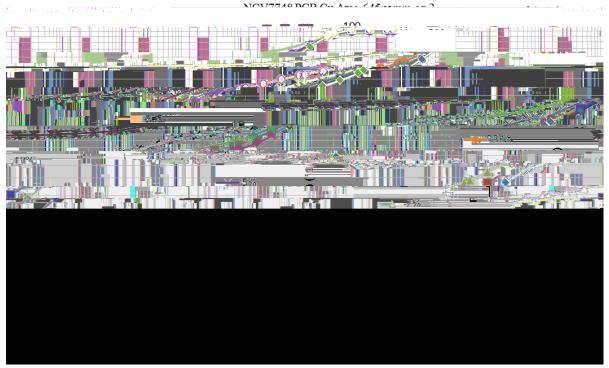


Figure 16. SOIC 14 Thermal Duty Cycle Curve on 645 mm2 Spreader Test Board (1s0p)

2S2P Thermal Performance

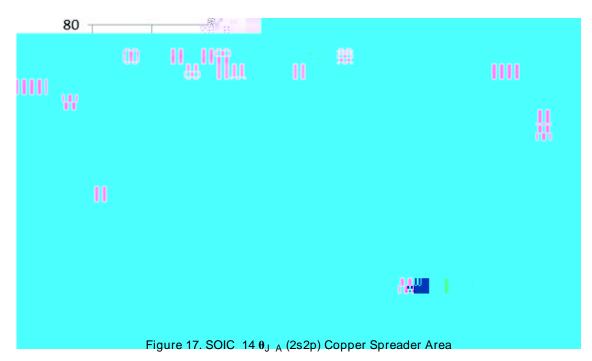




Figure 18. SOIC 14 Single Pulse Heating Curve (2s2p)

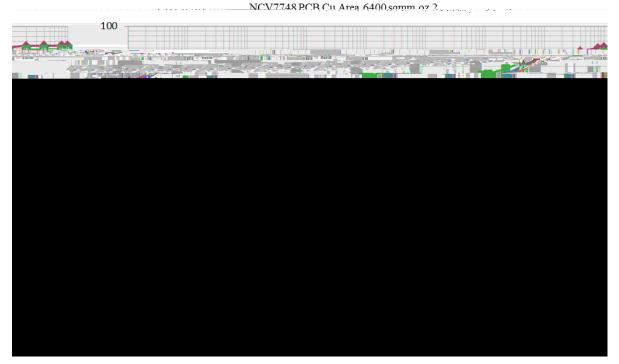


Figure 19. SOIC 14 Thermal Duty Cycle Curve on 645 mm2 Spreader Test Board (2s2p)

ORDERING INFORMATION

Device Order Number	Number of Channels	Package	Shipping [†]
NCV7748D2R2G	8	SOIC-14 (Pb-Free)	2500 / Tape & Reel

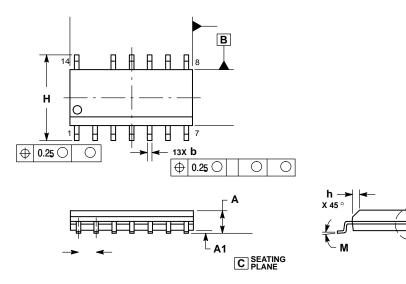
+For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.



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- NOTES:
 1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
 2. CONTROLLING DIMENSION: MILLIMETERS.
 3. DIMENSION & DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF AT MAXIMUM MATERIAL CONDITION.
 4. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSIONS.
 5. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.

SIDE.

GENERIC **MARKING DIAGRAM***

14	A	A	A	A	A	A	Æ
		xx	хх	хх	хх	XG	
	0	A	٩W	LY۱	٨٧	/	
1	H	Н	Н	Н	Н	H	Ч

XXXXX	= Specific Device Code
A	= Assembly Location
WL	= Wafer Lot
Y	= Year
WW	= Work Week
G	= Pb-Free Package

STYLES ON PAGE 2

DATE 03 FEB 2016

STYLE 7: PIN 1. ANODE/CATHODE 2. COMMON ANODE 3. COMMON CATHODE 4. ANODE/CATHODE 5. ANODE/CATHODE

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