

C 7708

The NCV7708F is a fully protected Hex Half Bridge Driver designed specifically for automotive and industrial motion control applications. The six low and high side drivers are freely configurable and can be controlled separately. This allows for high side, low side, and H-Bridge control. H-Bridge control provides forward, reverse, brake, and high impedance states. The drivers are controlled via a standard SPI interface.

Features

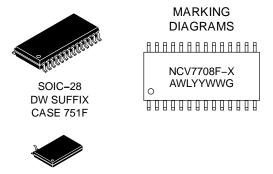
- Ultra Low Quiescent Current Sleep Mode
- Six Independent High-Side and Six independent Low-Side Drivers
- Integrated Freewheeling Protection (LS and HS)
- Internal Upper and Lower Clamp Diodes
- Configurable as H–Bridge Drivers
- $R_{DS(on)} = 0.6 \Omega$ (typ)
- 5 MHz SPI Control
- SPI Valid Frame Detection
- Compliance with 5 V and 3.3 V Systems
- Overvoltage Lockout
- Undervoltage Lockout
- Fault Reporting
- Current Limit
- Overtemperature Protection
- Internally Fused Lead in SOIC-28
- SSOP-24 NB EPAD
- These are Pb–Free Devices

Typical Applications

- Automotive
- Industrial
- DC Motor Management



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- = Optional Wafer Fab Indicator Х А
 - = Assembly Location
- WL = Wafer Lot
- = Year YΥ

G

- = Work Week WW
 - = Pb-Free Package

Device	Package	Shipping [†]
NCV7708FDWR2G*	SOIC-28W (Pb-Free)	1000 / Tape & Reel

+For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

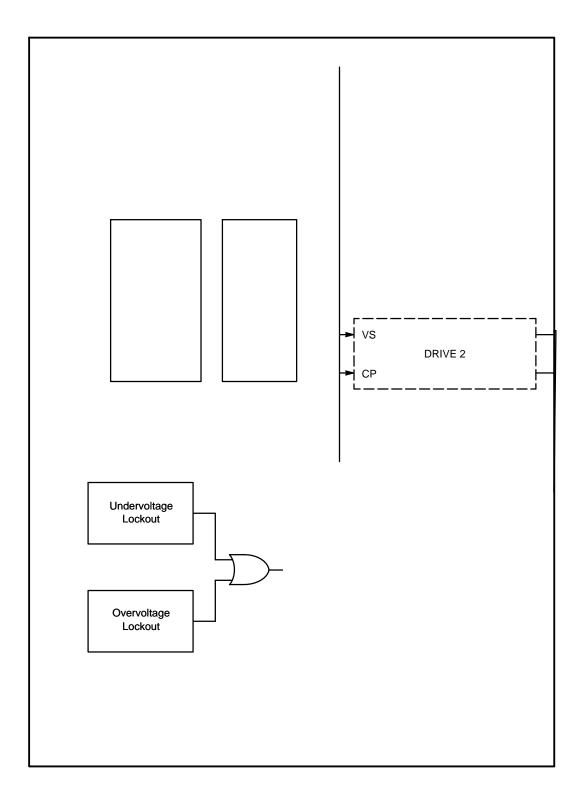
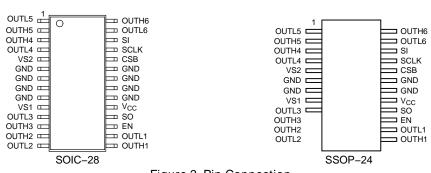


Figure 1. Block Diagram





MAXIMUM RATINGS

Rating	Value	Unit
Power Supply Voltage (VS1, VS2) (DC) (AC), t < 500 ms, lvsx > -2 A	-0.3 to 40 -1.0	V
Output Pin OUTHx (DC) (AC – inductive clamping)	-0.3 to 40 -8.0	V
Output Pin OUTLx (DC) (AC), t < 500 ms, IOUTLx > -2 A (AC Inductive Clamping)	-0.3 to 36 -1.0 45	V
Pin Voltage (Logic Input pins, SI, SCLK, CSB, SO, EN, V_{CC})	-0.3 to 5.5	V
Output Current (OUTL1, OUTL2, OUTL3, OUTL4, OUTL5, OUTL6, OUTH1, OUTH2, OUTH3, OUTH4, OUTH5, OUTH6) (DC) Vds = 12 V (DC) Vds = 20 V	–1.5 to 1.5 –0.7 to 0.7	A
(DC) Vds = 40 V (AC) Vds = 12 V, (50 ms pulse, 1 s period) (AC) Vds = 20 V, (50 ms pulse, 1 s period) (AC) Vds = 40 V, (50 ms pulse, 1 s period)	-0.25 to 0.25 -2.0 to 2.0 -0.9 to 0.9 -0.3 to 0.3	

Electrostatic Discharge, Human Body Model, VS1, VS2, OUTx (Note 1)

RECOMMENDED OPERATING CONDITIONS

		Va	Value	
Rating	Symbol	Min	Max	Unit
Digital Supply Input Voltage (V _{CC})	V _{CCmax}	3.15	5.25	V
Battery Supply Input Voltage (V _S)	V _{Smax}	5.5	28	V
DC Output Current (I(OUTLx), I(OUTHx))	DC _{max}	-	0.5	А
Junction Temperature	TJ	-40	150	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

ELECTRICAL CHARACTERISTICS (-40°C < $T_{\rm J}$ < 150°

ELECTRICAL CHARACTERISTICS (-40°C < T_J < 150°C, 5.5 V < VSx < 40 V, 3.15 V < V_{CC} < 5.25 V, EN = V_{CC}, unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min	Тур	Max	Unit
OUTPUTS						
Sink Leakage Current	I _{snk}	$\begin{array}{l} \text{OUTL}(1-6) = 34 \text{ V}, \\ \text{V}_{\text{CC}} = 5 \text{ V} \\ \text{OUTL}(1-6) = 34 \text{ V}, \\ \text{V}_{\text{CC}} = 5 \text{ V}, \text{ T} = 25^{\circ}\text{C} \end{array}$	-	-	5.0 1.0	μΑ
Power Transistor Body Diode Forward Voltage	V _{bd_fwd}	I _F = 500 mA	-	0.9	1.3	V
High-Side Clamping Voltage (Note 7)	V _{clp_hs}	I _(OUTHx) =		-	-	

ELECTRICAL CHARACTERISTICS

(-40°C < T_J < 150°C, 5.5 V < VSx < 40 V, 3.15 V < V_{CC} < 5.25 V, EN = V_{CC}, unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min	Тур	Max	Unit
TIMING SPECIFICATIONS						
Low Side Turn Off Time	t _{lsoff}	Vs = 13.2 V, R_{load} = 25 Ω	-	2.0	5.0	μS
High Side Rise Time	t _{hsr}	Vs = 13.2 V, R _{load} = 25 Ω	-	4.0	8.0	μS
High Side Fall Time	t _{hsf}	Vs = 13.2 V, R_{load} = 25 Ω	-	2.0	3.0	μS
Low Side Rise Time	t _{lsr}	Vs = 13.2 V, R_{load} = 25 Ω	-	1.0	2.0	μS
Low Side Fall Time	t _{lsf}	Vs = 13.2 V, R_{load} = 25 Ω	-	1.0	3.0	μS
Non-Overlap Time	t _{hs} OfflsOn	High Side Turn Off To Low Side Turn On	1.5	-	-	μS
Non-Overlap Time	t _{lsOffhsOn}	Low Side Turn Off To High Side Turn On	1.5	-	-	μs

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

5. For temperatures above 85°C, refer to graphs for VSx and V_{CC} Sleep Current vs. Temperature on page 17.

6. Thermal characteristics are not subject to production test.

Refer to "Typical High–Side Negative Clamp Voltage" graph on page 17.
Current limit is active with and without overcurrent detection.

9. Not production tested.

ELECTRICAL CHARACTERISTICS

 $(-40^{\circ}C < T_J < 150^{\circ}C, 5.5 \text{ V} < \text{VSx} < 40 \text{ V}, \text{EN} = \text{V}_{CC} = 5 \text{ V}, \text{ unless otherwise specified})$

Characteristic Conditions Symbol Min Typ	Max	Unit
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SERIAL PERIPHERAL INTERFACE (V_{CC} = 5 V)

- 1 01	, ,					
SCLK Frequency		f _{SCLK}	_	-	5.0	MHz
SCLK Clock Period	V _{CC} = 5 V V _{CC} = 3.3 V	t _{SCLK}	200 500			ns
SCLK High Time		t _{CLKH}	85	-	-	ns
SCLK Low Time		t _{CLKL}	85	-	-	ns
SCLK Setup Time		t _{CLKSU1} t _{CLKSU2}	85 85	-		ns

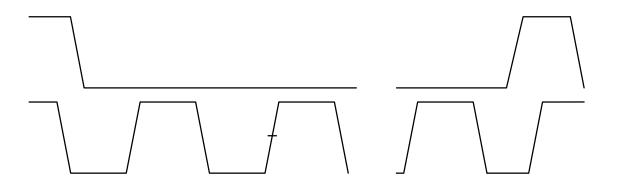


Figure 3. SPI Timing Diagram

SPI Communication

Standard 16-bit communication has been implemented for the communication of this IC to turn drivers on and off, and to report faults. (Reference the SPI Communication Frame Format Diagram). The LSB (Least Significant Bit) is clocked in first.

For SPI communication, the device must first be enabled (EN = high). The SPI inputs are TTL compatible and the SO output high level is defined by the applied VCC. The active-low CSB input has a pull–up resistor. SPI communication is active when CSB is low. Providing a pull-up resistor insures the communication bus is not active should the communication link between the microcontroller and NCV7708F become open. SCLK and SI have pull–down resistors. This provides known states when the SPI is not active.

Communication is implemented as follows:

- 1. CSB goes low to allow serial data transfer.
- 2. A 16 bit word is clocked (SCLK) into the SI (serial input) pin. The SI input signal is latched on the falling edge of SCLK.
- 3. Current SO data is simultaneously shifted out on every rising edge of SCLK starting with the LSB (TW).
- 4. CSB goes high to transfer the clocked in information to the data registers.(Note: SO is tristate when CSB is high.)
- 5. The SI data will be accepted when a valid SPI frame is detected. A valid SPI frame consists of the above conditions and a complete set of multiples of 16 bit words. Invalid frames are ignored with previous input data intact.

Figure 4. SPI Communication Frame Format

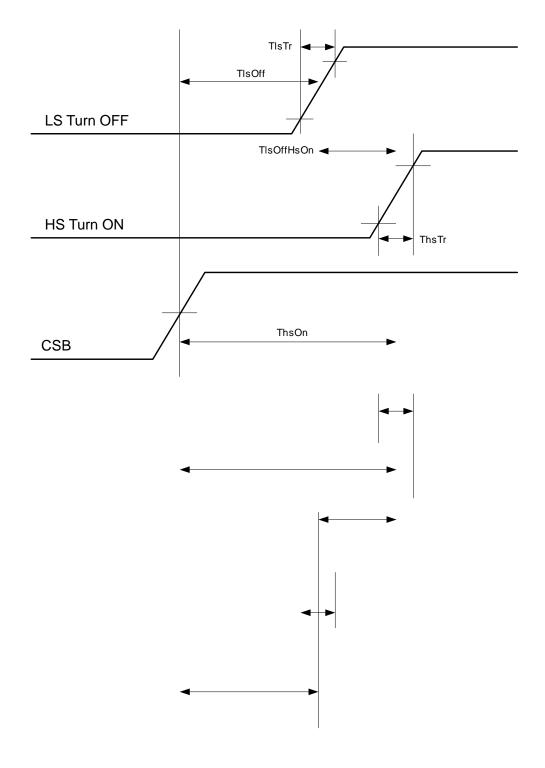
The table below defines the programming bits and diagnostic bits. Fault information is sequentially clocked out the SO pin of the NCV7708F as programming information is clocked into the SI pin of the device. Daisy chain

	Input Data							
Bit #	Bit Description	Bit Status						
15	Overvoltage Lock Out Control	0 = Disable						
	(OVLO)	1 = Enable						
14	Under Load Detection Shut	0 = Disable						
	Down Control (ULD)	1 = Enable						
13	Overcurrent Detection Shut	0 = 200 μsec						
	Down Control (OCD)	1 = 25 μsec						
12	OUTH6	0 = Off						
		1 = On						
11	OUTL6	0 = Off						
		1 = On						
10	OUTH5	0 = Off						
		1 = On						
9	OUTL5	0 = Off						
		1 = On						
8	OUTH4	0 = Off						
		1 = On						
7	OUTL4	0 = Off						
		1 = On						
6	OUTH3	0 = Off						
		1 = On						
5	OUTL3	0 = Off						
		1 = On						
4	OUTH2	0 = Off						
		1 = On						
3	OUTL2	0 = Off						
		1 = On						
2	OUTH1	0 = Off						
		1 = On						
1	OUTL1	0 = Off						
		1 = On						
0	Status Register Reset (SRR)	0 = No Reset						
		1 = Reset						

communication between SPI compatible IC's is possible by connection of the serial output pin (SO) to the input of the sequential IC (SI).

	Output Data							
Bit #	Bit Description	Bit Status						
15	Power Supply Fail Signal	0 = No Fault						
	(OVLO or UVLO = PSF)	1 = Fault						
14	Under Load Detect Signal	0 = No Fault						
	(ULD)	1 = Fault						
13	Over Load Detect Signal	0 = No Fault						
	(OLD)	1 = Fault						
12	OUTH6*	0 = Off						
		1 = On						
11	OUTL6*	0 = Off						
		1 = On						
10	OUTH5*	0 = Off						
		1 = On						
9	OUTL5*	0 = Off						
		1 = On						
8	OUTH4*	0 = Off						
		1 = On						
7	OUTL4*	0 = Off						
		1 = On						
6	OUTH3*	0 = Off						
		1 = On						
5	OUTL3*	0 = Off						
		1 = On						
4	OUTH2*	0 = Off						

CHARACTERISTIC TIMING DIAGRAMS



Overcurrent Detection Shut Down Control Timer

There are two protection mechanisms for output current, overcurrent and current limit.

- 1. Current limit Always active with a typical threshold of 3 A.
- 2. Overcurrent Detection Selectable shutdown time via Bit 13 with a typical threshold of 1.45 A.

Figure 6 shows the typical performance of a part which has exceeded the 1.45 A Overcurrent Detection threshold and started the shutdown control timer. When Bit 13 = 1, the shutdown time is 25 µsec. When Bit 13 = 0, the shutdown time is 200 µsec.

Once an Overcurrent Shutdown Delay Time event has been detected by the NCV7708F, the timer setting cannot be interrupted by an attempted change via a SPI command of Bit 13.

Input Bit 13	Overcurrent Shutdown Delay Time
0	200 µsec
1	25 µsec

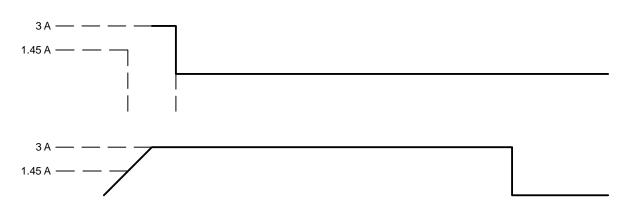


Figure 6. Output Current Shutdown Control

Under Load Detection

The under-load detection is accomplished by monitoring the current from each output driver. A minimum load current (this is the maximum detection threshold) is required when the drivers are turned on. If the under-load circuit detection Thermal Shutdown

Six independent thermal shutdown circuits are featured (one common sensor for each HS and LS transistor pair). Each sensor has two levels, one to give a Thermal Warning (TW) and a higher one, Thermal Shutdown, which will shut the drivers off. When the part reaches the temperature point of Thermal Warning, the output data bit 0 (TW) will be set Applications Drawing

The applications drawing below displays the range with which this part can drive a multitude of loads.

- 1. H-Bridge Driver configuration
- 2. Low Side Driver
- 3. High Side Driver

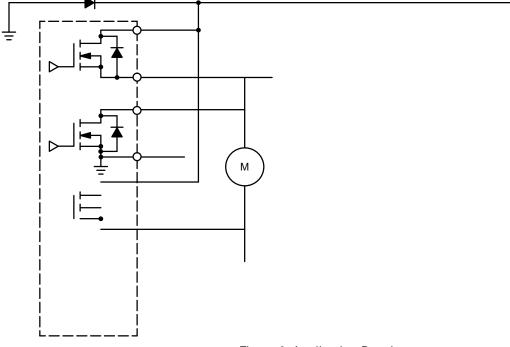


Figure 8. Application Drawing

TYPICAL OPERATING CHARACTERISTICS

Figure 9. High-

Table 1. FAULT HANDLING

Fault

Fault Memory

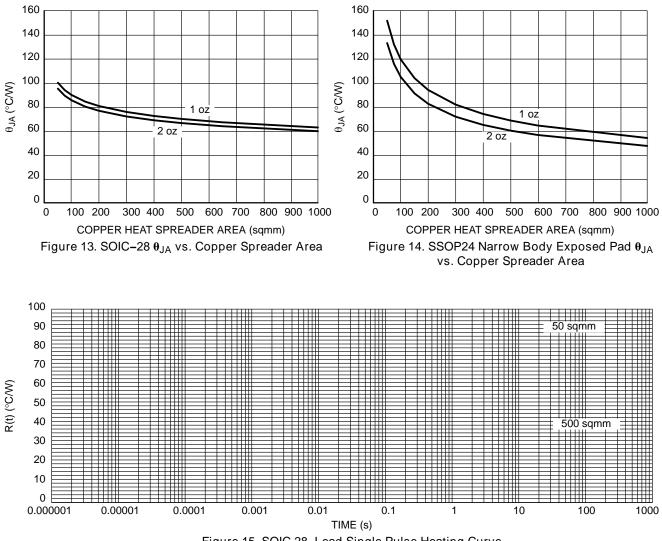
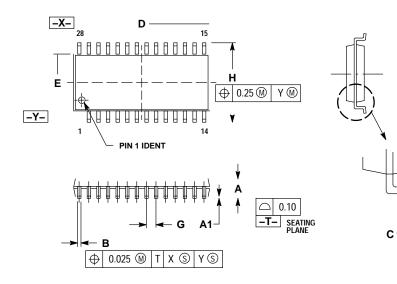


Figure 15. SOIC 28-Lead Single Pulse Heating Curve

SOIC-28 WB CASE 751F ISSUE J

DATE 23 SEP 2015



NOTES:

- NOTES: 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982. 2. CONTROLLING DIMENSION: MILLIMETER. 3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION 4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE. 5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBER PRSOTRUSION SHALL NOT BE 0.13 TOTATL IN EXCESS OF B DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS			
DIM	MIN	MAX		
Α	2.35	2.65		
A1	0.13	0.29		
В	0.35	0.49		
С	0.23	0.32		
D	17.80	18.05		
Ε	7.40	7.60		
G	1.27 BSC			
Н	10.05	10.55		
L	0.41	0.90		
М	0 °	8°		

Μ

GENERIC **MARKING DIAGRAM***

111111 1111111 111111 XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX	_
XXXXXXXXXXXXXXXXXX	
XXXXXXXXXXXXXXXXX	
AWLYYWWG	

XXXXX	= Specific Device Code	
Α	= Assembly Location	
WL	= Wafer Lot	
Y	= Year	

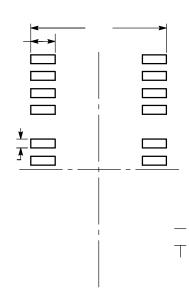
= Year

G

WW = Work Week

= Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot " •",

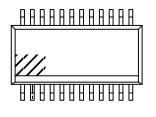


SSOP24 NB EP CASE 940AK ISSUE O

DATE 24 APR 2012

NOTES: 1. DIMENSIONINGTOP VIEW

SIDE VIEW



	1 11 1 1 1	
1		1.1
		1.70
. 1	0.00	0.10
•	0.19	0.30
-	0.09	0.20

	0.65 BSC		
	0.25	0.50	
1	0.40	0.85	
1	0.25 BSC		
1	0°	8°	

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