NCV7708E

Double Hex Driver

The NCV7708E is a fully protected Hex−Half Bridge−Driver designed specifically for automotive and industrial motion control applications. The six low and high side drivers are freely configurable and can be controlled separately. This allows for high side, low side, and H−Bridge control. H−Bridge control provides forward, reverse, brake, and high impedance states. The drivers are controlled via a standard SPI interface.

Features

- Ultra Low Quiescent Current Sleep Mode
- Six Independent High−Side and Six independent Low−Side Drivers
- Integrated Freewheeling Protection (LS and HS)
- Internal Upper and Lower Clamp Diodes
- Configurable as H−Bridge Drivers
- 0.5 A Continuous (1 A peak) Current
- $R_{DS(on)}$ = 0.8 Ω (typ)
- 5 MHz SPI Control
- SPI Valid Frame Detection
- Compliance with 5 V and 3.3 V Systems
- Overvoltage Lockout
- Undervoltage Lockout
- Fault Reporting
- Current Limit
- Overtemperature Protection
- Internally Fused Lead in SOIC−28
  Packaged for Better Thermal Performance
- These are Pb−Free Devices*

Typical Applications

- Automotive
- Industrial
- DC Motor Management

*For additional information on our Pb−Free strategy and soldering details, please

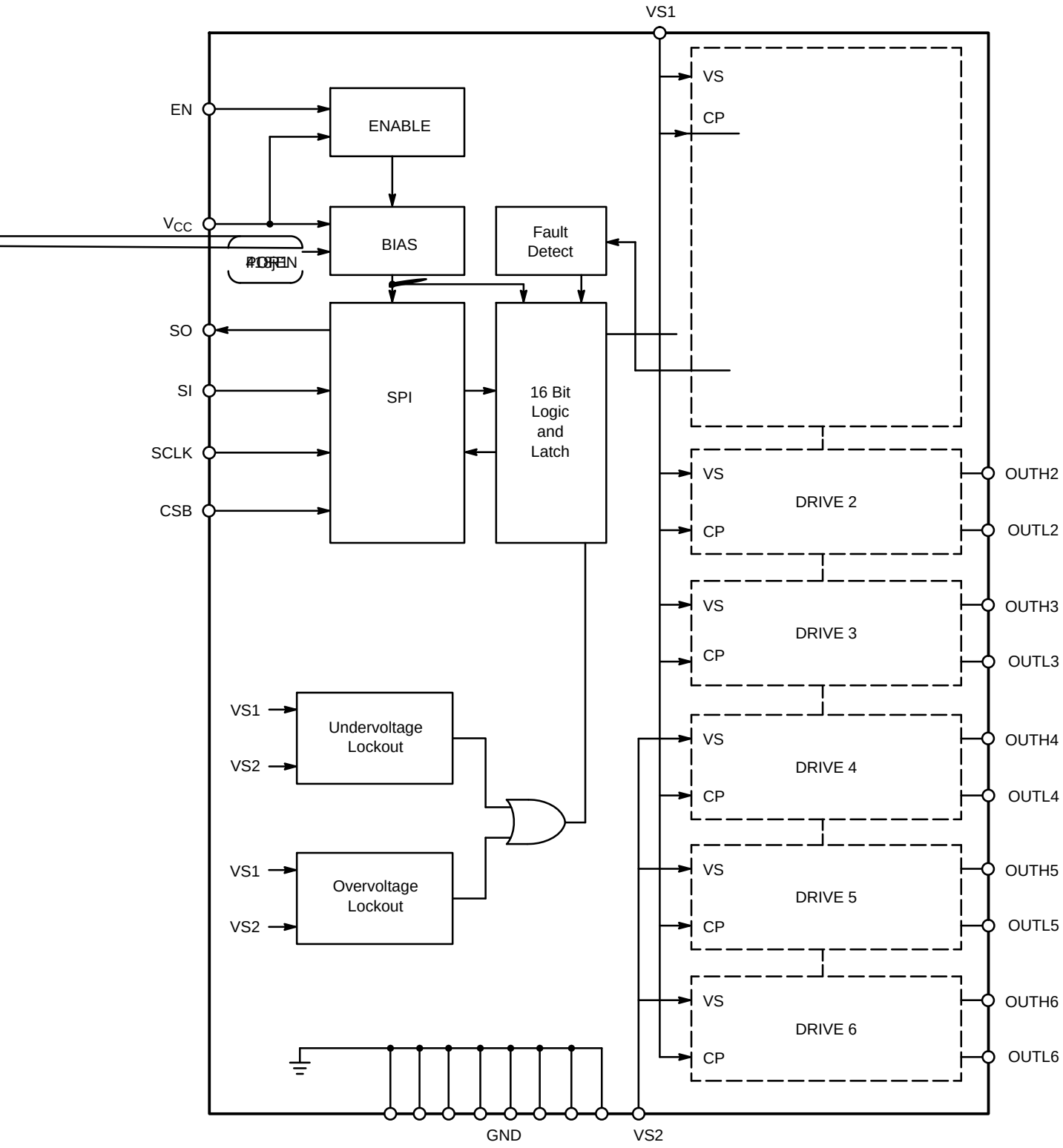


Figure 1. Block Diagram

n connected to VS2.
n connected to VS2.
low side pre−drivers,
n connected to VS1.
n connected to VS1.
n connected to VS1.

ELECTRICAL CHARACTERISTICS

(−40°C < T_J < 150°C, 5.5 V < VSx < 40 V, EN = V_{CC} = 5 V, unless otherwise specified)

Characteristic	Conditions	Timing Chart #	Min	Typ	Max	Unit
Serial Peripheral Interface (V_{CC} = 5 V)						
SCLK Frequency			−	−	5.0	MHz
SCLK Clock Period	V_{CC} = 5 V V_{CC} = 3.3 V		200 500	− −	− −	ns
Maximum Input Capacitance (Note 8)	SI, SCLK	−	−	−	12	pF
SCLK High Time		1	85	−	−	ns
SCLK Low Time		2	85	−	−	ns
SCLK Setup Time		3 4	85 85	− −	− −	ns
SI Setup Time		11	50	−	−	ns
SI Hold Time		12	50	−	−	ns
CSB Setup Time		5 6	100 100	− −	− −	ns
CSB High Time (Note 9)		7	200	−	−	ns
SO enable after CSB falling edge		8	−	−	50	ns
SO disable after CSB rising edge		9	−	−	50	ns
SO Rise Time	C_{load} = 40 pF	−	−	10	25	ns
SO Fall Time	C_{load} = 40 pF	−	−	10	25	ns
SO Valid Time	SCLK High to SO 50%	10	−	20	50	ns

8. Not tested in production
9. This is the minimum time the user must wait between SPI commands.

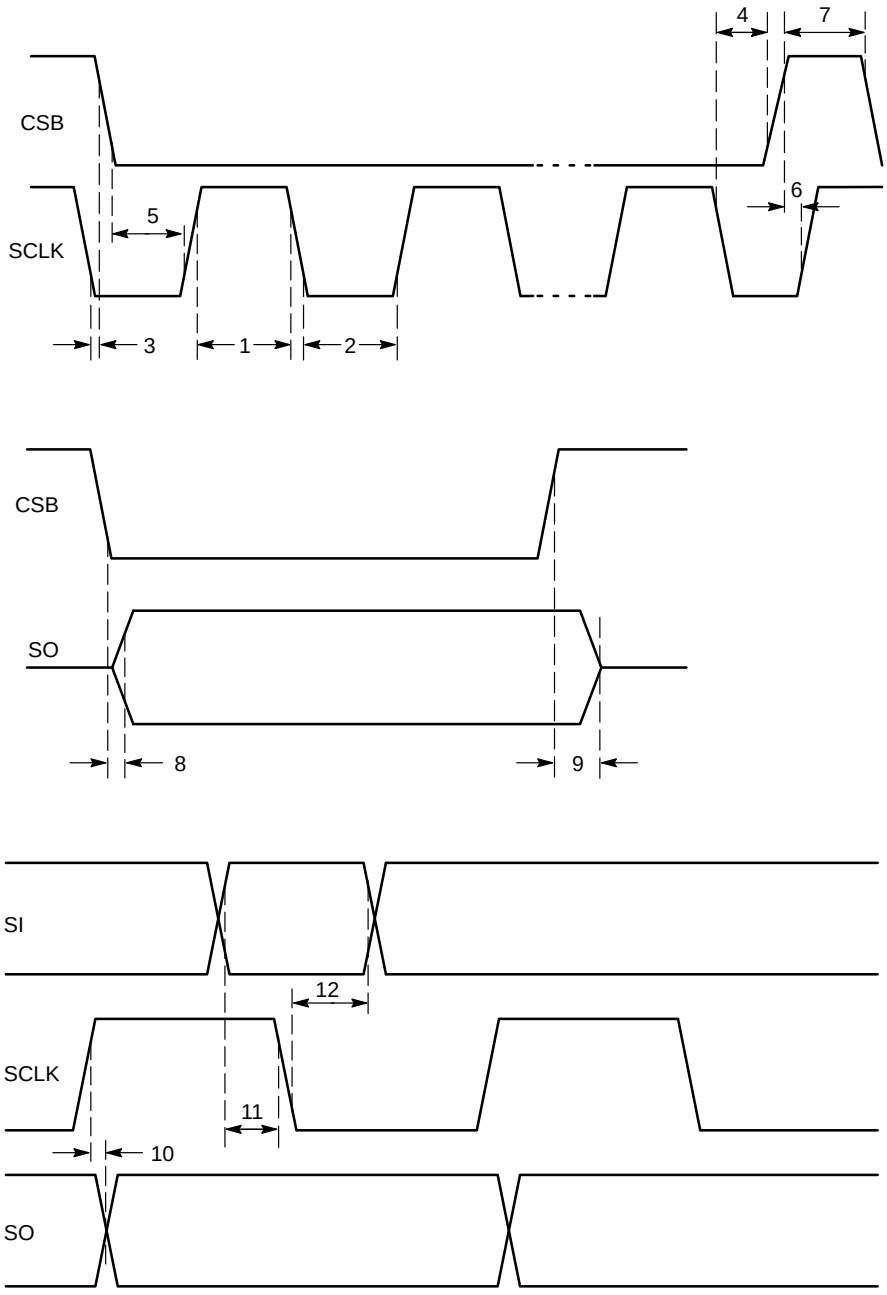


Figure 2. SPI Timing Diagram

SPI Communication

Standard 16−bit communication has been implemented for the communication of this IC to turn drivers on and off, and to report faults. (Reference the SPI Communication Frame Format Diagram). The LSB (Least Significant Bit) is clocked in first.

Communication is implemented as follows:

1. CSB goes low to allow serial data transfer.
2. A 16 bit word is clocked (SCLK) into the SI (serial input) pin. The SI input signal is latched on the falling edge of SCLK.
3. CSB goes high to transfer the clocked in information to the data registers. (Note: SO is tristate when CSB is high.)
4. The SI data will be accepted when a valid SPI frame is detected. A valid SPI frame consists of the above conditions and a complete set of multiples of 16 bit words.

DETAILED OPERATING DESCRIPTION

General

The NCV7708E Double Hex Driver provides drive capability for 3 independent H−Bridge configurations, or 6 High Side configurations with 6 Low Side configurations, or any combination of arrangements. Each output drive is characterized for a 500 mA load and has a typical 1.0 A surge capability (at 12 V). Strict adherence to integrated circuit die temperature is necessary. Maximum die temperature is 150°C. This may limit the number of drivers enabled at one time. Output drive control and fault reporting is handled via the SPI (Serial Peripheral Interface) port.

An Enable function (EN) provides a low quiescent sleep current

Over Voltage Shutdown

Over voltage shutdown circuitry monitors the voltage on the VS1 and VS2 pins. When the Over−voltage Threshold voltage level has been breached on both or either one of the VSx supply inputs, output bit 15 will be set and, if input bit 15 (OVLO) is set to 1, all outputs will turn off. Turn on/off status is maintained in the logic circuitry. When proper input voltage levels are re−established, the programmed outputs will turn back on. Over−voltage shutdown can be disabled by using the SPI input bit 15 (OVLO = 0).

Over Voltage Lock Out (OVLO) Shut Down

OVLO Input Bit 15	VSx OVLO Condition	Output Data Bit 15 Power Supply Fail (PSF) Status	OUTx Status
0	0	0	Unchanged
0	1	1 (Need SRR to reset)	Unchanged
1	0	0	Unchanged
1	1	1 (Need SRR to reset)	All Outputs Off (Remain off until VSx is out of OVLO)

Thermal Shutdown

Six independent thermal shutdown circuits are featured (one common sensor for each HS and LS transistor pair). Each sensor has two levels, one to give a Thermal Warning (TW) and a higher one, Over Temperature, which will shut the drivers off. When the part reaches the temperature point of Thermal Warning, the output data bit 0 (TW) will be set to a 1, and the outputs will remain on. With one or more sensors detecting the over temperature level, all channels

Applications Drawing

The applications drawing below displays the range with which this part can drive a multitude of loads.

1. H−Bridge Driver configuration
2. Low Side Driver
3. High Side Driver

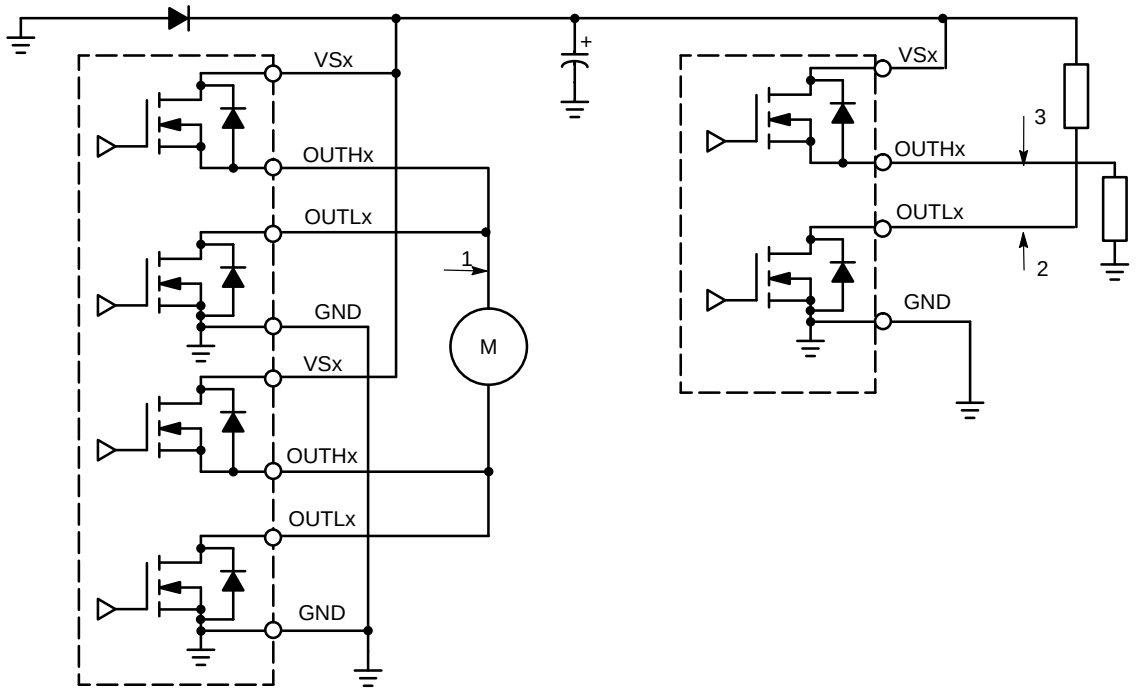


Figure 5. Application Drawing

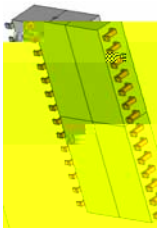
Any combination of motors and high side drivers can be designed in. This allows for flexibility in many systems.

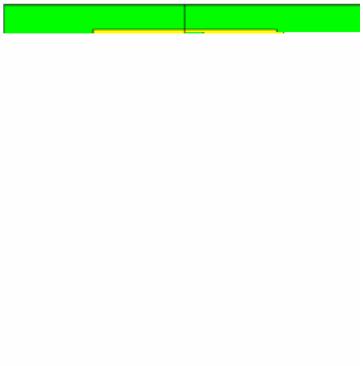
H−Bridge Driver Configuration

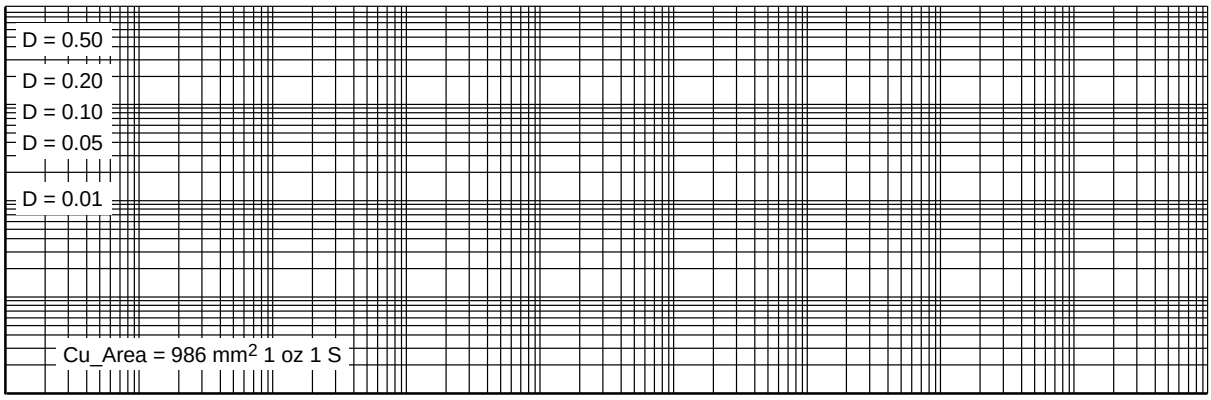
The NCV7708E has the flexibility of controlling each driver independently. When the device is set up in an H−Bridge configuration, the software design has to take care of avoiding simultaneous activation of connected HS and LS transistors. Resulting high shoot through currents could cause irreversible damage to the device.

Overvoltage Clamping − Driving Inductive Loads

To avoid excessive voltages when driving inductive loads in a single−side−mode (LS or HS switch, no freewheeling path), the NCV7708E provides internal clamping diodes. Thus any load type can be driven without the requirement of external freewheeling diodes. Due to high power dissipation during clamping, the maximum energy capability of the driver transistor has to be considered.






D = 0.50
D = 0.20
D = 0.10
D = 0.05
D = 0.01
Cu_Area = 986 mm2 1 oz 1 S

The Cauer networks generally have physical significance and may be divided between nodes to separate thermal behavior due to one portion of the network from another. The Foster networks, though when sorted by time constant (as above) bear a rough correlation with the Cauer networks, are really only convenient mathematical models. Both Foster and Cauer networks can be easily implemented using circuit simulating tools, whereas Foster networks may be more easily implemented using mathematical tools (for instance, in a spreadsheet program), according to the following formula:

$$R(t) = \sum_{i=1}^{n} R_i \left(1 - e^{-t/tau_i}\right)$$

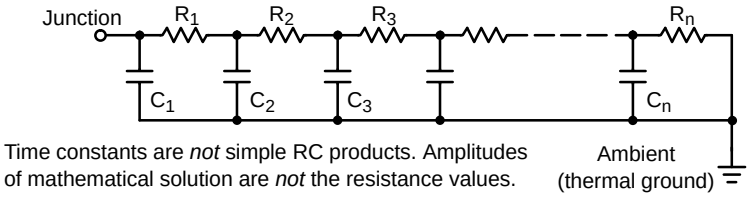


Figure 12. Grounded Capacitor Thermal Network (“Cauer” Ladder)

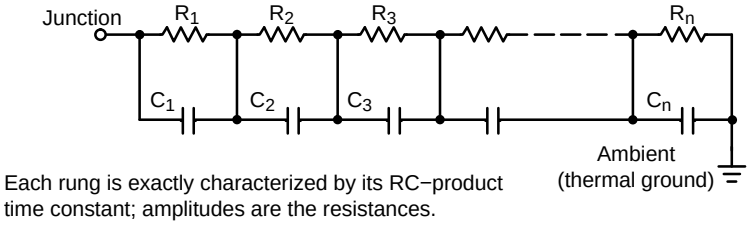
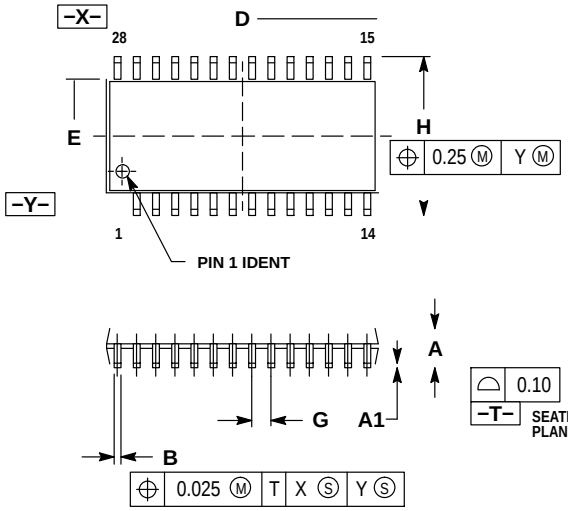
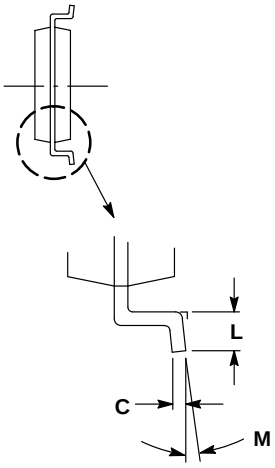


Figure 13. Non−Grounded Capacitor Thermal Ladder (“Foster” Ladder)

SOIC−28 WB
CASE 751F
ISSUE J

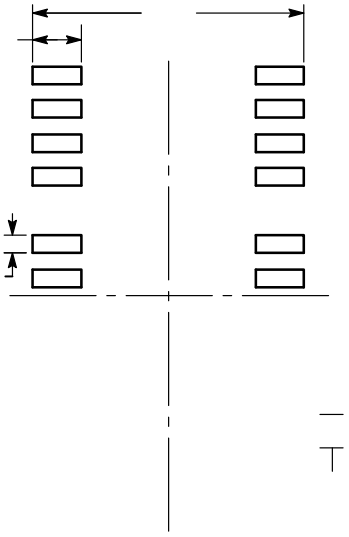
DATE 23 SEP 2015



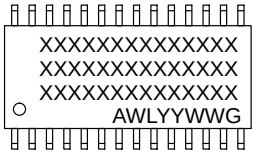


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBER PR5OTRUSION SHALL NOT BE 0.13 TOTATL IN EXCESS OF B DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS	
DIM	MIN	MAX
A	2.35	2.65
A1	0.13	0.29
B	0.35	0.49
C	0.23	0.32
D	17.80	18.05
E	7.40	7.60
G	1.27 BSC	
H	10.05	10.55
L	0.41	0.90
M	0 °	8 °



GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”,