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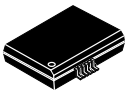


SSOP36 EP
DQ SUFFIX
CASE 940AB

MARKING DIAGRAM

$R_{DS(on)}$ = 100 mΩ @ 25°C

- Electro Chromic Mirror Control (NCV7714 Only)
  - 1x 6−Bit Selectable Output Voltage Controller
  - 1x LS for EC Control; I_{load} = 0.75 A; $R_{DS(on)}$ = 1.6 Ω @ 25°C
- Independent PWM Functionality for All Outputs
- Integrated Programmable PWM Generator Unit for All Lamp Driver Outputs
  - 7−bit / 9−bit Selectable Duty−cycle Setting Precision
- Programmable Soft−start Function to Drive Loads with Higher Inrush Currents as Current Limitation Value
- Multiplex Current Sense Analog Output for Advanced Load Monitoring
- Very Low Current Consumption in Standby Mode
- Charge Pump Output to Control an External Reverse Polarity Protection MOSFET
- 24−Bit SPI Interface for Output Control and Diagnostic
- Protection Against Short−circuit, Overvoltage and Over−temperature
- Downwards Pin−to−Pin and SPI Registers Compatible with NCV7707
- AEC−Q100 Qualified and PPAP Capable
- SSOP36−EP Power Package
- This is a Pb−Free Device

Typical Applications

- De−centralized Door Electronic Systems
- Body Control Units (BCUs)

April, 2016 − Rev. 0load = 6 A;

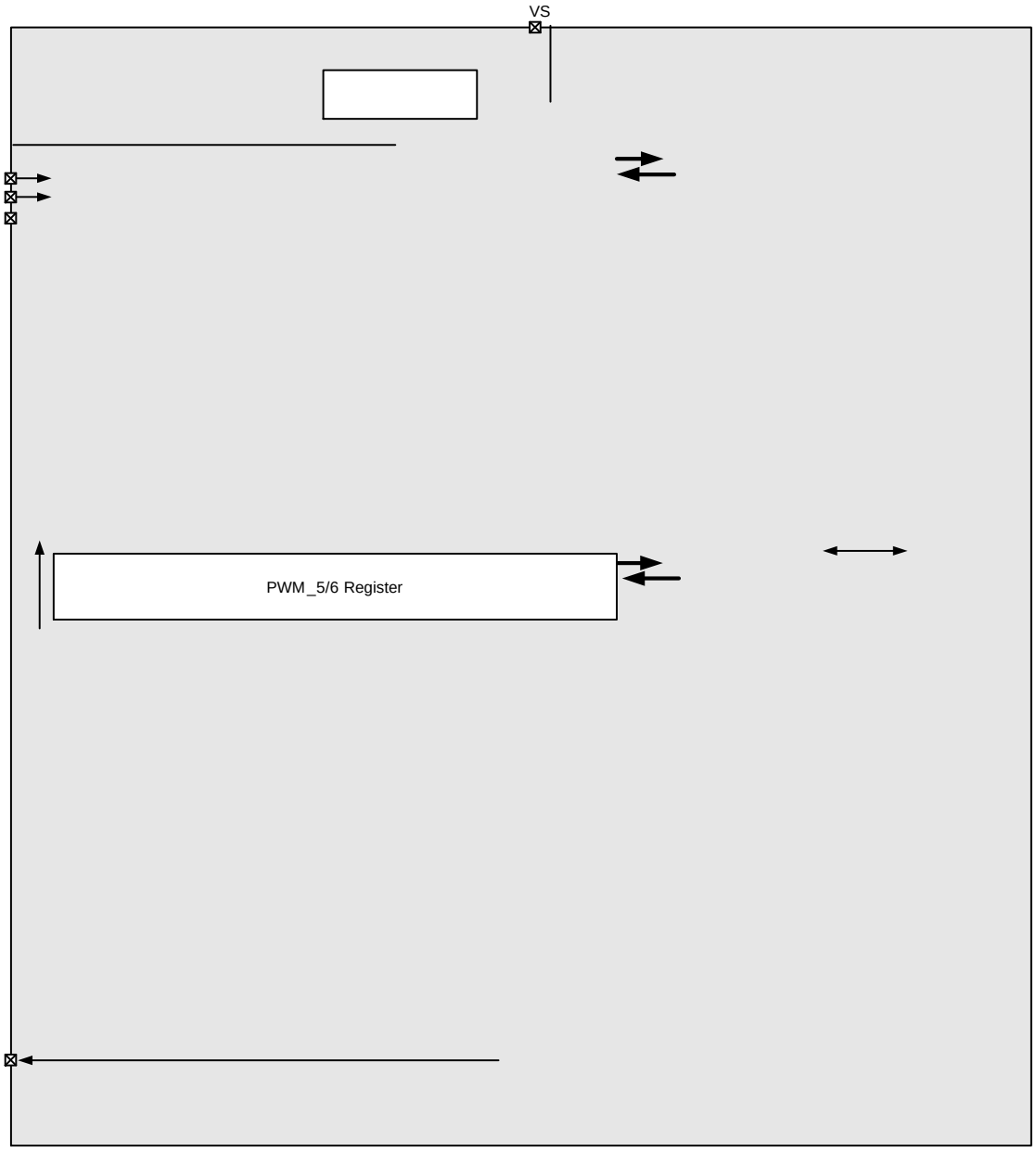


Figure 1. Block Diagram

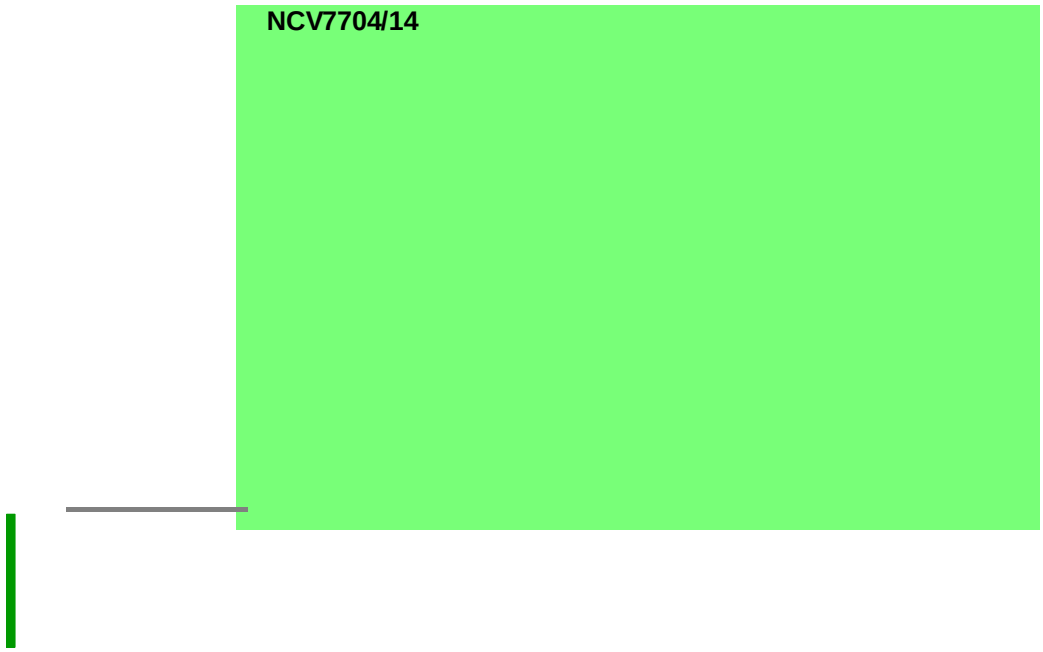


Figure 2. Application Diagram

Table 1. PIN FUNCTION DESCRIPTION

Pin No.	Pin Name	Pin Type	Description
1	GND	Ground	Ground Supply (all GND pins have to be connected externally)
2	OUT7	HS driver Output	Heater Output (has to be connected externally to pin 35)
3	OUT1	Half bridge driver Output	Mirror common Output
4	OUT2	Half bridge driver Output	Mirror x/y control Output
5	OUT3	Half bridge driver Output	Mirror x/y control Output
6	VS	Supply	Battery Supply Input (all VS pins have to be connected externally)
7	VS	Supply	Battery Supply Input (all VS pins have to be connected externally)
8	SI	Digital Input	SPI interface Serial Data Input
9	ISOUT/PWM2	Digital Input / Analog Output	PWM control Input / Current Sense Output. This pin is a bidirectional pin. Depending on the selected multiplexer bits, an image of the instant current of the corresponding HS stage can be read out. This pin can also be used as PWM control input pin for OUT4 and OUT6.
10	CSB	Digital Input	SPI interface Chip Select
11	SO	Digital Output	SPI interface Serial Data Output
12	VCC	Supply	Logic Supply Input
13	SCLK	Digital Input	SPI interface Shift Clock
14	n.c.		Not connected
15	n.c.		Not connected
16	n.c.		Not connected
17	n.c.		Not connected
18	n.c.		Not connected
19	GND	Ground	Ground Supply (all GND pins have to be connected externally)
20	n.c.		Not connected
21	n.c.		Not connected
22	n.c.		Not connected
23	n.c.		Not connected
24	n.c.		Not connected
25	VS/TEST (NCV7704 only)	Supply	Test Input, has to be connected to VS in application
	ECON (NCV7714 only)	ECM driver Output	Electrochromic mirror control DAC output. If the Electrochrome feature is selected, this output controls an external Mosfet, otherwise it remains in high−impedance state. If the electrochrome feature is not used in the application and not selected via SPI the pin can be connected to VS.
26	CHP	Analog Output	Reverse Polarity FET Control Output
27	PWM1	Digital Input	PWM control Input for OUT1−3, OUT5 and OUT7
28	VS	Supply	Battery Supply Input (all VS pins have to be connected externally)
29	VS	Supply	Battery Supply Input (all VS pins have to be connected externally)
30	n.c.		Not connected
31	OUT4	HS driver Output	LED / Bulb Output
32	VS (NCV7704 only)	Supply	Connect to VS pins externally (no power connection)
	ECFB (NCV7714 only)	ECM Input / Output	Electrochromic Mirror Feedback Input, Fast discharge transistor Output
33	OUT5	HS driver Output	LED Output
34	OUT6	HS driver Output	LED Output
35	OUT7	HS driver Output	Heater Output (has to be connected externally to pin 2)
36	GND	Ground	Ground Supply (all GND pins have to be connected externally)
	Heat slug	Ground	Substrate; Heat slug has to be connected to all GND pins

Table 2. ABSOLUTE MAXIMUM RATINGS

Symbol	Rating	Min	Max	Unit
Vs	Power supply voltage − Continuous supply voltage − Transient supply voltage (t < 500 ms, “clamped load dump”)	 −0.3 −0.3	 28 40	V
Vcc	Logic supply	−0.3	5.5	V
Vdig	DC voltage at all logic pins (SO, SI, SCLK, CSB, PWM1)	−0.3	Vcc + 0.3	V
Visout/pwm2	Current monitor output / PWM2 logic input	−0.3	Vcc + 0.3	V
Vchp	Charge pump output (the most stringent value is applied)	−25 Vs − 25	40 Vs + 15	V
Voutx, Vecon, Vecfb	Static output voltage (OUT1−7, ECON, ECFB)	−0.3	Vs + 0.3	V
Iout1/2/3	OUT1/2/3 Output current − Tj ≥ 25°C − Tj < 25°C	 −1.25 −1.35	 1.25 1.35	A
Iout4	OUT4 Output current − DC − Transient	 −5	 5	A
Iout5/6	OUT5/6 Output current − DC − Transient	 −1.25	 1.25	A
Iout7	OUT7 Output current − DC − Transient	 −10	 10	A
Iout_ecfb (NCV7714 only)	ECFB Output current		1.25	A
ESD_HBM	ESD Voltage, HBM (Human Body Model); (100 pF, 1500 Ω) (Note 1) − All pins			

Table 4. ELECTRICAL CHARACTERISTICS 4.5 V < Vcc < 5.25 V, 8 V < Vs < 18 V, −40°C < Tj < 150°C; unless otherwise noted.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
SUPPLY						
Vs	Supply voltage	Functional (see Vuv_vs / Vov_vs) Parameter specification	5.5 8		28 18	V
Is(standby)	Supply Current (VS), Standby					

Table 4. ELECTRICAL CHARACTERISTICS 4.5 V < Vcc < 5.25 V, 8 V < Vs < 18 V, −40°C < Tj < 150°C; unless otherwise noted.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
MIRROR x/y POSITIONING OUTPUTS OUT1, OUT2, OUT3						
Ron_out,12,3	On−resistance HS or LS	Tj = 25°C, Iout1,2,3 = ± 0.5 A		1.6		Ω
		Tj = 125°C, Iout1,2,3 = ± 0.5 A			3	Ω
Ioc1,2,3_hs	Overcurrent threshold HS	Tj < 25°C Tj ≥ 25°C	−1.35 −1.25		−0.75	A
Ioc1,2,3_ls	Overcurrent threshold LS	Tj < 25°C Tj ≥ 25°C	0.75		1.35 1.25	A
Vlim1,2,3	Vds voltage limitation HS or LS		2		3	V
Iuld1,2,3_hs	Underload detection threshold HS		−32	−20	−10	mA
Iuld1,2,3_ls	Underload detection threshold LS		10	20	32	mA
td_HS1,2,3(on)	Output delay time, HS Driver on	Time from CSB going high to V(OUT1,2,3) = 0.1·Vs / 0.9·Vs (on/off)		2.5	6	µs
td_HS1,2,3(off)	Output delay time, HS Driver off			3	6	µs
td_LS1,2,3(on)	Output delay time, LS Driver on	Time from CSB going low to V(OUT1,2,3) = 0.9·Vs / 0.1·Vs (on/off)		1	6	µs
td_LS1,2,3(off)	Output delay time, LS Driver off			1	6	µs
tdLH1,2,3						

Table 4. ELECTRICAL CHARACTERISTICS 4.5 V < Vcc < 5.25 V, 8 V < Vs < 18 V, −40°C < Tj < 150°C; unless otherwise noted.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
BULB / LED DRIVER OUTPUT OUT4						
Ron_out4_ICB	On−resistance to supply, HS switch, Bulb mode					

Table 4. ELECTRICAL CHARACTERISTICS 4.5 V < Vcc < 5.25 V, 8 V < Vs < 18 V, −40°C < Tj < 150°C; unless otherwise noted.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
LED DRIVER OUTPUTS OUT5, OUT6						
Ron_out5,6	On−resistance to supply, HS switch	Tj = 25°C, Iout5,6 = −0.2 A		1.4		Ω
		Tj = 125°C, Iout5,6 = −0.2 A			3	

Table 4. ELECTRICAL CHARACTERISTICS 4.5 V < Vcc < 5.25 V, 8 V < Vs < 18 V, −40°C < Tj < 150°C; unless otherwise noted.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
ELECTROCHROMIC MIRROR CONTROL (ECFB, ECON) (NCV7714 ONLY)						
Ron_ecfb	On−resistance to GND, LS switch	Tj = 25°C, Iecfb = 0.5 A		1.6		Ω
		Tj = 125°C, Iecfb = 0.5 A			3	Ω
Ilim_ecfb_src	Output current limitation to GND	Vs = 13.5V, Vcc = 5 V	0.75		1.25	A
Vlim_ecfb	Vds voltage limitation	Output enabled	2		3	V
Iuld_ecfb	Underload detection threshold	Vs = 13.5 V, Vcc = 5 V	10	20	35	mA
td_ecfb(on)	Output delay time, LS Driver on	Vs = 13.5 V, Vcc = 5 V, Rload = 64 Ω, V(ECFB) = 0.9·VS / 0.1·VS (on /off)		1	12	μs
td_ecfb(off)	Output delay time, LS Driver off			2	12	μs
Ileak_ecfb_stdby	Output leakage current, LS off	Vecfb = Vs, Standby mode	−15		15	μA
Ileak_ecfb_act		Vecfb = Vs, Active mode	−10		10	μA
td_uld_ecfb	Underload blanking delay		430		610	μs
tdb_old_ecfb	Overload shutdown blanking delay	Timer started after output activation	30		48	μs
td_old_ecfb	Overload shutdown blanking delay	Timer started after blanking delay				

Table 4. ELECTRICAL CHARACTERISTICS 4.5 V < Vcc < 5.25 V, 8 V < Vs < 18 V, −40°C < Tj < 150°C; unless otherwise noted.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
CURRENT SENSE MONITOR OUTPUT ISOUT/PWM2						
Vis	Current Sense output functional voltage range	Vcc = 5 V, Vs = 8−20 V	0		Vcc – 0.5	V
Kis (Note 6)	Current Sense output ratio OUT7 and 4 (low on−resistance bulb mode)	K = Iout / Iis, 0 V ≤ Vis ≤ 4.5 V, Vcc = 5 V		10000		
	Current Sense output ratio OUT5/6 and 4 (high on−resistance LED mode)			2000		
Iis,acc (Notes 7, 8)	Current Sense output accuracy OUT4 (low on−resistance bulb mode)	0.3 V ≤ Vis ≤ 4.5 V, Vcc = 5 V Iout4 = 0.5−1.3 A	−2% − 6% FS		23% − 4% FS	
	Current Sense output accuracy OUT4 (high on−resistance LED mode)	0.3 V ≤ Vis ≤ 4.5 V, Vcc = 5 V Iout4 = 0.1−0.28 A	−6% − 4% FS		21% − 4% FS	
	Current Sense output accuracy OUT5/6	0.3 V ≤ Vis ≤ 4.5 V, Vcc = 5 V Iout5/6 = 0.1−0.4 A	−3% − 6% FS		17% − 3% FS	
	Current Sense output accuracy OUT7	0.3 V ≤ Vis ≤ 4.5 V, Vcc = 5 V Iout7 = 0.5−5.9 A	−7% − 5% FS		12% − 1% FS	
tis_blank	Current Sense blanking time		50		65	μs
tis	Current Sense settling time	0 V to FSR (full scale range)		230	264	μs

6. Kis trimmed at 150°C to higher value of spec range to be more centered over temp range.
7. Current sense output accuracy = Isout−Isout_ideal relative to Isout_ideal
8. FS (Full scale) = Ioutmax/Kis

Table 4. ELECTRICAL CHARACTERISTICS 4.5 V < Vcc < 5.25 V, 8 V < Vs < 18 V, −40°C < Tj < 150°C; unless otherwise noted.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
DIGITAL INPUTS CSB, SCLK, PWM1/2, SI						
Vinl	Input low level	Vcc = 5 V			0.3·Vcc	V
Vinh	Input high level	Vcc = 5 V	0.7·Vcc			V
Vin_hyst	Input hysteresis		500			mV
Rcsb_pu	CSB pull−up resistor	Vcc = 5 V, 0 V < Vcsb < 0.7·Vcc	30	120	250	kΩ
Rsclk_pd	SCLK pull−down resistor	Vcc = 5 V, Vsclk = 1.5 V	30	60	220	kΩ
Rsi_pd	SI pull−down resistor	Vcc = 5 V, Vsi = 1.5 V	30	60	220	kΩ
Rpwm1_pd	PWM1 pull−down resistor	Vcc = 5 V, Vpwm1 = 1.5 V	30	60	220	kΩ
Rpwm2_pd	PWM2 pull−down resistor	Vcc = 5 V, Vpwm2 = 1.5 V, current sense disabled	30	60	220	kΩ
Ileak_isout	Output leakage current	current sense enabled	−2		2	μA
Ccsb/sclk/pwm1/2	Pin capacitance	0 V < Vcc < 5.25 V (Note 9)			10	pF
DIGITAL INPUTS CSB, SCLK, SI; TIMING						
tsclk	Clock period	Vcc = 5 V		1000		ns
tsclk_h	Clock high time		115			ns
tsclk_l	Clock low time		115			ns
tset_csb	CSB setup time, CSB low before rising edge of SCLK		400			ns
tset_sclk	SCLK setup time, SCLK low before rising edge of CSB		400			ns
tset_si	SI setup time		200			ns
thold_si	SI hold time		200			ns
tr_in	Rise time of input signal SI, SCLK, CSB				100	ns
tf_in	Fall time of input signal SI, SCLK, CSB				100	ns
tcsb_hi_stdby	Minimum CSB high time, switching from Standby mode	Transfer of SPI−command to input register, valid before tsact mode transition delay expires		5	10	μs
tcsb_hi_min	Minimum CSB high time, Active mode			2	4	μs

9. Values based on design and/or characterization

DETAILED OPERATING AND PIN DESCRIPTION

General

The NCV7704/NCV7714 provides three half−bridge drivers, four independent high−side outputs and a programmable PWM control unit for free configuration. Strict adherence to integrated circuit die temperature is necessary, with a static maximum die temperature of 150°C. This may limit the number of drivers enabled at one time. Output drive control and fault reporting are handled via the SPI (Serial Peripheral Interface) port. A SPI−controlled mode control provides a low quiescent sleep current mode when the device is not being utilized. A pull down is provided on the SI and SCLK inputs to ensure they default to a low state in the event of a severed input signal. A pull−up is provided on the CSB input disabling SPI communication in the event of an open CSB input.

Supply Concept

Power Supply Scheme − VS and VCC

The Vs power supply voltage is used to supply the half bridges and the high−side drivers. An all−internal chargepump is implemented to provide the gate−drive voltage for the n−channel type high−side transistors. The VCC voltage is used to supply the logic section of the IC, including the SPI interface.

Table 5. PWM CONTROL SCHEME

Output	PWM Control Input		
	CONTROL_2.PWMI = 0	CONTROL_2.PWMI = 1	
		CONFIG.PWM_RESEN=0	CONFIG.PWM_RESEN=1
OUT1	PWM1	PWM1	PWM1
OUT2	PWM1	PWM1	PWM1
OUT3	PWM1	PWM1	PWM1
OUT4	ISOUT/PWM2	PWM_4.PW4[6:0]	PWM_4.PW4[6:−2]
OUT5	PWM1	PWM_5/6.PW5[6:0]	PWM_5/6.PW5[6:0] & PWM_4.PW5[−1:−2]
OUT6	ISOUT/PWM2	PWM_5/6.PW6[6:0]	PWM_5/6.PW6[6:0] & PWM_4.PW6[−1:−2]
OUT7	PWM1	PWM1	PWM1

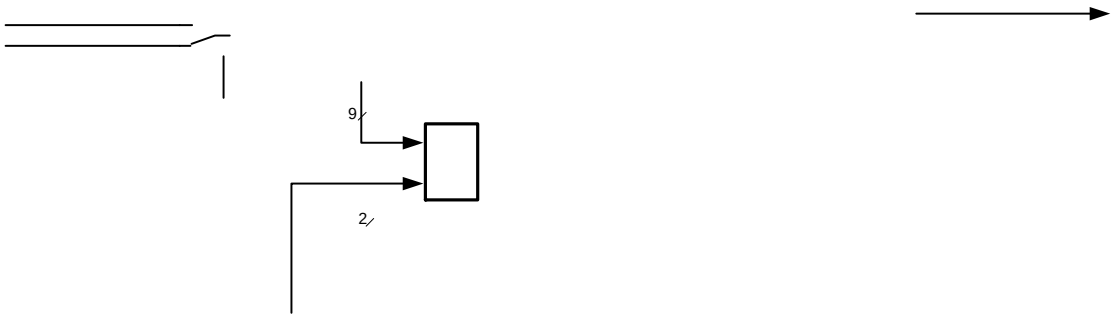


Figure 5. PWM Generation Diagram

Current Sensing

Current Sense Output / PWM2 Input (Bidirectional Pin ISOUT/PWM2)

The current sense output allows a more precise analysis of the actual state of the load rather than the basic detection of an under− or overload condition. The sense output provides an image of the actual load current at the selected high side driver transistor. The current monitor function is available for the high current high−side output (OUT7) as well as for the all bulb and LED outputs (OUT4−6).

The current sense ratio is fixed to 1/10000 for the low resistance outputs OUT4 (bulb mode) and OUT7 and for the high ohmic outputs OUT5/6 and OUT4 (LED mode) to 1/2000. To prevent from false readouts, the signal at pin ISOUT is blanked after switching on the driver until correct settlement of the circuitry (max. 65 μs). Bits CONTROL_3.IS[3:0] are used to select the output to be multiplexed to the current sense output.

The NCV7704/NCV7714 provides a sample−and−hold functionality for the current sense output to enable precise and simple load current diagnostics even during PWM operation of the respective output. While in active high−side output state, the current provided at ISOUT reflects a (low−pass−filtered) image of the actual output current, the IS−output current is sampled and held constant as soon as the HS output transistor is commanded off via PWM (high−impedance). In case no previous current information is available in the Sample−and−hold stage (current sense channel changed while actual channel is commanded off) the sample stage is reset so that it reflects zero output current.

Electro Chromic Mirror (NCV7714 ONLY)

Controller for Electro−chromic Glass

The voltage of the electro−chromic element connected at pin ECFB can be controlled to a target value which is set by Control Register 1 (bits CONTROL_1.DAC[5:0]). Setting

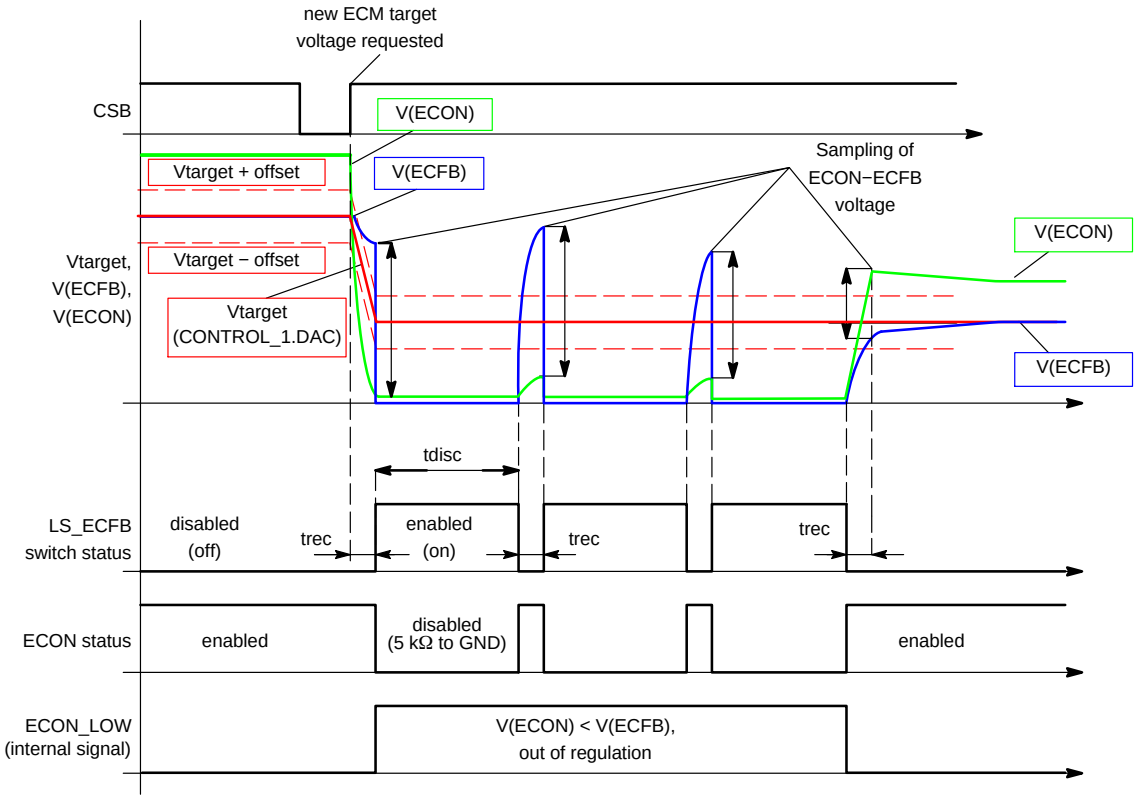
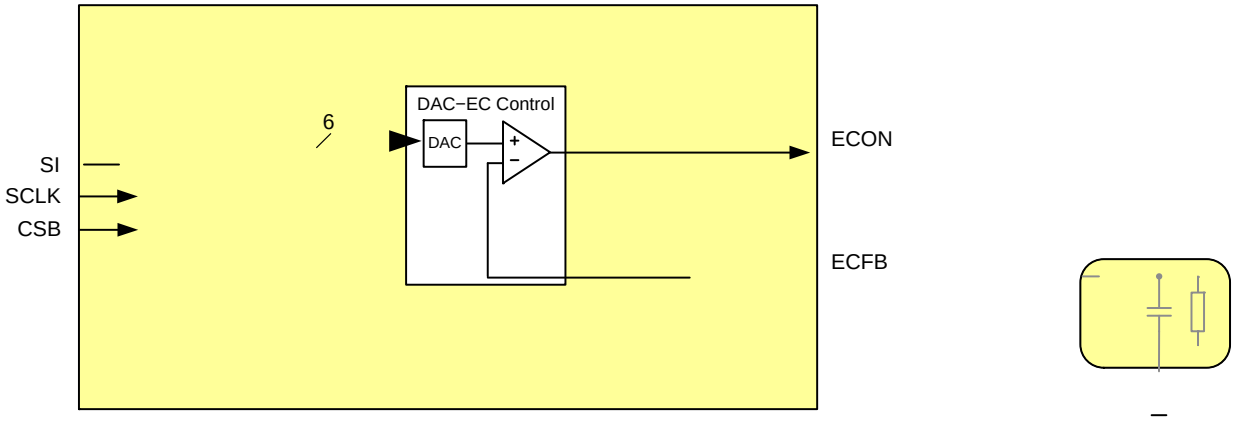


Figure 6. PWM Discharge Mode for ECFB

The controller provides a chip−internal diode from ECFB (Anode) to pin ECON (Cathode) to protect the external MOSFET. A capacitor of at least 4.7 nF has to be added to pin ECON for stability of the control loop. It is recommended to place 220 nF capacitor between ECFB and ground to increase the stability.

The status of the voltage control loop is reported via SPI. Bit STATUS_2.ECHI = 1 indicates that the voltage on ECFB is higher than the programmed target value, STATUS_2.ECLO = 1 indicates that the ECFB voltage is below the programmed value. Both status bits are valid if they are stable for at least 150 µs (settling time of the regulation loop). If PWM discharge is enabled (CONFIG.ECM_LSPWM = 1), STATUS_2.ECHI is latched at the end of the discharge cycle, therefore if set it indicates that the device is in active discharge operation.

Since OUT6 is the output of a high−side driver, it contains the same diagnostic functions as the other high−side drivers (e.g. switch−off during overcurrent condition). In electro−chrome mode, OUT6 can't be controlled by PWM. For noise immunity reasons, it is recommended to place the loop capacitors at ECON as well as another capacitor between ECFB and GND as close as possible to the respective pins.



Diagnostic Functions

All diagnostic functions (overcurrent, underload, power supply monitoring, thermal warning and thermal shutdown) are internally filtered. The failure condition has to be valid for the minimum specified filtering time (td_old, td_uld, td_uvov and td_tx) before the corresponding status bit in the status register is set. The filter function is used to improve the noise immunity of the device. The undercurrent and temperature warning functions are intended for information purpose and do not affect the state of the output drivers. An overcurrent condition disables the corresponding output driver while a thermal shutdown event disables all outputs into high impedance state. Depending on the setting of the overcurrent recovery bits in the input register, the driver can either perform an auto−retry or remain latched off until the microcontroller clears the corresponding status bits. Overtemperature shutdown is latch−off only, without auto−retry functionality.

Overvoltage / Undervoltage Shutdown

If the supply voltage Vs rises above the switch off voltage Vov_vs(off) or falls below Vuv_vs(off), all output transistors are switched to high−impedance state and the global status bit UOV_OC (multi information) is set. The status flag STATUS_2.VSOV, resp. STATUS_2.VSUV is set, too, to log the over−/under−voltage event. The bit CONTROL_3.OVUVR can be used to determine the recovery behavior once the Vs supply voltage gets back into the specified nominal operating range. OVUVR = 0 enables auto−recovery, with OVUVR = 1 the output stages remain in high impedance condition until the status flags have been cleared. Once set, STATUS2.VSOV / VSUV can only be reset by a read&clear access to the status register STATUS_2.

Thermal Warning and Overtemperature Shutdown

The device provides a dual−stage overtemperature protection. If the junction temperature rises above Tjtw_on, a temperature warning flag (TW) is set in the Global Status Byte and can be read via SPI. The control software can then react onto this overload condition by a controlled disable of individual outputs. If however the junction temperature reaches the second threshold Tjsd_on, the thermal shutdown bit TSD is set in the Global Status Byte and all output stages are switched into high impedance state to protect the device. The minimum shutdown delay for overtemperature is td_tx. The output channels can be re−enabled after the device cooled down and the TSD flag has been reset by the microcontroller by setting CONTROL_0.MODE = 0.

Openload (Underload) Detection

The openload detection monitors the load current in the output stage while the transistor is active. If the load current is below the openload detection threshold for at least td_uld, the corresponding bit (ULDx) is set in the status registers STATUS_1/2. The status of the output remains unchanged. Once set, ULDx remains set regardless of the actual load condition. It has to be reset by a read&write access to the corresponding status register.

Overload Detection

An overcurrent condition is indicated by the flag (UOV_OC) in the Global Status Byte after a filter time of at least td_old. The channel dependent overcurrent flags are set in the status registers (STATUS_0/2.OCx) and the corresponding driver is switched into high impedance state to protect the device. Each low−side and high−side driver stage provides its own overcurrent flag. Resetting this overcurrent flag automatically re−enables the respective output (provided it is still enabled thru the Control register). If the over current recovery function is enabled, the internal chip logic automatically resets the overcurrent flag after a fixed delay time, generating a PWM modulated current with a programmable duty cycle. Otherwise the status bits have to be cleared by the microcontroller by a read&clear access to the corresponding status register.

Cross−current Protection

All six half−bridges are protected against cross−currents by internal circuitry. If one driver is turned off (LS or HS), the activation of the other driver of the same output will be automatically delayed by the cross current protection mechanism until the active driver is safely turned off.

Mode Control

Wake−up and Mode Control

Two different modes are available:

- Active mode
- Standby mode

After power−up of VCC the device starts in Standby mode. Pulling the chip−select signal CSB to low level causes the device to change into Active mode (analog part active).

After at least 10 μs delay, the first SPI communication is valid and bit CONTROL_0.MODE can be used to set the desired mode of operation. If bit MODE remains reset (0), the device returns to the Standby mode after an internal delay of max. 8 μs, clearing all register content and setting all output stages into high impedance state.

24−bit SPI Interface

Both 24−bit input and output data are MSB first. Each SPI−input frame consists of a command byte followed by two data bytes. The data returned on SO within the same frame always starts with the global status byte. It provides general status information about the device. It is then followed by 2 data bytes (in−frame response) which content depends on the information transmitted in the command byte. For write access cycles, the global status byte is followed by the previous content of the addressed register.

Chip Select Bar (CSB)

CSB is the SPI input pin which controls the data transfer of the device. When CSB is high, no data transfer is possible and the output pin SO is set to high impedance. If CSB goes low, the serial data transfer is allowed and

Table 8. COMMAND BYTE, REGISTER ADDRESS

A[5:0]	Access	Description	Content
00h	R/W	Control Register CONTROL_0	Device mode control, Bridge outputs control
01h	R/W	Control Register CONTROL_1	High−side outputs control, ECM control (NCV7714 only)
02h	R/W	Control Register CONTROL_2	Bridge outputs recovery control, PWM enable, ECM setup (NCV7714 only)
03h	R/W	Control Register CONTROL_3	High−side outputs recovery control, PWM enable, Current Sense selection
08h	R/W	PWM Control Register PWM_4	PWM control register for OUT4
09h	R/W	PWM Control Register PWM_5/6	PWM control register for OUT5/6
10h	R/RC	Status Register STATUS_0	Bridge outputs Overcurrent diagnosis
11h	R/RC	Status Register STATUS_1	Bridge outputs Underload diagnosis
12h	R/RC	Status Register STATUS_2	HS outputs Overcurrent and Underload diagnosis, Vs Over− and Under-voltage, EC−mirror (NCV7714 only)
3Fh	R/W	Configuration Register CONFIG	Mask bits for global fault bits

Table 9. CHIP ID INFORMATION

A[5:0]	Access	Description	Content
00h	RDID	ID header	4300h
01h	RDID	Version	0000h
02h	RDID	Product Code 1	7700h
03h	RDID	Product Code 2	0400h (NCV7704) 0E00h (NCV7714)
3Eh	RDID	SPI−Frame ID	0200h

Table 10. GLOBAL STATUS BYTE CONTENT

FLT	Global Fault Bit	
0	No fault Condition	Failures of the Global Status Byte, bits [6:0] are always linked to the Global Fault Bit FLT. This bit is generated by an OR combination of all failure bits of the device (RESB inverted). It is reflected via the SO pin while CSB is held low and NO clock signal is present (before first positive edge of SCLK). The flag will remain valid as long as CSB is held low. This operation does not cause the

SPI REGISTERS CONTENT

CONTROL_0 Register

Address: 00h

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Access type	RW	RW	RW	RW	RW	RW	−	−	−	−	−	−	−	−	−	RW
Bit name	HS1	LS1	HS2	LS2	HS3	LS3	0	0	0	0	0	0	0	0	0	MODE
Reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	HSx	LSx		Description	Remark
HS/LS Outputs OUT1−3 Driver Control	0	0	default	OUTx High impedance	If a driver is enabled by the control register AND the corresponding PWM enable bit is set in CONTROL_2 register, the output is only activated if PWM1 (PWM2) input signal is high. Since OUT1..OUT3 are half−bridge outputs, activating both HS and LS at the same time is prevented by internal logic.
	0	1		LSx enabled	
	1	0		HSx enabled	
	1	1		OUTx High impedance	

	MODE		Description	Remark
Mode Control	0	default	Standby	If MODE is set, the device is switched to Active mode. Resetting MODE forces the device to transition into Standby mode, all internal memory is cleared and all output stages are switched into their default state (off).
	1		Active	

CONTROL_1 Register
Address: 01h

NCV7704:

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Access type	−	−	RW	RW	RW	RW	RW	−	−	−	−	−	−	−	−	−
Bit name	0	0	HS4.1	HS4.0	HS5	HS6	HS7	0	0	0	0	0	0	0	0	0
Reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

NCV7714:

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Access type	−	−	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	−
Bit name	0	0	HS4.1	HS4.0	HS5	HS6	HS7	LS ECFB	DAC5	DAC4	DAC33I1.833 591.024 26.872 .9 .T336.309 5697.3163I1.833 5					

CONTROL_3 Register

Address: 03h

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Access Type	−	RW	RW	RW	RW	−	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Bit name	0	OCR4	OCR5	OCR6	OCR7	0	OUT4 PWM2	OUT5 PWM1	OUT6 PWM2	OUT7 PWM1	OCRF	OVUVR	IS3	IS2	IS1	IS0
Reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	OCRx		Description	Remark
Overcurrent Recovery	0	default	Overcurrent Recovery disabled	During an overcurrent event the overcurrent status bit STATUS_0/2.OCx is set and the dedicated output is switched off. (The global multi bit UOV_OC is set, also). When the overcurrent recovery bit is enabled, the output will be reactivated automatically after a programmable delay time (CONTROL_3.OCRF).
	1		Overcurrent Recovery enabled	

	OUTx PWM		Description	Remark
PWM1/2 Selection	0	default	PWMx not selected	For the HS outputs it is possible to select the PWM input pins PWM1, PWM2 or internal PWMI unit (OUT4−6 only). In this case the dedicated output (selected in CONTROL_1 register) is on if the PWM input signal is high. OUT4 and OUT6 are controlled by PWM2, OUT5 and OUT7 are controlled by PWM1.
	1		PWMx selected	

	OCRF		Description	Remark
Overcurrent Recovery Frequency Selection	0	default	Slow Overcurrent recovery mode	If the overcurrent recovery bit is set, the output will be switched on automatically after a delay time. The recovery behavior of OUT4 in bulb mode is not affected by this bit.
	1		Fast Overcurrent recovery mode	

	OVUVR		Description	Remark
Over− / Under−voltage Recovery	0	default	Over− and undervoltage recovery function enabled	If the OV/UV recovery is disabled by setting OVUVR=1, the status register STATUS_2 bits VSOV or VSUV have to be cleared after an OV/UV event.
	1		No over− and undervoltage recovery	

	IS3	IS2	IS1	IS0	Description	Remark
	0	0	0	0	current sensing deactivated	
Current Sensing Selection						The current in all high−side power stages (except of OUT1/2/3) can be monitored at the bidirectional multifunctional pin ISOUT/PWM2. This pin is a multifunctional pin and can be activated as output by setting the current selection bits IS[3:0]. The selected high−side

PWM_5/6 Register
Address: 09h

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0D0

STATUS_0 Register

Address: 10h

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Access Type	R/RC	R/RC	R/RC	R/RC	R/RC											

STATUS_2 Register
Address: 12h

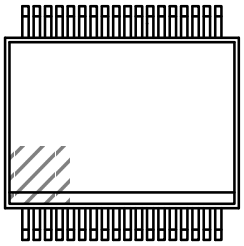
NCV7704:

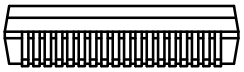
Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Access type	−	−	R/RC	R/RC	R/RC	R/RC	R/RC	R/RC	R/RC	R/RC	−	−	R/RC	R/RC	−	−
Bit name	0	0	OC HS4	ULD HS4	OC HS5	ULD HS5	OC HS6	ULD HS6	OC HS7	ULD HS7	0	0	VSUV	VSOV	0	0
Reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

SSOP36 EP
CASE 940AB
ISSUE A

DATE 19 JAN 2016

SCALE 1:1





DIM	MILLIMETERS MIN	MAX
A		2.65
A1	---	0.10
b	0.18	0.30
c	0.23	0.32
D2		
E2	3.10	4.10
e	0.50	
h	0.25	0.75
L	0.50	0.90