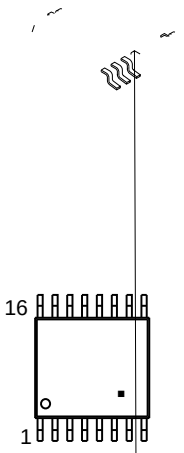

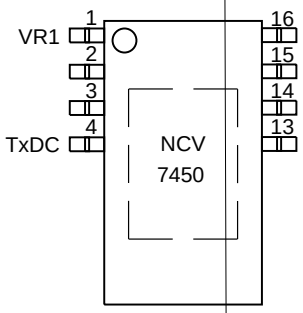

ORDERING INFORMATION

Device	Package	Shipping†
NCV7450DB0R2G	TSSOP16−EP (Pb−Free)	4000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

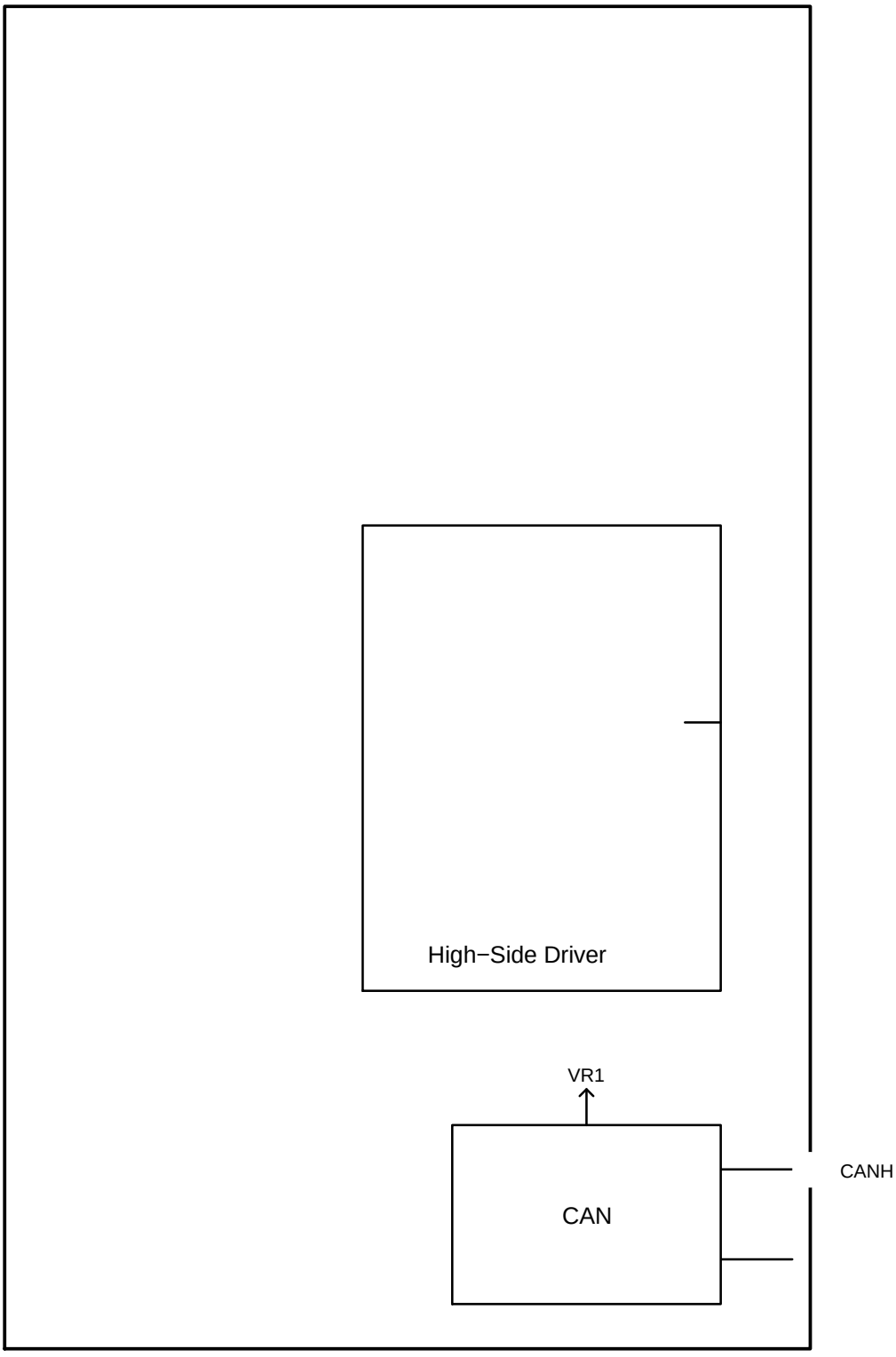

Figure 2. Block Diagram

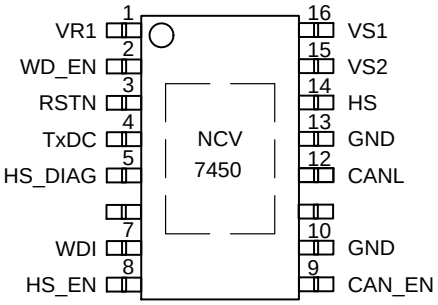
1
VR1
2
WD_EN
3
RSTN
4
TxDC
5
HS_DIAG
7
WDI
8
HS_EN
16
VS1
15
VS2
14
HS
13
GND
12
CANL
10
GND
9
CAN_EN
NCV
7450

Table 4. RECOMMENDED OPERATING RANGES

Symbol	Rating	Min	Max	Unit
VS1	Functional supply voltage	5	28	V
	Supply voltage for valid parameter specification	6	18	V
VS2	Functional supply voltage	4.3	24	V
	Supply voltage for valid parameter specification	6	18	V
VR1	VR1 LDO output voltage	4.9	5.1	V
VdigIO	Digital inputs/outputs voltage	0	VR1	V
HS	High−side driver voltage	0	VS2	V
CANH, CANL	CAN bus pins voltage	−40	40	V
T_J	Junction Temperature	−40	150	°C
T_A	Ambient Temperature	−40	125	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

Table 5. ELECTRICAL CHARACTERISTICS (6 V ≤ Vs1 = Vs2 ≤ 18 V; −40°C ≤ Tj ≤ 150°C; unless otherwise specified.)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
DIGITAL OUTPUT RSTN						
VoutL_RSTN	Low−level output voltage, low VR1/VS1	VR1 > 4.7 V, I(RSTN) = 0.7 mA	−	−	0.4	V
		VR1 > 2 V, VS1 < VR1, I(RSTN) = 0.1 mA	−	−	0.4	
		VS1 > 2 V, I(RSTN) = 0.3 mA	−	−	0.4	
Rpullup_RSTN	Internal pull−up resistor to VR1		5.0	10	19	kΩ
DIGITAL INPUTS TxDC, CAN_EN, WD_EN, HS_EN, WDI						
VinL_pinx	Low−level input voltage (logical “Low”)		0	−	0.8	V
VinH_pinx	High−level input voltage (logical “High”)		2.0	−	VR1	

.)

Typ	Max	Unit
−	+5.0	mA
0	+5.0	μA
2.5	3.0	V
2.5	3.0	V
0	0.1	V
0	0.1	V
0	0.2	V
3.5	4.5	V
1.5	2.25	V
	1.1	VR1
2.25	3.0	V

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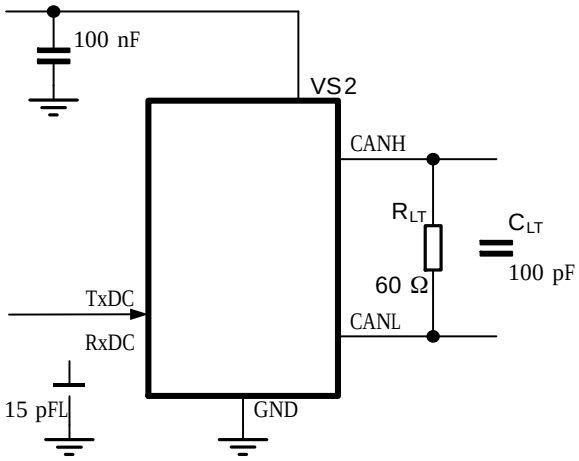
Table 6. ELECTRICAL CHARACTERISTICS (CONTINUED)

(VR1 = 4.75 V to 5.25 V; T_J = −40°C to +150°C; R_{LT} = 60 Ω, C_{LT} = 100 pF, C_1 not used unless specified otherwise.)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
CAN BUS LINES (Pins CANH and CANL)						
$R_{i(cm)\ (CANL)}$	Common−mode input resistance at pin CANL	−2 V ≤ V_{CANH}				


100 nF
VS2
CANH
R_{LT}
C_{LT}
100 pF
60 Ω
TxDC
RxDC
CANL
15 pFL
GND

FUNCTIONAL DESCRIPTION

Supply Concept

The device has two independent supply pins VS1 and VS2. While VR1 regulator and logic control are supplied from VS1, High side driver is supplied from VS2. Both supply lines have to be properly decoupled by filtration capacitors close to the device pins.

As long as VS1 < VS_POR level, all the blocks are in power down mode.

VR1 Low−drop Regulator

VR1 is a low drop output regulator providing 5 V voltage derived

HS Driver

HS high side driver is intended to drive an external load. Its state is directly controlled via HS_EN pin and diagnostics are flagged on HS_DIAG pin (see Table 7).

When the driver is enabled (HS_EN = High), it is protected against an excessive current and temperature and

In case the watchdog is not triggered before the timeout or open window elapses (Figure 11, Figure 12), or trigger is sent within the closed window (Figure 13), RSTN signal is generated and then watchdog restarted in the timeout mode again.

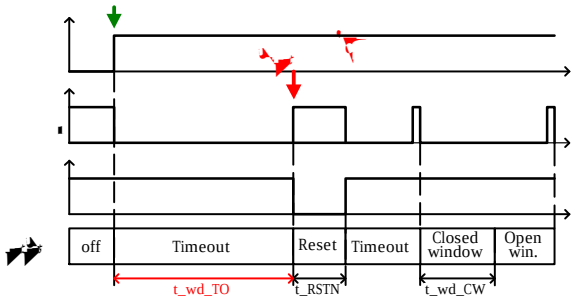


Figure 11. Missed watchdog in Timeout mode

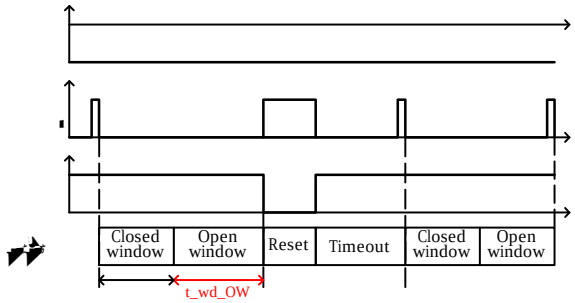


Figure 12. Missed watchdog in Window mode

Table 8. ISO11898−2:2016 PARAMETER CROSS−REFERENCE TABLE

ISO 11898−2:2016 Specification		NCV7450 Datasheet
Parameter	**Notation**	**Symbol**
DOMINANT OUTPUT CHARACTERISTICS		
Single ended voltage on CAN_H	V_{CAN_H}	$V_{o(dom)(CANH)}$
Single ended voltage on CAN_L	V_{CAN_L}	$V_{o(dom)(CANL)}$
Differential voltage on normal bus load	V_{Diff}	$V_{o(dom)(diff)}$
Differential voltage on effective resistance during arbitration	V_{Diff}	$V_{o(dom)(diff)\_arb}$
Optional: Differential voltage on extended bus load range		

Table 8. ISO11898−2:2016 PARAMETER CROSS−REFERENCE TABLE

ISO 11898−2:2016 Specification		NCV7450 Datasheet
Parameter	**Notation**	**Symbol**
OPTIONAL IMPLEMENTATION DATA SIGNAL TIMING REQUIREMENTS for use with bit rates above 2 Mbit/s and up to 5 Mbit/s		
Transmitted recessive bit width @ 5 Mbit/s	$t_{Bit(Bus)}$	$t_{Bit(Vi(diff))}$
Transmitted recessive bit width @ 5 Mbit / s	$t_{Bit(RXD)}$	$t_{Bit(RxD)}$
Received recessive bit width @ 5 Mbit / s	Δt_{Rec}	Δt_{Rec}
MAXIMUM RATINGS OF V_{CAN_H}, V_{CAN_L} AND V_{DIFF}		
Maximum rating V_{Diff}	V_{Diff}	Vmax_diff
General maximum rating V_{CAN_H} and V_{CAN_L}	V_{CAN_H} V_{CAN_L}	V_{CANH} V_{CANL}
Optional: Extended maximum rating V_{CAN_H} and V_{CAN_L}	V_{CAN_H} V_{CAN_L}	NA
MAXIMUM LEAKAGE CURRENTS ON CAN_H AND CAN_L, UNPOWERED		
Leakage current on CAN_H, CAN_L	I_{CAN_H}, I_{CAN_L}	I_{LI}
BUS BIASING CONTROL TIMINGS		
CAN activity filter time, long	t_{Filter}	NA
CAN activity filter time, short	t_{Filter}	t_{wake_filt}
Optional: Wake−up timeout, short	t_{Wake}	t_{wake_to}
Optional: Wake−up timeout, long	t_{Wake}	t_{wake_to}
Timeout for bus inactivity (Required for selective wake−up implementation only)	$t_{Silence}$	NA
Bus Bias reaction time (Required for selective wake−up implementation only)	t_{Bias}	NA

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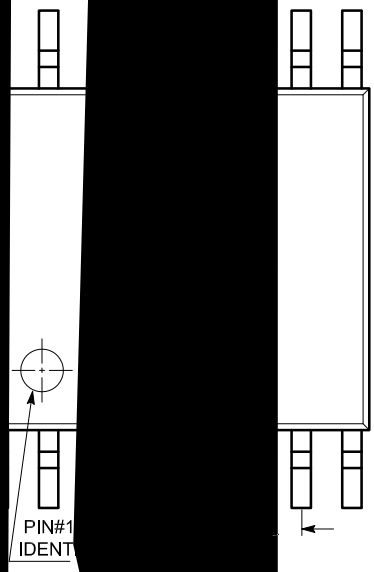

END VIEW

BOTTOM VIEW

S

MBOL	M		M	MAX
A				1.10
A1	0.0			0.15
A2	0.85			0.95
b	0.19			0.30
c	0.13			0.20
D	4.90			5.10
E	6.30			6.50
E1	4.30			4.50
e			SC	
L			EF	
L1	0.45			0.75
N	0.90			1.00
P	6.50			6.70
R	4.60			4.80
	0.37			0.47

LAND PATTERN