NCV7240, NCV7240A, NCV7240B

O L -S R D

The NCV7240 is an automotive eight channel low−side driver providing drive capability up to 600 mA per channel. Output control is via a SPI port and offers convenient reporting of faults for open load (or short to ground), over load, and over temperature conditions. Additionally, parallel control of the outputs is addressable (in pairs) via the INx pins.

A dedicated limp−home mode pin (LHI) enables OUT1−OUT4 while disabling OUT5−OUT8.

Each output driver is protected for over load current and includes an output clamp for inductive loads.

The NCV7240 is available in a SSOP−24 fused lead package.

Features

- 8 Channels
- 600 mA Low−Side Drivers
  - $R_{DS(on)}$ 1.5 Ω (Typ), 3 Ω (Max)
- 16−€

MAXIMUM RATINGS

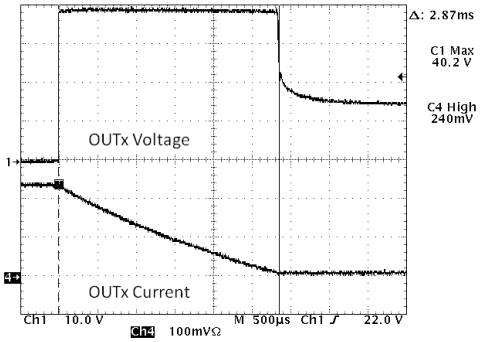
Parameter	Min	Max	Unit
Supply Input Voltage (VDDA, VDD) DC	 −0.3	 5.5	V
Digital I/O pin voltage (EN, LHI, Inx, CSB, SCLK, SI) (SO)	 −0.3 −0.3	 5.5 V_{DD} + 0.3	V
High Voltage Pins (OUTx) DC Peak Transient	 −0.3	 36 44 (Note 1)	V
Output Current (OUTx)	−1	1.3	A
Clamping Energy Maximum (single pulse) Repetitive (multiple pulse) (Note 2)	 − −	 75 −	mJ
Operating Junction Temperature Range	−40	150	°C
Storage Temperature Range	−55	150	°C
ESD Capability, Human body model (100 pF, 1.5 kΩ) (OUTx pins) Human body model (100 pF, 1.5 kΩ) (all other pins)	 −4000 −2000	 4000 2000	V
ESD Capability Machine Model (200 pF)	 −200	 200	V
AECQ10x−12−RevA Short Circuit Reliability Characterization	 Grade A	 −	

PACKAGE

Moisture Sensitivity Level	MSL2		−
Lead Temperature Soldering: SMD style only, Reflow (Note 3) Pb−Free Part 60 − 150 sec above 217°C, 40 sec max at peak		265 peak	°C
Package Thermal Resistance (per JESD51) SSOP−24 Junction−to−Ambient (1s0p + 600 mm^2 Cu) (Note 4) Junction−to−Ambient (2s2p) (Notes 4 and 5) Junction−to−Pin (pins 1, 2, 11, 12) (Note 6)		 68 62 30	°C/W

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Internally limited. Specification applies to unpowered and powered modes. (0 V to VDDA, 0 V to VDD)
2. Testing particulars, 2M pulses, V_{bat} = 15 V, 63 Ω, 390 mH, T_A = 25°C. (See Figure 4)
3. For additional information, see or download ON Semiconductor's Soldering and Mounting Techniques Reference Manual, SOLDERRM/D and Application Note AND8083/D.
4. 76 mm x 76 mm x 1.5 mm FR4 PCB with additional heat spreading copper (2 oz) of 600 mm^2, LS1 to LS8 dissipating 100 mW each. No vias.
5. Include 2 inner 1 oz copper layers. No vias.
6. One output dissipating 100 mW.



ELECTRICAL CHARACTERISTICS

ELECTRICAL CHARACTERISTICS (3.0 V < VDD < VDDA, 4.5 V < VDDA (Note 7) < 5.5 V, −40°C ≤ T_J ≤ 150°C, EN = VDD, LHI = 0 V unless otherwise specified).

Symbol	Characteristic	Conditions	Min	Typ	Max	Unit
SPI TIMING (all timing specifications measured at 20% and 80% voltage levels)						
t_{SO_DIS}	SO Output Disable Time (CSB rising to SO tri−state)	Figure 5, #9 Not ATE tested	−	−	200	ns
t_{SO_valid}	SO Output Data Valid Time with capacitive load	Figure 5, #10, C_{load} = 50 pF Not ATE tested	−	−	100	ns

7. Reduced performance down to 4 V provided VDDA Power−On Reset threshold has not been breached.
8. Each output driver is protected by its' own individual thermal sensor.
9. Input signals H→L→H greater than 50usec are guaranteed to be detected.

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

TYPICAL PERFORMANCE GRAPHS

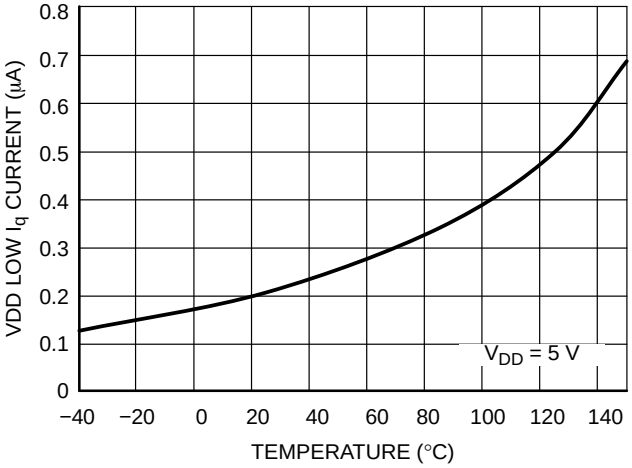


Figure 6. VDD Low I_q Current vs. Temperature

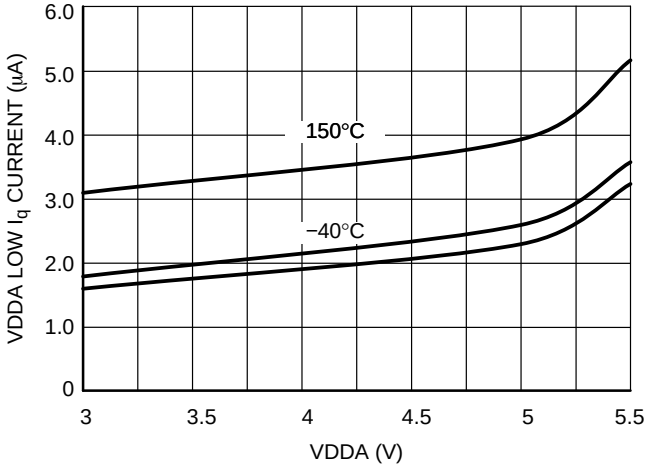


Figure 7. VDDA Low I_q Quiescent Current vs. VDDA

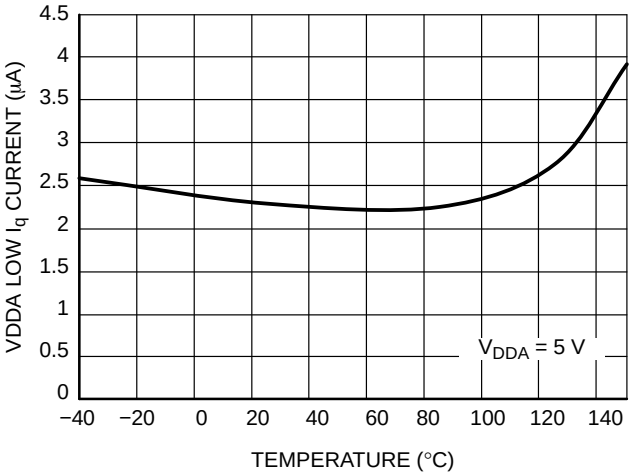


Figure 8. VDDA Low I_q Current vs. Temperature

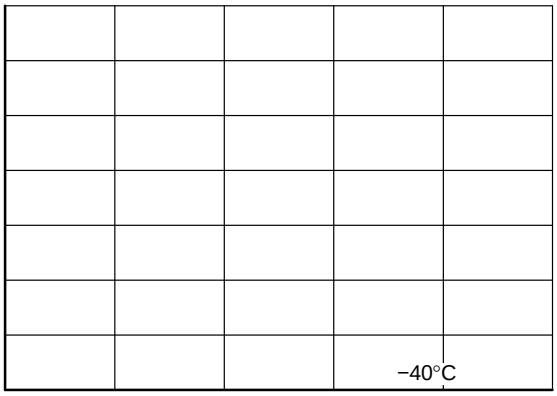
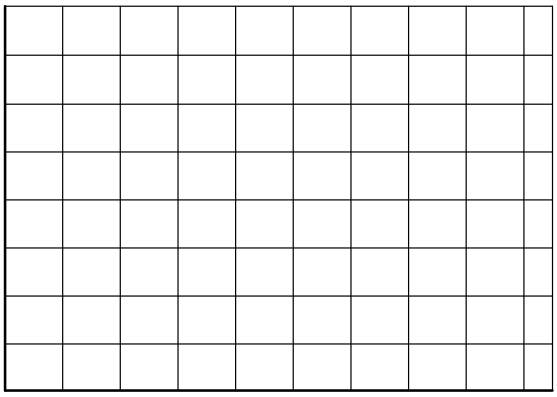


Figure 9. VDD Low I_q Current vs. VDD



TYPICAL PERFORMANCE GRAPHS

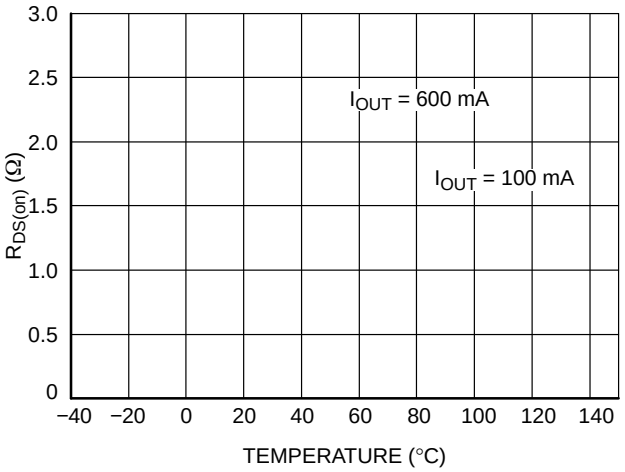


Figure 12. Output $R_{DS(on)}$ vs. Temperature

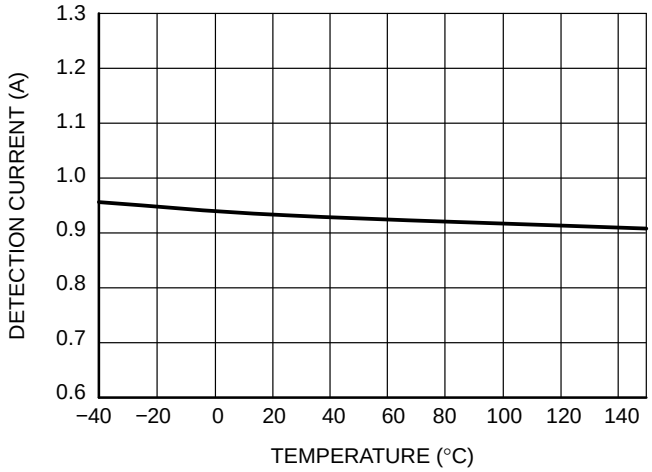


Figure 13. Over Load Current vs. Temperature

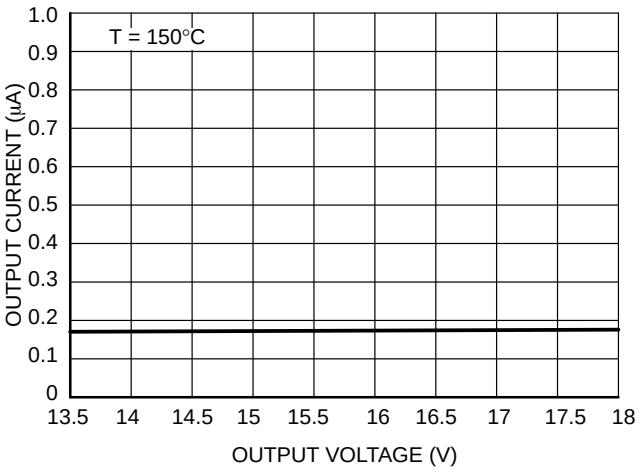


Figure 14. Output Leakage vs. Voltage (150°C)

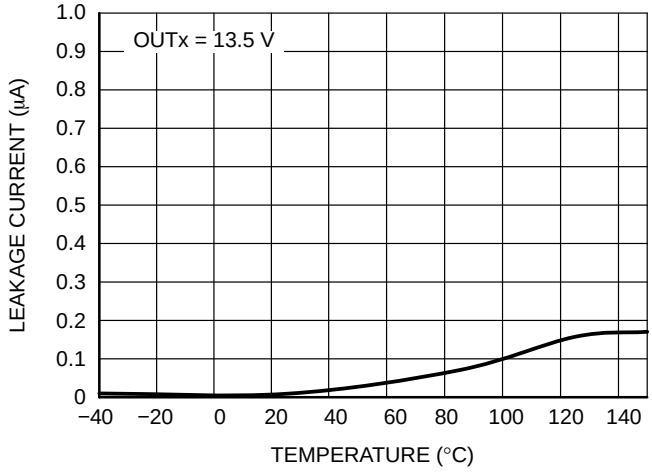


Figure 15. Output Leakage vs. Temperature

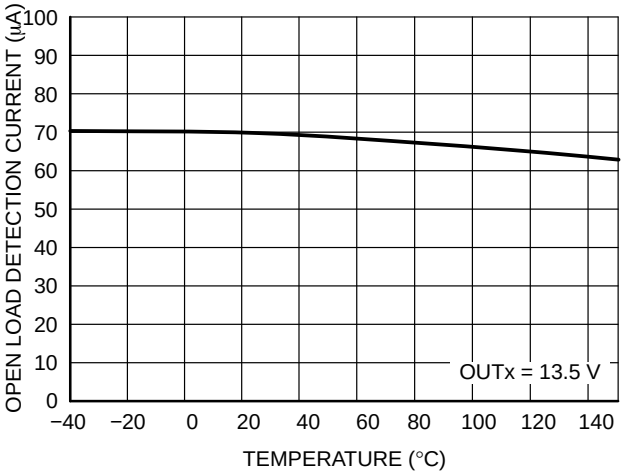


Figure 16. Output Load Detection Current vs. Temperature

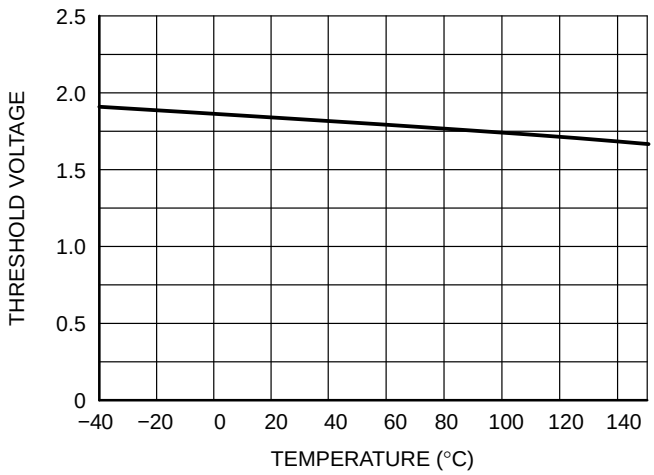


Figure 17. Open Load Detection Voltage vs. Temperature

TYPICAL PERFORMANCE GRAPHS

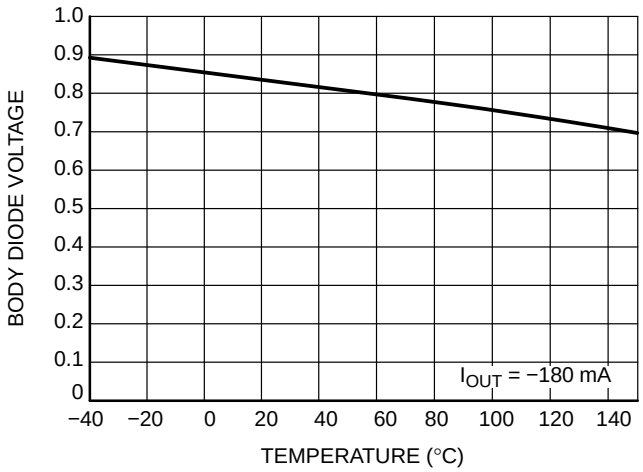


Figure 18. Output Body Diode Voltage vs. Temperature

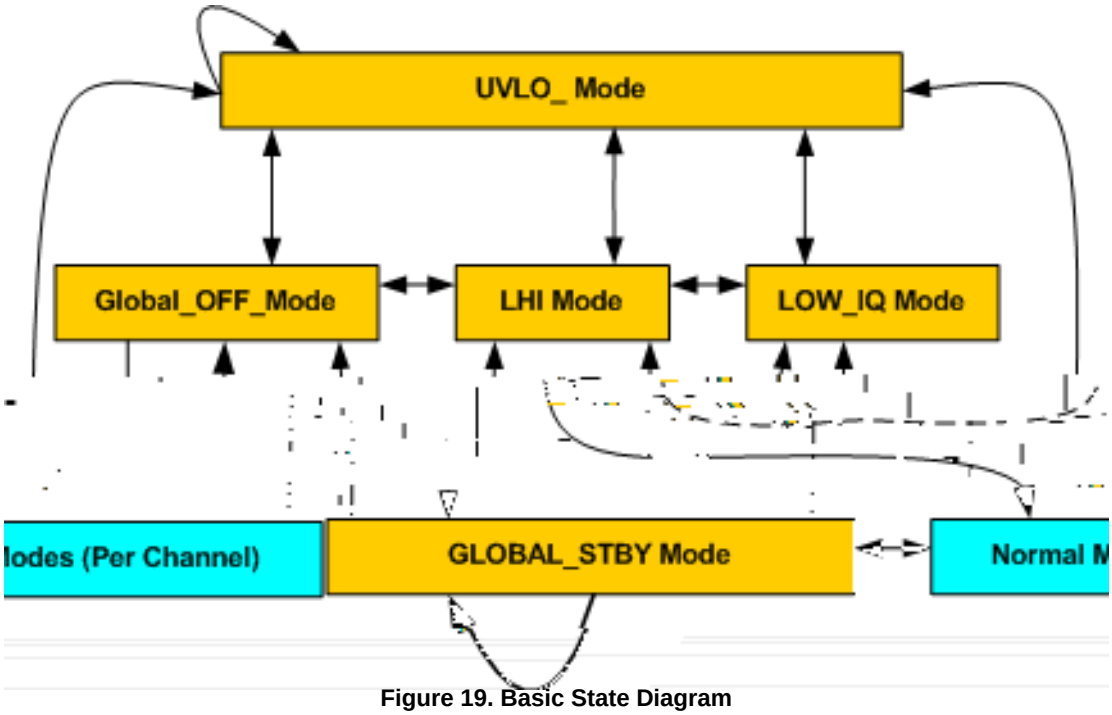


Figure 19. Basic State Diagram

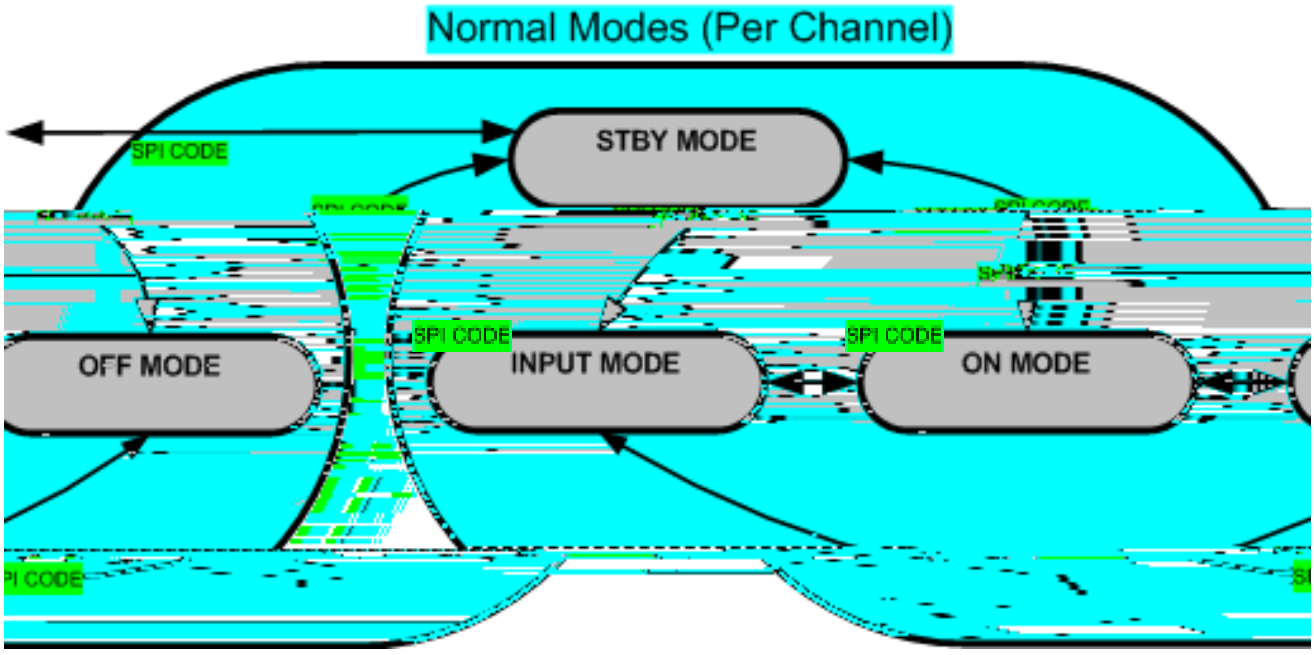
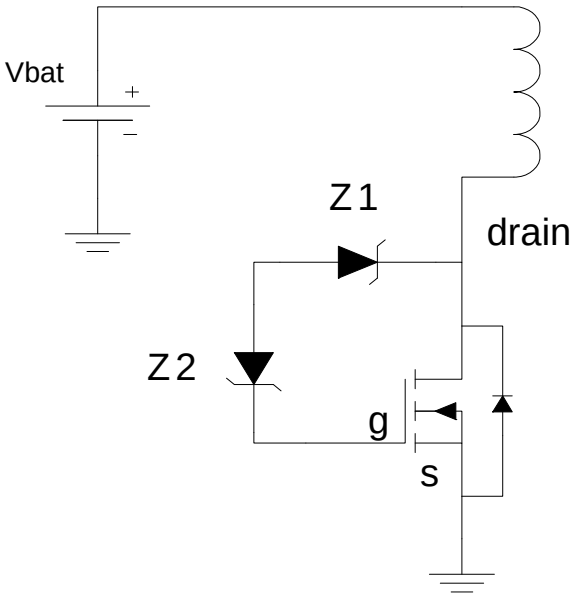
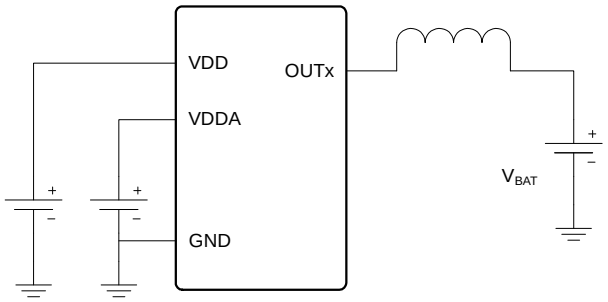
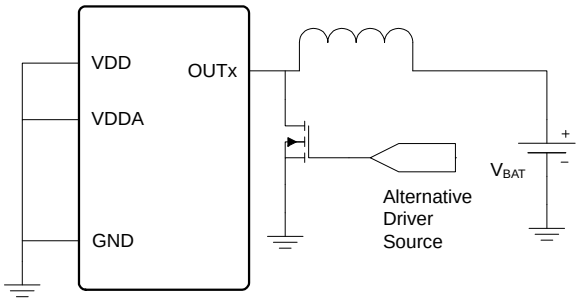


Figure 20. Normal Operation State Diagram



$$Vdrain = VZ1 + VZ2 + Vgs$$

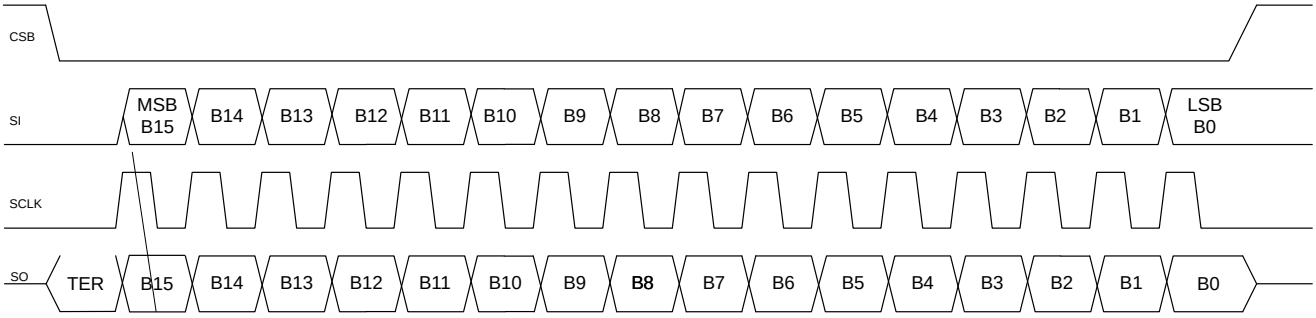




SO Output Driver

TER Information Retrieval

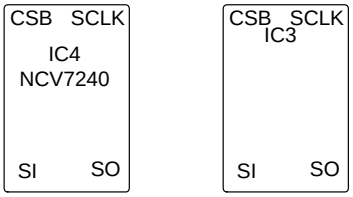
TER information retrieval is as simple as bringing CSB high−to−low. No clock signals are required.



DAISY CHAIN SETUP

Serial Connection

Daisy chain setups are possible with the NCV7240. The serial setup shown in Figure 31 highlights the NCV7240 along with any 16 bit device using a similar SPI protocol. Particular attention should be focused on the fact that the first 16 bits which are clocked out of the SO pin when the CSB pin transitions from a high to a low will be the Diagnostic Output Data from the Fault Output Register. These are the bits representing the status of the IC. Additional programming bits should be clocked in which follow the Diagnostic Output bits. The timing diagram shows a typical transfer of data from the microprocessor to the SPI connected IC's.



Stepper Motor Operation

The NCV7240 device is capable of driving stepper motors. Each stepper motor requires 4 low−side drive outputs. Consequently, each NCV7240 device is capable of driving two stepper motors. Figure 36 below illustrates a Unipolar stepper motor setup. For proper operation, the code listed in Table 3 should be used (and repeated) for one way operation (clockwise).

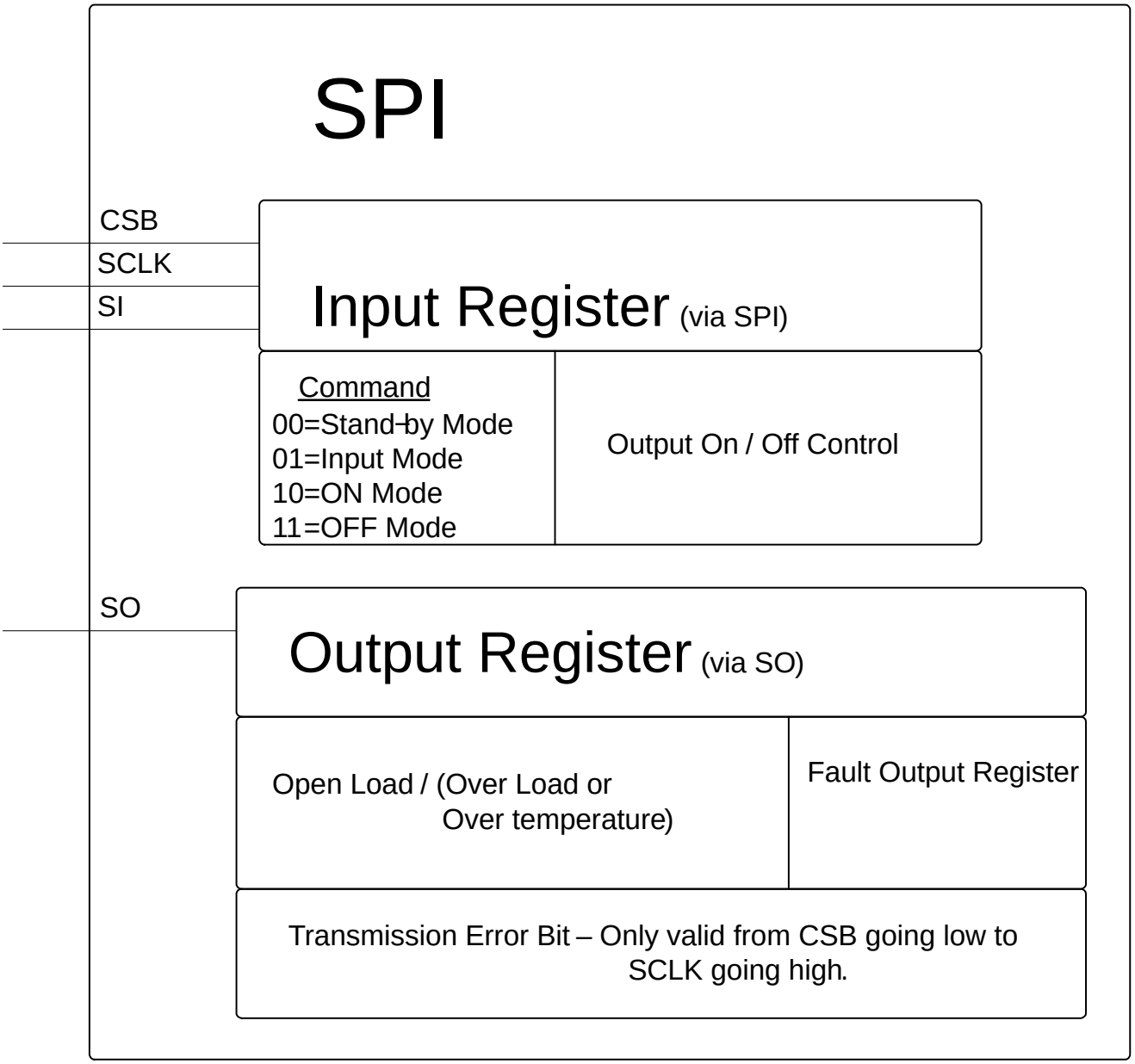


Figure 38. SPI Register Overview

Figure 38 displays the functions controlled and reported via the SPI port.
The input register controls the input source (parallel or SPI) and the SPI input data.
The output register transmits the output fault bits and the frame detection integrity.

SI SPI Inp t D t (16- t t t t)

The 16−bit data received (SI) is decoded into instructions for each channel per the table below.
After a power−on reset, all register bits are set to a 1.

Table 4. SPI INPUT DATA

Channel 8		Channel 7		Channel 6		Channel 5		Channel 4		Channel 3		Channel 2		Channel 1	
MSB														LSB	
B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0

INPUT DATA REGISTER

Field	Bits	Description		
channel x (x = 1−8)	15, 14 13, 12 11, 10 9, 8 7, 6 5, 4 3, 2 1, 0	Command		
		00	Channel Stand−by Mode Fast channel turn off Corresponding Channel Fault Register reset	
			Diagnostic Current	Disabled
		01	Input Mode Channel Input directed to INx. (reference PWM operation section).	
			Diagnostic Current	Enabled in OFF State.
		10	ON Mode Channel turned on.	
			Diagnostic Current	Disabled
		11	OFF Mode Channel turned off.	
			Diagnostic Current	Enabled (Disabled after POR)*

*For proper LED load operation.

SO (fault diagnostic retrieval)

Output fault diagnostics from the output fault diagnostic register are shifted out on any 16 bit word clocked into Serial Input (SI).
Only output fault diagnostics and frame detection errors are available through the serial output (SO).

Table 5. SPI OUTPUT DATA

TER	OL8	D8	OL7	D7	OL6	D6	OL5	D5	OL4	D4	OL3	D3	OL2	D2	OL1	D1

FAULT DIAGNOSTIC REGISTER

Field	Bits	Description
TER	CSB high−to−low prior to 1st SCLK low−to−high	Transmission Error. 0 Successful transmission in previous communication. 1 Frame detection error in previous transmission or exiting Limp Home Mode, exiting UVLO Mode, or exiting Low Iq mode to Global Off Mode.
Oln (n = 1 − 8)	1, 3, 5, 7, 9, 11, 13, 15	Open Load 0 Normal Operation 1 Fault detected
Dn (n = 1 − 8)	0, 2, 4, 6, 8, 10, 12, 14	Over Load or Over Temperature 0 Normal Operation 1 Fault detected

Table 6. FAULT CONDITIONS

Output Fault Condition	Fault Memory	Miscellaneous
Open Load	Latched	Detected in Driver Off State (1.75 V [Typ] threshold) when detection is enabled. Reported in Output Fault Diagnostics Register until cleared via the SPI port. Output will maintain turn−on capability.
Short to Ground	Latched	Detected as part of the Open Load circuitry described above.
Short to V_{bat}	N/A	Protected via Over Load and Over Temperature functions.
Over Load	Latched	Detected in Driver On State 0.6 A [min], 1.3 A [max]. A latched off condition must be cleared via the SPI port before it can be turned on.
Over Temperature	Latched	Detected in IC On State (T_J = 175°C [Typ]) A latched off condition must be cleared via the SPI port before it can be turned on.

DEVICE ORDERING INFORMATION

Part Number	Package Type	Shipping†
NCV7240DPR2G	SSOP−24 (Pb−Free)	2500 / Tape & Reel
NCV7240ADPR2G		
NCV7240BDPR2G		

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.