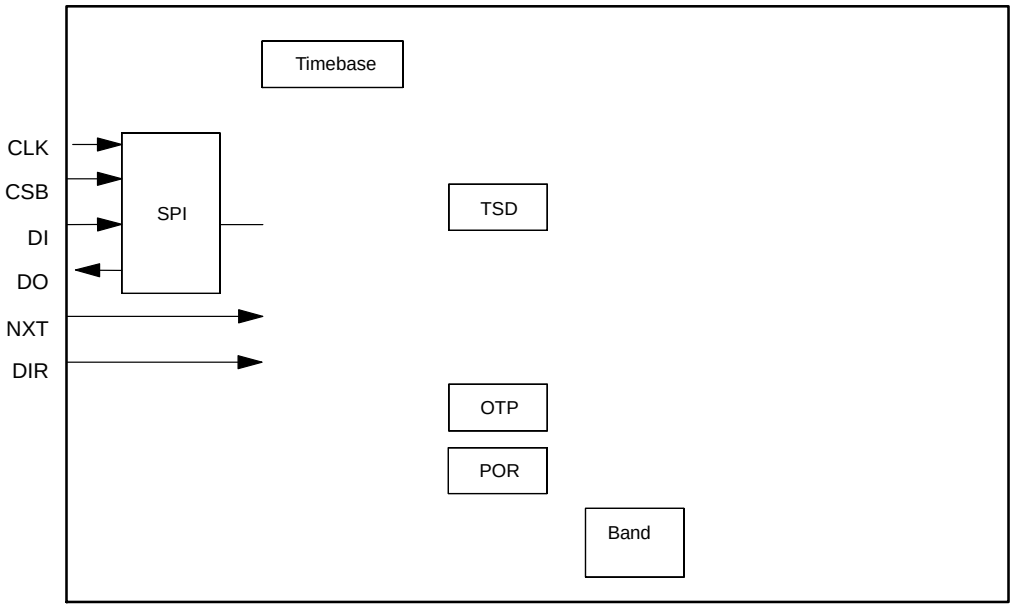
Publication Order Number:


Timebase
CLK
CSB
DI
DO
NXT
DIR
SPI
TSD
OTP
POR
Band

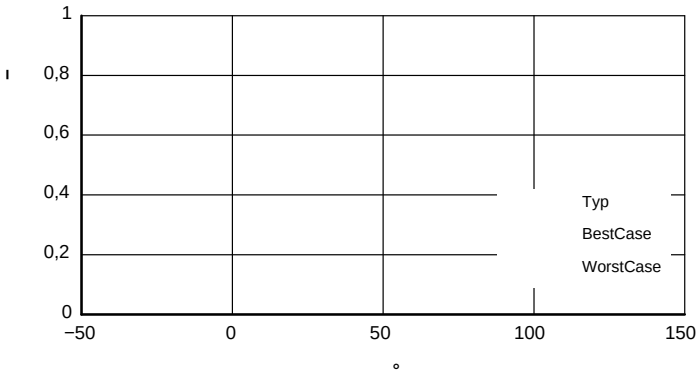
Supply voltage (Note 6)	V_{BB}	−0.3	+40	V
Digital input/outputs voltage	V_{IO}	−0.3	+6.0	V
Junction temperature range (Note 7)	T_j	−50	+175	°C

The following figure gives the equivalent schematics of the user relevant inputs and outputs. The diagrams are simplified representations of the circuits used.

(continued)

V_{inL}	CSB	Logic low input level, max				0.8	V

15. Thermal warning and low temperature level are derived from thermal shutdown ($T_{tw} = T_{tsd} – 20°C$, $T_{low} = T_{tsd} – 137°C$).
16. No more than 100 cumulated hours in life time above T_{tw}.
17. Parameter guaranteed by trimming relevant OTPs in production test at 160°C and VBB = 14 V.
18. Dynamic current is with oscillator running, all analogue cells active. Coil currents 0 mA, SPI active, ERRB inactive, no floating inputs.
19. All outputs unloaded, no floating inputs. Not tested in production, guaranteed by device characterization.
20. Pin VDD must not be used for any external supply.
21. The SPI registers content will not be altered above this voltage.
22. Maximum allowed drain current that the output can withstand without getting damaged. Not tested in production.



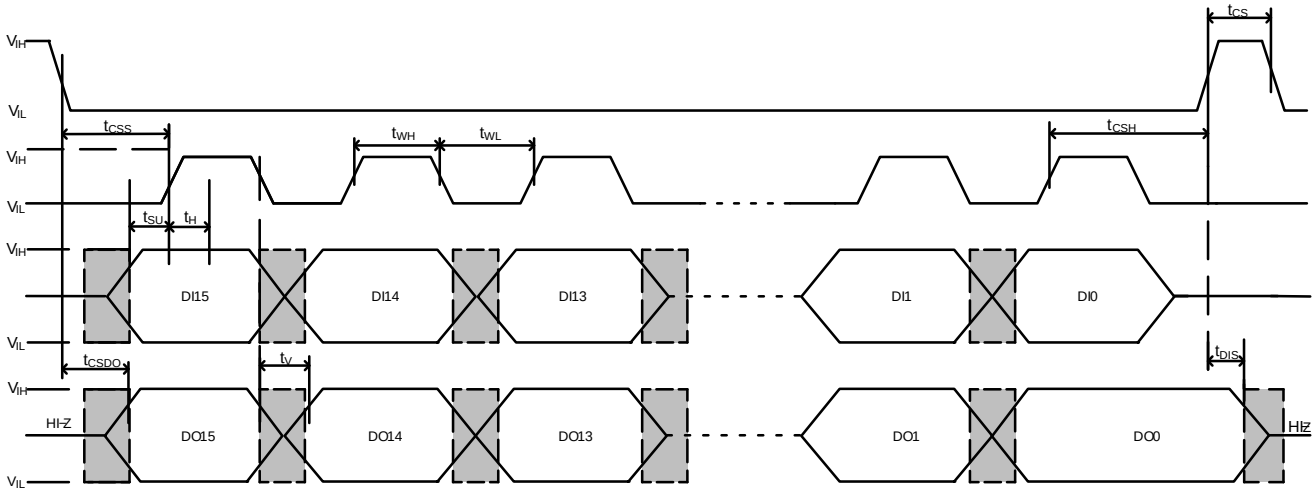
t_{DIR_SET}	NXT, DIR	NXT set time, following change of DIR		25			μs
t_{DIR_HOLD}		NXT hold time, before change of DIR		25			μs

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

23. Derived from the internal oscillator.

t_{CSS}	CSB setup time (Note 24)	0.5			μs
t_{CSH}	CSB hold time	0.5			μs
t_{CS}	CSB high time	1			μs
t_{WL}	CLK low time	0.5			μs
t_{WH}	CLK high time	0.5			μs
t_{SU}	DI set up time, valid data before rising edge of CLK	0.25			μs
t_H	DI hold time, hold data after rising edge of CLK	0.275			μs
t_{CSDO}	CSB low to DO valid			0.23	μs
t_{DIS}	Output (DO) disable time (Note 25)	0.08		0.32	μs
$t_{V1\rightarrow0}$	Output (DO) valid (Note 25)			0.32	μs
$t_{V0\rightarrow1}$	Output (DO) valid (Note 26)			0.32 + t(RC)	μs

24. After leaving sleep mode an additional wait time of 250 μs is needed before pulling CSB low.
25. SDO low–side switch activation time.
26. Time depends on the SDO load and pull–up resistor.



Two H−bridges are integrated to drive a bipolar stepper motor. Each H−bridge consists of two low−side N−type MOSFET switches and two high−side P−type MOSFET switches. One PWM current control loop with on−chip current sensing is implemented for each H−bridge. Depending on the desired current range and the micro−step position at hand, the $R_{DS(on)}$ of the low−side transistors will be adapted to maintain current−sense accuracy. A comparator compares continuously the actual winding current with the requested current and feeds back the information to generate a PWM signal, which turns on/off the H−bridge switches. The switching points of the PWM duty−cycle are synchronized to the on−chip PWM clock.

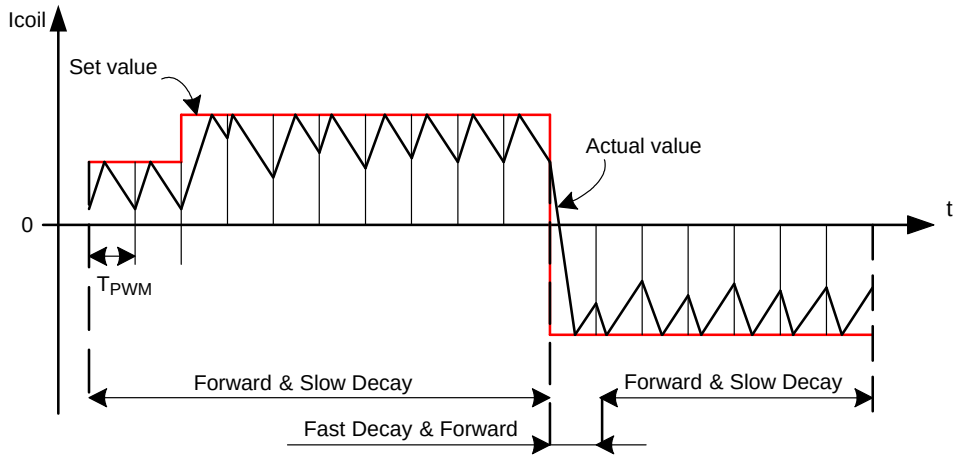
The PWM frequency will not vary with changes in the supply voltage. Also variations in motor−speed or load−conditions of the motor have no effect. There are no external components required to adjust the PWM frequency. In order to avoid large currents through the H−bridge switches, it is guaranteed that the top− and bottom−switches of the same half−bridge are never conductive simultaneously (interlock delay).

In order to reduce the radiated/conducted emission, voltage slope control is implemented in the output switches.

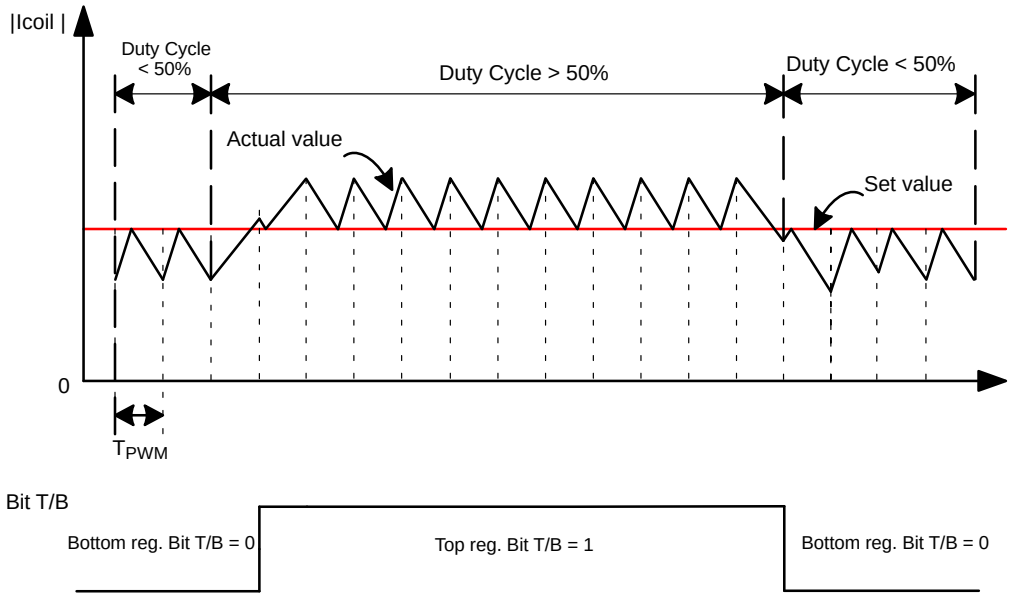
A protection against shorts on motor lines is implemented. When excessive voltage is sensed across a MOSFET for a time longer than the required transition time, then the MOSFET is switched−off.

The H−bridges and PWM control can be disabled (high−impedance state) by means of a bit <MOTEN> in the SPI control registers. <MOTEN>=0 will only disable the drivers and will not impact the functions of NXT, DIR, SPI bus, etc. The H−bridges will resume normal PWM operation by writing <MOTEN>=1 in the SPI register. PWM current control is then enabled again and will regulate current in both coils corresponding with the position given by the current translator.

The PWM generation is in steady−state using a combination of forward and slow−decay. For transition to lower current levels, fast−decay is automatically activated to allow high−speed response. The selection of fast or slow decay is completely transparent for the user and no additional parameters are required for operation.

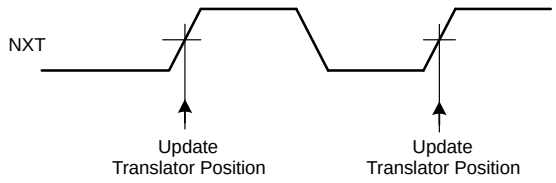


If during regulation the set point current is not reached before 75% of t_{pwm}, the duty cycle of the PWM is adapted automatically to > 50% (top regulation) to maintain the requested average current in the coils. This process is completely automatic and requires no additional parameters for operation. The state of the duty cycle adaptation mode is represented in the internal T/B bits for both motor windings X and Y. Figure 9 gives a representation of the duty cycle adaptation.


|Icoil |
Duty Cycle
< 50%
Duty Cycle > 50%
Duty Cycle < 50%
Actual value
Set value
0
T_{PWM}
Bit T/B
Bottom reg. Bit T/B = 0
Top reg. Bit T/B = 1
Bottom reg. Bit T/B = 0

Whenever

The translator position can be read and set by the SPI register <MSP[5:0]>. This is a 6−bit number equivalent to the 1/16th micro−step from Table 9: Translator Table. The translator position is updated immediately following a next micro−step trigger (see below).



The direction of rotation is selected by means of input pin DIR and its “polarity bit” <DIRP> (SPI register). The polarity bit <DIRP> allows changing the direction of rotation by means of only SPI commands instead of the dedicated input pin.

Direction = DIR−pin EXOR <DIRP>

Positive direction of rotation means counter−clockwise rotation of electrical vector Ix + Iy. Also when the motor is disabled (<MOTEN>=0), both.00u388ounter2

0	59	81
1	71	98
2	84	116
3	100	138
4	119	164
5	141	194
6	168	231
7	200	275
8	238	327
9	283	389
A	336	462
B	400	550
C	476	655
D	566	778
E	673	925
F	800	1100

Whenever <IMOT[3:0]> is changed, the new coil currents will be updated immediately at the next PWM period.

In case the motor is disabled (<MOTEN>=0), the logic is functional and will have effect on NXT/DIR operation (not on the H−bridges). When the chip is in sleep mode, the logic is not functional and as a result, the NXT pin and DIR pin will have no effect.

Note: The hard−reset function is embedded by means of a special sequence on the DIR pin and NXT pin, see also Hard−Reset Function chapter.

–

The NCV70517 has one undervoltage threshold level UV (see Table 6 − DC Parameters).

For slow speed or when a motion ends at a full step position (there is an absence of next NXT trigger), the end of the zero crossing is taking too long or is non−existing. In this case, the back emf voltage is taken the latest at “stall time−out” time and this value is used also for comparison with <StThr[3:0]> stall threshold to detect stall situation. The “stall time−out” is set in SPI by means of <StTo[7:0]> register and is expressed in counts of $4/f_{pwm}$ (See AC Parameters), roughly in steps of 0.2 ms. If <StTo[7:0]> = 0, time−out is not active.

At the end of the current zero crossing phase the internal circuitry compares measured back emf voltages with <StThr[3:0]> register, which determines threshold for stall detection. The last sample of back emf taken before end of zero crossing phase is used for stall detection in normal mode as well as in enhanced back emf mode. When <StThr[3:0]> = 0 then stall detection is disabled. When value of <StThr[3:0]> is different from 0 and measured back emf signal is lower than <StThr[3:0]> threshold for 2 succeeding coil current zero−crossings (including both X and Y coil), then the <STALL> bit in SPI status register 1 is set, the current translator table goes 135 degrees in opposite direction and the ERRB pin is pulled down, IMOT is maintained. Direction has to change its state at least once and then <STALL> bit can be cleared by reading the status register 1. With stall bit cleared, the chip reacts on “Next Micro−step Triggers” and ERRB pin becomes inactive again.

Notes:

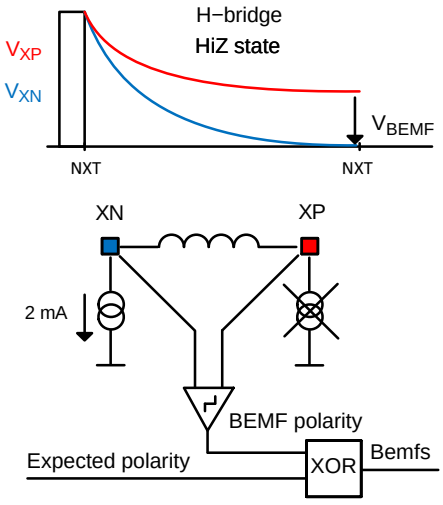
1. Used stall detection is covered by patent US 8,058,894B2
2. As the stall threshold register <StThr[3:0]> is 4 bits wide, the 4 MSBs of 5−bit <Bemf[4:0]> register are taken for comparison

Stall detection and Bemf measurement are performed only when Speed register value <Sp[7:0]> is less than or equal to Speed threshold register value <SpThr[7:0]>.

Stall detection is disabled if time between two consecutive NXT pulses is lower than 74.5 μs (PWMJen = 0) or 80 μs (PWMJen = 1).

Range and resolution of Speed register and Speed threshold register are 0 to 5100 us and 20 us/digit for half stepping mode. Accuracy of speed (time) measurement is given by the accuracy of the internal oscillator.

If measured back emf voltage has not expected polarity, the back emf sign flag <Bemfs> is set. Motor pin, where lower voltage is expected, is tied to GND by pull down current. Sign is determined by comparator, which compares the polarity of voltage measured over the coil with expected polarity of voltage.



The last measured back emf value <Bemf[4:0]>, sign flag <Bemfs> and coil where the last back emf sample was taken <Bemfcoil> can be read out via SPI.

	BemfGain = 0	BemfGain = 1
0	Disable	Disable
1	0.48	0.24
2	0.96	0.48
3		

The NCV70517 stepper driver features an enhanced diagnostic

This is an open drain output to flag a problem to the external microcontroller. The signal on this output is active low and the logic combination of:

NOT(ERRB) = (<SPI> OR <ELDEF> OR <TSD> OR <TW> OR <STALL> OR (BemfIntEn AND BemfRes) OR <UV> OR (*)reset state) AND not (**)sleep mode

Note (*) reset state: After a power−on or a hard−reset, the ERRB is pulled low during t_{hr_err} (Table 7 − AC Parameters).

Note (**) sleep mode: In sleep mode the ERRB is always inactive (high).

The motor driver can be put in a low−power consumption mode (sleep mode). The sleep mode is entered automatically after a power−on or hard reset and can also be activated by means of SPI bit <SLP>. In sleep−mode, all analog circuits are suspended in low−power, logic output pin ERRB is disabled (ERRB has no function) and none of the input pins is functional with the exception of pin CSB. Only CSB pin can wake−up the chip to normal mode (i.e. clear bit <SLP>) by means of a low pulse with a specified width within t_{csb_with} time. Time t_{wu} (see Table 7 − AC Parameters) is needed to restore all analog and digital circuits after wake−up.

Notes:

- The hard−reset function is disabled in sleep mode.
- The CSB low pulse width has to be within t_{csb_with}, (see Table 7 − AC Parameters) to guarantee a correct wake−up.

– –

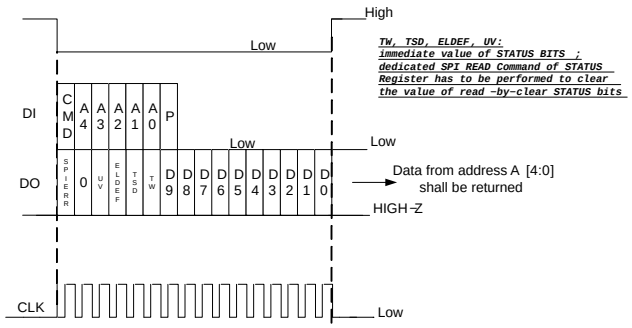
After a power−on or a hard−reset, a flag <HR> in the SPI status

diagnostic check (copy of the main detected errors, see Figure 18 and Figure 19 for details),

- In case of previous SPI error or after power−on−reset, only the MSB bit will be 1, followed by zeros.

If parity bit in the frame is wrong, device will not perform command and <SPI> flag will be set.

The frame protocol for the ***read operation***:




```
P  =  not(CMD xor A4 xor A3 xor A2 xor A1 xor A0)
```

Referring to the previous picture, the read frame coming from the master (into the DI) is composed from the following fields:

- Bit[15] (MSB): CMD bit = 0 for read operation,
- Bits[14:10]: 5 bits READ ADDRESS field,
- Bit[10]: frame parity bit. It is ODD parity formed by the negated XOR of all other bits in the frame,
- Bits [8:0]: 9 bits zeroes field.

Device in the same frame provides to the master (on the DO) data from the required address (in frame response), thus achieving the lowest communication latency.

(continued)

IMOT[3:0]	Bits [3:0] – ADDR_0x01 (CR1)	Current amplitude
PWMJen		

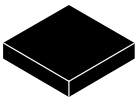
PAR	Bit 8 – ADDR_0x05 (SR1)	Parity bit for SR1
SL	Bit 7 – ADDR_0x05 (SR1)	Step loss register
HR	Bit 6 − ADDR_0x06 (SR2)	Hard reset flag: 1 indicates a hard reset has occurred
ELDEF	Bit 5 – ADDR_0x05 (SR1)	Eletrical defect: Short circuit was detected (at least one of the SHORTij individual bits is set) or Open Coil X or Y was detected
TAMB	Bit 4 – ADDR_0x05 (SR1)	Temperature below T_{low} level − Iboost function can be activated
UVW	Bit 3 – ADDR_0x06 (SR2)	Under−voltage warning – UV threshold hit
TW	Bit 2 – ADDR_0x05 (SR1)	Thermal warning
UV	Bit 1 – ADDR_0x05 (SR1)	Under voltage detection – action taken according to UVact bit
Stall	Bit 0 – ADDR_0x05 (SR1)	Stall detected by the internal algorithm
PAR	Bit 8 – ADDR_0x06 (SR2)	Parity bit for SR2
SPI	Bit 6 – ADDR_0x05 (SR1)	SPI error: no multiple of 16 rising clock edges between falling and rising edge of CSB line
TSD	Bit 5 – ADDR_0x05 (SR1)	Thermal shutdown
OPENX	Bit 4 – ADDR_0x06 (SR2)	Open Coil X detected
SHRTXPB	Bit 3 – ADDR_0x06 (SR2)	Short circuit detected at XP pin towards ground (Bottom)
SHRTXNB	Bit 2 – ADDR_0x06 (SR2)	Short circuit detected at XN pin towards ground (Bottom)
SHRTXPT	Bit 1 – ADDR_0x06 (SR2)	Short circuit detected at XP pin towards supply (Top)
SHRTXNT	Bit 0 – ADDR_0x06 (SR2)	Short circuit detected at XN pin towards supply (Top)
PAR	Bit 8 – ADDR_0x07 (SR3)	Parity bit for SR3
NXTpin	Bit 6 – ADDR_0x07 (SR3)	Read out of NXT pin logic status
DIRpin	Bit 5 – ADDR_0x07 (SR3)	Read out of DIR pin logic status
OPENY	Bit 4 – ADDR_0x07 (SR3)	Open Coil Y detected
SHRTYPB	Bit 3 – ADDR_0x07 (SR3)	Short circuit detected at YP pin towards ground (Bottom)
SHRTYNB	Bit 2 – ADDR_0x07 (SR3)	Short circuit detected at YN pin towards ground (Bottom)
SHRTYPT	Bit 1 – ADDR_0x07 (SR3)	Short circuit detected at YP pin towards supply (Top)
SHRTYNT	Bit 0 – ADDR_0x07 (SR3)	Short circuit detected at YN pin towards supply (Top)
PAR	Bit 8 – ADDR_0x08 (SR4)	Parity bit for SR4
DEVID[4:0]	Bits [7:3] – ADDR_0x08 (SR4)	Device ID
REVID[2:0]	Bits [2:0] – ADDR_0x08 (SR4)	Revision ID
PAR	Bit 8 – ADDR_0x09 (SR5)	Parity bit for SR5
BemfRes	Bit 7 – ADDR_0x09 (SR5)	BEMF result ready at <Bemf> register
BemfCoil	Bit 6 – ADDR_0x09 (SR5)	Last BEMF measurement was done on coil: 0 = X, 1 = Y
Bemfs	Bit 5 – ADDR_0x09 (SR5)	BEMF measured voltage has expected polarity (Yes = 0, No = 1)
Bemf[4:0]	Bits [4:0] – ADDR_0x09 (SR5)	BEMF value measured during zero crossing
Sp[7:0]	Bits [7:0] – ADDR_0x0A (SR6)	Speed register

DEVID [4:0] for NCV70517 device is $(17)_{dec.}$

REVID [2:0] for N70517−2 device is $(3)_{dec.}$

The wiring diagrams below show possible connection of multiple slaves to one microcontroller. In these examples, all movements of the motors are synchronized by means of a common NXT wire. The direction and Run/Hold activation is controlled by means of an SPI bus.

Further I/O reduction is accomplished in case the ERRB is not connected. This would mean that the microcontroller operates while polling the error flags of the slaves. Ultimately, one can operate multiple slaves by means of only



QFNW32 5x5, 0.5P
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SCALE 2:1