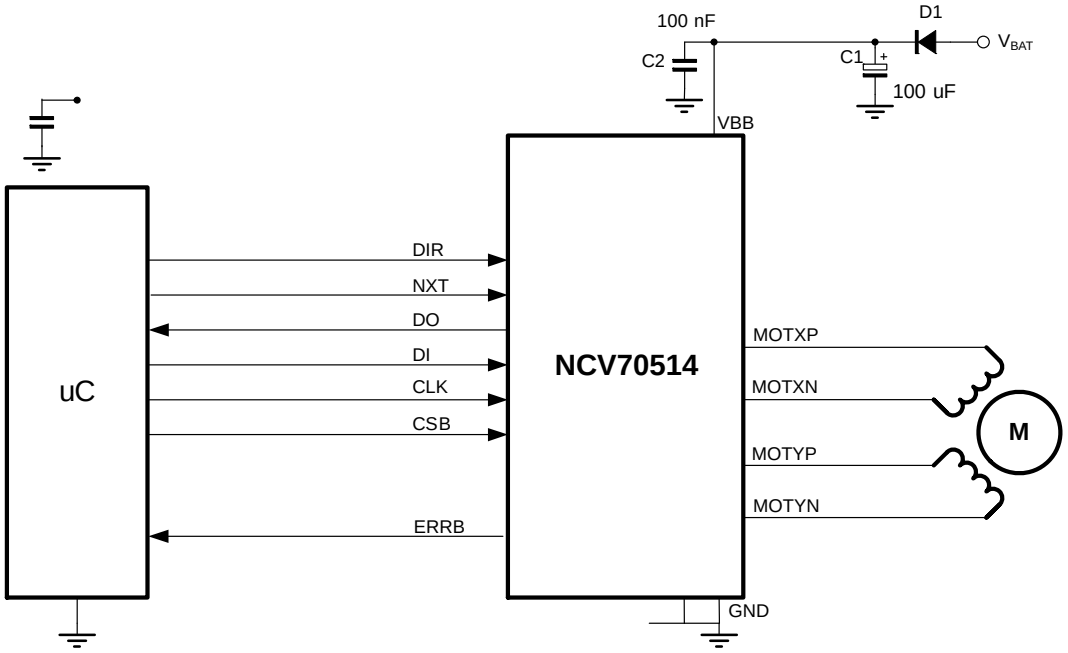
TYPICAL APPLICATION SCHEMATIC

The application schematic below shows typical connections for applications with low axis counts and/or with software SPI implementation. For applications with many stepper motor drivers, some “minimal wiring” examples are shown at the last sections of this datasheet.



PACKAGE AND PIN DESCRIPTION

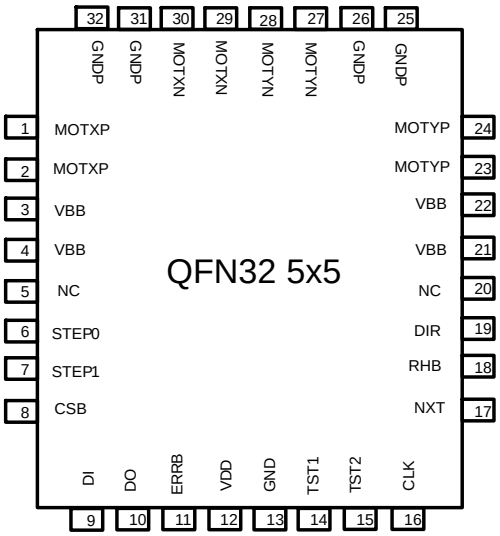


Figure 3. Pin Connections – QFN32 5x5

Table 2. PIN DESCRIPTION

Pin No. QFN32 5x5	Pin Name	Description	I/O Type
1, 2	MOTXP	Positive end of phase X coil	Driver output
3, 4, 21, 22	VBB	Battery voltage supply	Supply
5, 20	NC	Not Connected	
6	STEP0	Step mode selection input 0	Digital Input
7	STEP1	Step mode selection input 1	Digital Input
8	CSB	SPI chip select input	Digital Input
9	DI	SPI data input	Digital Input
10	DO	SPI data output (Open Drain)	Digital Output
11	ERRB	Error Output (Open Drain)	Digital Output
12	VDD	Internal supply (needs external decoupling capacitor)	Supply
13	GND	Ground	Supply
14	TST1		

NCV70514

ELECTRICAL CHARACTERISTICS

DC PARAMETERS

The DC parameters are guaranteed over junction temperature from −40 to 145°C and VBB in the operating range from 6 to 29 V, unless otherwise specified. Convention: currents flowing into the circuit are defined as positive.

Table 6. DC PARAMETERS

Symbol	Pin(s)	Parameter	Test Conditions	Min	Typ	Max	Unit
MOTORDRIVER							
$I_{MS-max,Peak}$	MOTXP MOTXN MOTYP MOTYN	Max current through motor coil in normal operation	V_{BB} = 14 V		800		mA
I_{MSabs}		Absolute error on coil current (Note 16)	V_{BB} = 14 V, T_j = 145°C	−10		10	%
I_{MSrel}		Matching of X & Y coil currents (Note 16)	V_{BB} = 14 V	−7		7	%
$R_{DS(on)}$		On resistance of High side + Low side Driver at the highest current range	$T_j \le 25°C$			1.8	Ω
			T_j = 145°C			2.4	Ω
R_{mpd}		Motor pin pull−down resistance	HiZ mode		70		kΩ
LOGIC INPUTS							
V_{inL}	DI, CLK, NXT, DIR, RHB, STEP0, STEP1	Logic low input level, max	T_j = 145°C			0.8	V
V_{inH}		Logic high input level, min	T_j = 145°C	2.4			V
I_{inL}		Logic low input level, max	T_j = 145°C	−1			μA
I_{inH}		Logic high input level, max	T_j = 145°C	1	2	4	μA
V_{inL}	CSB	Logic low input level, max	T_j = 145°C			0.8	V
V_{inH}		Logic high input level, min	T_j = 145°C	2.4			V
I_{inL}		Logic low input level, max (Note 17)	T_j = 145°C	−50	−30	−10	μA
I_{inH}		Logic high input level, max (Note 17)	T_j = 145°C			1	μA
R_{pd}	TST1	Internal pull−down resistor		3		9	kΩ
LOGIC OUTPUTS							
V_{OLmax}	DO, ERRB	Output voltage when	8 mA sink current			0.4	V
V_{OHmax}		Maximum drain voltage				5.5	V
I_{OLmax}		Maximum allowed drain current (Note 25)				12	mA
THERMAL WARNING & SHUTDOWN							
T_{tw}		Thermal warning (Notes 18 and 19)		136	145	154	°C
T_{tsd}		Thermal shutdown (Note 20)		156	165	174	°C

16. Tested in production for 800 mA, 400 mA, 200 mA and 100 mA current settings for both X and Y coil.
17. CSB has an internal weak pull−up resistor of 100 kΩ.
18. Thermal warning is derived from thermal shutdown ($T_{tw} = T_{tsd}$

Table 6. DC PARAMETERS

Symbol	Pin(s)	Parameter	Test Conditions	Min	Typ	Max	Unit
SUPPLY AND VOLTAGE REGULATOR							
UV_3	V_{BB}	H−Bridge off voltage low threshold			5.98		V
UV_1 UV_2		Under voltage low threshold	UVxThr[3:0] = 0000		5.98		V
			UVxThr[3:0] = 1111		10.96		V
UV_{1_STEP} UV_{2_STEP}		Under voltage low threshold step	Between two UVxThr codes		0.33		V
UV_{X_ACC}		Under voltage low threshold accuracy		−4		4	%
UV_{X_HYST}		Under voltage hysteresis		30			

AC PARAMETERS

The AC parameters are guaranteed over junction temperature from −40 to 145°C and VBB in the operating range from 6 to 29 V, unless otherwise specified.

Table 7. AC PARAMETERS

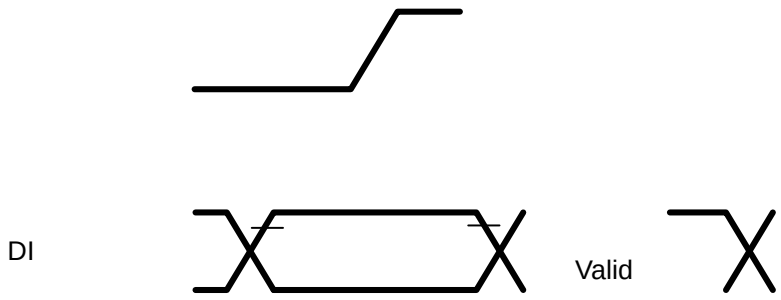
Symbol	Pin(s)	Parameter	Test Conditions	Min	Typ	Max	Unit
INTERNAL OSCILLATOR							
f_{osc}		Frequency of internal oscillator	V_{BB} = 14 V	7.2	8	8.8	MHz
MOTORDRIVER							
f_{pwm}	MOTxx	PWM frequency	(Note 26)	20.5	22.8	25.1	kHz
t_{OCdet}		Open coil detection with PWM=100% (Note 26)	SPI bit OpenDet[1:0] = 00		5		ms
			SPI bit OpenDet [1:0] = 01		25		
			SPI bit OpenDet [1:0] = 10		50		
			SPI bit OpenDet [1:0] = 11		200		
t_{brise}		Turn−on transient time, between 10% and 90%, I_{MD} = 200 mA, V_{BB} = 14 V, 1 nF at motor pins	SPI bit EMC[1:0] = 00		80		ns
			SPI bit EMC[1:0] = 01		120		
			SPI bit EMC[1:0] = 10		190		
t_{bfall}		Turn−off transient time, between 10% and 90%, I_{MD} = 200 mA, V_{BB} = 14 V, 1 nF at motor pins	SPI bit EMC[1:0] = 00		70		ns
			SPI bit EMC[1:0] = 01		110		
			SPI bit EMC[1:0] = 10		180		
DIGITAL OUTPUTS							
t_{H2L}	DO, ERRB	Output fall−time (90% to 10%) from V_{InH} to V_{InL}	Capacitive load 200 pF and pull−up 1.5 kΩ			50	

t

Table 8. SPI INTERFACE

Symbol	Parameter	Min	Typ	Max	Unit
t_{CLK}	SPI clock period	1			μs
t_{HI_CLK}	SPI clock high time	200			ns
$t_{CLKRISE}$	SPI clock rise time			1	μs
$t_{CLKFALL}$	SPI clock fall time			1	μs
t_{LO_CLK}	SPI clock low time	200			ns
t_{SET_DI}	DI set up time, valid data before rising edge of CLK	50			ns
t_{HOLD_DI}	DI hold time, hold data after rising edge of CLK	50			ns
t_{HI_CSB}	CSB high time	2.5			μs
$t_{SET\_CSB\_LO}$	CSB set up time, CSB low before rising edge of CLK (Note 27)	1			μs
$t_{CLK\_CSB\_HI}$	CSB set up time, CSB high after rising edge of CLK	200			ns
$t_{DEL\_CSB\_DO}$	DO delay time, DO settling time after CSB low (Note 28)			250	ns
$t_{DEL\_CLK\_DO}$	DO delay time, DO settling time after CLK low (Note 28)			100	ns

27. After leaving sleep mode an additional wait time of 250 μs is needed before pulling CSB low.
28. Specified for a capacitive load 10 pF and a pull−up resistor of 1.5 kΩ.

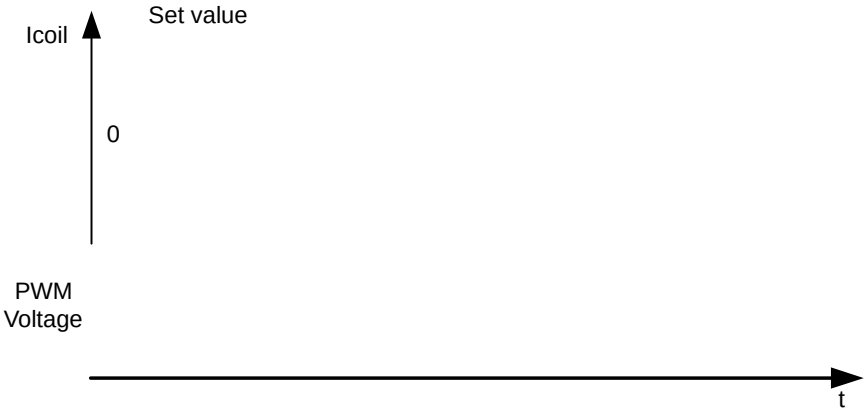


DETAILED OPERATING DESCRIPTION

H−

PWM Duty Cycle Measurement

For both motor windings the actual PWM duty cycle is measured and stored in two status registers. The duty cycle values are a representation of the applied average voltage to the motor windings to achieve and maintain the actual set point current. Figure 8 gives an example of the duty cycle representation.



STEP TRANSLATOR

Step Mode

The step translator provides the control of the motor by means of SPI register step mode: SM[2:0], SPI bits DIRP, RHBP and input pins STEP0, STEP1, DIR (direction of rotation), RHB (run/hold of motor) and NXT (next pulse). It is translating consecutive steps in corresponding currents in both motor coils for a given step mode.

One out of seven possible stepping modes can be selected through SPI−bits SM[2:0] and pins STEP0, STEP1. Device takes the value from SPI−bits SM[2:0] and increases StepMode value with adding binary information from STEP0, STEP1 pins. After power−on or hard reset, the coil−current translator is set to the default to 1/32 micro−stepping at position ‘16*’. When remaining in the default step mode, subsequent translator positions are all in the same column and increased or decreased with 1. Table 9 lists the output current versus the translator position.

When the micro−step resolution is reduced, then the corresponding least−significant bits of the translator position are set to “0”. This means that the position in the current table moves to the right and in the case that micro−step position of desired new resolution does not overlap the micro−step position of current resolution, the closest value up or down in required column is set depending on the direction of rotation.

When the micro−step resolution is increased, then the corresponding least−significant bits of the translator position are added as “0”: the micro−step position moves to the left on the same row.

In general any change of <SM[2:0]> SPI bits or STEP0 and STEP1 pins have no effect on current micro−step position without consequent occurrence of NXT pulse or <NXTP> SPI command. (see NXT input timing below). When NXT pulse or <NXTP> SPI command arrives, the motor moves into next micro−step position according to the current <SM[2:0]> SPI bits value and STEP0, STEP1 pins level set.

NCV70514

Table 9. CIRCULAR TRANSLATOR TABLE

	Step mode SM[2:0]					% of Imax			Step mode SM[2:0]					% of Imax	
	000	001	010	011	100				000	001	010	011	100		
MSP[6:0]	1/32	1/16	1/8	1/4	1/2	Coil Y	Coil X	MSP[6:0]	1/32	1/16	1/8	1/4	1/2	Coil Y	Coil X
010 0111	39	–	–	–	–	94.2	−33.7	**110 0111**	103	–	–	–	–	−94.2	33.7
010 1000	40	20	10	5	–	92.4	−38.3	**110 1000**	104	52	26	13	–	−92.4	38.3
010 1001	41	–	–	–	–	90.4	−42.8	**110 1001**	105	–	–	–	–	−90.4	42.8
010 1010	42	21	–	–	–	88.2	−47.1	**110 1010**	106	53	–	–	–	−88.2	47.1
010 1011	43	–	–	–	–	85.8	−51.4	**110 1011**	107	–	–	–	–	−85.8	51.4
010 1100	44	22	11	–	–	83.1	−55.6	**110 1100**	108	54	27	–	–	−83.1	55.6
010 1101	45	–	–	–	–	80.3	−59.6	**110 1101**	109	–	–	–	–	−80.3	59.6
010 1110	46	23	–	–	–	77.3	−63.4	**110 1110**	110	55	–	–	–	−77.3	63.4
010 1111	47	–	–	–	–	74.1	−67.2	**110 1111**	111	–	–	–	–	−74.1	67.2
011 0000	48														

Table 10. SQUARE TRANSLATOR TABLE FOR FULL STEP

MSP[6:0]	Step mode (SM[2:0])		% of Imax	
	101 or 110	111		
	Full Step1	Full Step2	Coil x	Coil y
000 0000	0	–	100	0
001 0000	–	0	71	71
010 0000	1	–	0	100
011 0000	–	1	−71	71
100 0000	2	–	−100	0
101 0000	–	2	−71	−71
110 0000	3	–	0	−100
111 0000	–	3	71	−71

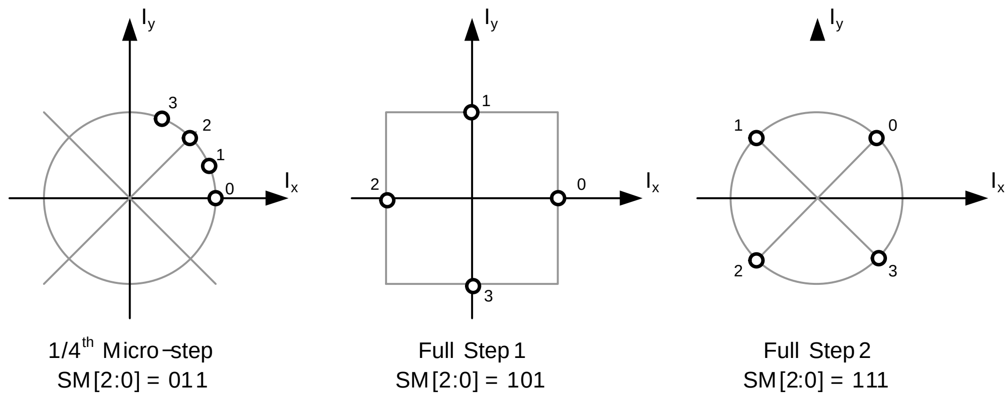


Figure 10. Translator Table: Circular and Square

Translator Position

The translator position can be read in the SPI register <MSP[6:0]>. This is a 7−bit number equivalent to the 1/32th micro−step from : Circular Translator Table. The translator position is updated immediately following a next micro−step trigger (see below).

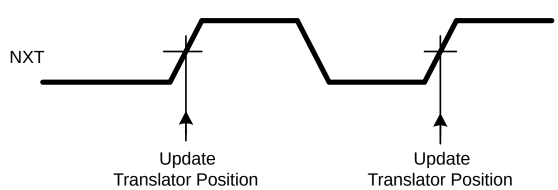


Figure 11. Translator Position Timing Diagram

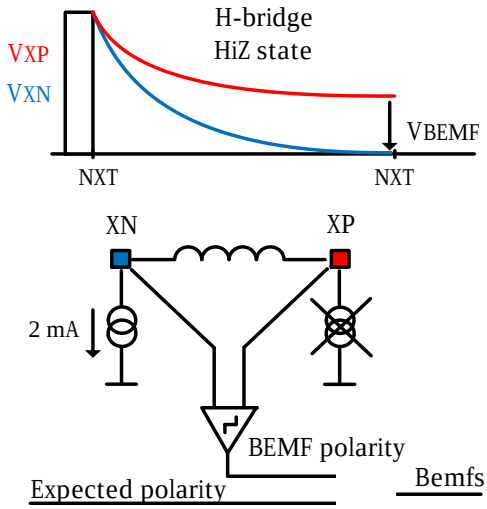
Direction

The direction of rotation is selected by means of input pin DIR and its “polarity bit” <DIRP>52 -1.1962 s1'3A3507...Timing Dia]3A3ptrigger (see below).Directio98.608

Table 11. IRUN AND IHOLD VALUES (4BIT)

E

the polarity of voltage measured over the coil with expected polarity of voltage.



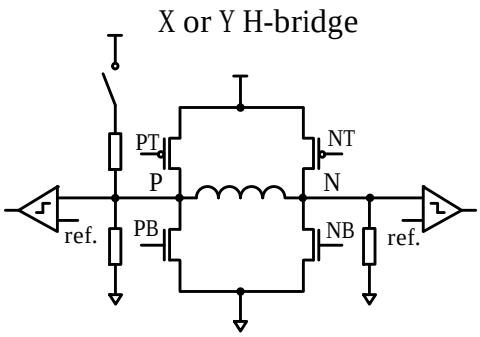


Figure 16. Automatic Diagnostic

Table 14. DIAGNOSTICS OPEN/SHORT DETECTION

Fault condition	SR1[5:4] = {SHORT, OPEN}	SR7A[6] = {OPENX,L}	SR7A[3] = {SHRTXPB}	SR7A[2] = {SHRTXNB}	SR7A[1] = {SHRTXPT}	SR7A[0] = {SHRTXNT}
No short, No open coil – unique detection	0, 0	0	0	0	0	0
Short XP and/or XN top side, no open coil; Short XP and XN top side and open coil	1, 0	0	0	0	1	1
Short XP and/or XN bottom side, no open coil; Short XP and XN bottom side and open coil	1, 1	1	1	1	0	0
No short or short XN bottom side, open coil	1, 1	1	0	1	0	0
Short XP top side, open coil	1, 1	1	0	0	1	0
Short XN top side and short XP bottom side, open coil	1, 1	1	1	0	0	1
Short XN top side, open coil	1, 1	1	0	0	0	1

Open & Short circuit User Diagnostic

When in normal mode, the device will continuously check upon errors with respect to the expected behavior.

The open load condition is determined by the fact that the PWM duty cycle keeps 100% value for a time longer than set by <OpenDet[1:0]> register. This is valid of course only for the X/Y coil where the current is supposed to circulate, meaning that in full step positions (MSP[6:0] = {0; 32; 64; 96} (dec)) the open load can be detected only for one of the coil at a time (respectively {X; Y; X; Y}). The same reasoning applies for the short circuits detection.

Due to the timeout value set by <OpenDet[1:0]>, the open coil detection is dependent on the motor speed. In more detail, there is a maximum speed at which it can be done. Table 15 specifies these maxima for the different step modes. For practical reasons, all values are given in full steps per second.

Table 15. MAXIMUM VELOCITIES FOR OPEN COIL DETECTION

Step Mode	Speed [FS/s] for given <OpenDet[1:0]>			
	00	01	10	11
Full Step1	200	40	20	5
Full Step2	400	80	40	10
1/2	300	60	30	7.5
1/4	350	70	35	8.8
1/8	375	75	37.5	9.4
1/16	387.5	77.5	38.8	9.7
1/32	393.8	78.8	39.4	9.8

When Open coil condition is detected, the appropriate bit (<OPENX> or <OPENY>) together with <OPEN> bit in the SPI status register are set. Reaction of the H−bridge to Open coil condition depends on the settings of <OpenHiZ> and <OpenDis> bits.

When both <OpenHiZ> and <OpenDis> bits are 0, <MOTEN> bit stays in 1 and only H−bridge where open coil is detected is disabled. When <OpenHiZ> bit is set, both H−bridges are disabled (<MOTEN>=0) in case of Open coil detection. When <OpenDis> bit is set, drivers remain active for both coils independently of <OpenHiZ> bit.

The short circuit detection monitors the load current in each activated output stage. The current is measured in terms of voltage drop over the MOSFETS' $R_{DS(ON)}$. If the load

pulled down (*). If junction temperature increases above thermal shutdown level, then also the <TSD> flag is set, the ERRB pin is pulled down, the motor is disabled (<MOTEN> = 0) and the hardware reset is disabled. If $T_j < T_{tw}$ level and <TSD> bit has been read−out, the status of <TSD> is cleared and the ERRB pin is released.

Only if the <TSD>=<TW>=0, the motor can be enabled again by writing <MOTEN>=1 in the control register 1.

During the over temperature condition the hardware reset will not work until $T_j < T_{tw}$ and the <TSD> readout is done.

In this way it is guaranteed that after a <TSD>=1 event, the die−temperature decreases back to the level of <TW>.

Note: (*): During the <TW> situation the motor is not disabled while the ERRB is pulled down. To be informed about other error situations it is recommended to poll the status registers on a regular base (time base driven by application software in the millisecond domain).

SPI Framing Error

The SPI transmission is continuously monitored for correct amounts of incoming data bits. If within one frame of data the number of SPI CLK high transitions is not equal to a multiple of 16 (16,32,48,...), then the SPI error bit in the status register is set and the ERRB pin goes low to indicate this error to the micro controller. During this fault condition the incoming data are not loaded into the internal registers and the transmit shift register is not loaded with the requested data.

pleteanalog anpart16 Tc2.728 1 Tf.553189 TD-0034 Tc.7(motor driv ha gp(0.3is 4189“Hz.23 a1 196 TD-0th63 TTw(after a power)Tj6.2731 Tf2.4446 0 TD0

The status of the SPI framing error is reset by an errorless received frame requesting for the motor controller status register 0. This request will reset the SPI error bit and releases the ERRB pin (high).

Error Output

This is an open drain output to flag a problem to the external microcontroller. The signal on this output is active low and the logic combination of:

NOT(ERRB) = (<SPI> OR <SHORT> OR <OPENX> OR <OPENY> OR <TSD> OR <TW> OR <STALL> OR (BemfIntEn AND BemfRes) OR (UV1IntEn AND UV1) OR (UV2IntEn AND UV2) OR (UV2MIntEn AND UV2M) OR (UV3IntEn AND UV3) OR (UV3MIntEn AND UV3M) OR (*)reset state) AND not (**)sleep mode

Note: (*) reset state: After a power−on or a hard−reset, the ERRB is pulled low during t_{hr_err} (Table 7 − AC PARAMETERS).

Note: (**) sleep mode: In sleep mode the ERRB is always inactive (high).

Sleep Mode

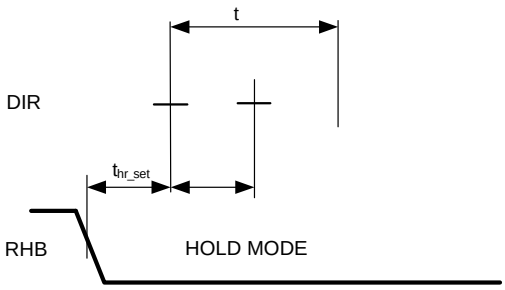
The motor driver can be put in a low−power consumption mode (sleep mode). The sleep mode is entered automatically after a power−on or hard reset and can also be activated by means of SPI bit <SLP>. In sleep−mode, all analog circuits are suspended in low−power and all digital clocks are stopped: SPI communication is impossible. The motor driver is disabled (even if <MOTEN>=1), the content of all logic registers is maintained (including <MOTEN>, <TSD> and <TW>), all logic output pins are disabled (ERRB has no function) and none of the input pins are functional with the exception of pin CSB. Only this pin can wake−up the chip to normal mode (i.e. clear bit <SLP>) by means of a “high−to−low voltage” transition. After wake−up, time t_{wu} (see AC Table) is needed to restore analog and digital clocks and to bring SPI communication within specification.

Notes:

- The hard−reset function is disabled in sleep mode.
- The thermal shutdown function will be “frozen” during sleep mode and re−activated at wake−up. This is important in case bit <TSD>=1 was cleared already by the micro and <TW> was not “0” yet.
- The CSB low pulse width has to be within t_{csb_with}, (see AC Table) to guarantee a correct wake−up.

Power−on Reset, Hard−Reset Function

After a power−on or a hard−reset, a flag <HR> in the SPI status


t
DIR
t_{hr_set}
RHB
HOLD MODE

SPI Control Registers (CR)

All SPI control registers have Read/Write access.

Table 17. SPI CONTROL REGISTERS (CR)

4−bit Address	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default after Reset
01h or 11h (CR1)	DIRP	RHBP	NXTP	MOTEN	StThr3	StThr2	StThr1	StThr0	0000 0000
02h or 12h (CR2)	Ihold3	Ihold2	Ihold1	Ihold0	Irun3	Irun2	Irun1	Irun0	0000 0000
03h or 13h (CR3)	EnhBemf En	DIAGEN	EMC1	EMC0	SLP	SM2	SM1	SM0	0010 0000
04h (CR4)	StTo7	StTo6	StTo5	StTo4	StTo3	StTo2	StTo1	StTo0	0001 0000
05h or 15h (CR5)	SpThr7	SpThr6	SpThr5	SpThr4	SpThr3	SpThr2	SpThr1	SpThr0	0000 0000
06h or 16h (CR6)	UV1Thr3	UV1Thr2	UV1Thr1	UV1Thr0	UV2Thr3	UV2Thr2	UV2Thr1	UV2Thr0	0000 0000
07h or 17h (CR7)	AD4	BemfGain	Bemf ResIntEn	UV1IntEn	UV2IntEn	UV2MIntEn	UV3IntEn	UV3MIntEn	0000 0000
14h (CR4A)	NotUsed	NotUsed	NotUsed	Iboost	OpenDet1	OpenDet0	OpenDis	OpenHiZ	0000 0100

NCV70514 responds on every incoming byte by shifting out the data stored on the last address sent via the bus. After POR the initial address is unknown, so the first data shifted out are undefined.

Table 18. BIT DEFINITION

Symbol	MAP position	Description
DIRP	Bit 7 – ADDR_0x01 or 0x11 (CR1)	Polarity of DIR pin, which controls direction status; DIRP = 1 inverts the logic polarity of the DIR pin)
RHBP	Bit 6 – ADDR_0x01 or 0x11 (CR1)	Polarity of RHB pin, which controls RUN/HOLD status; RHBP = 1 inverts logic polarity of the RHB pin (Hold = NOT(RHB XOR <RHBP>))
NXTP	Bit 5 – ADDR_0x01 or 0x11 (CR1)	Push button pin, generating next step in position table
MOTEN	Bit 4 – ADDR_0x01 or 0x11 (CR1)	Enables the H−bridges (motor activated in RUN or HOLD mode)
StThr[3:0]	Bits [3:0] – ADDR_0x01 or 0x11 (CR1)	Threshold level for stall detection, when “0”, stall detection is disabled
Ihold[3:0]	Bits [7:4] – ADDR_0x02 or 0x12 (CR2)	Current amplitude in HOLD mode
Irun[3:0]	Bits [3:0] – ADDR_0x02 or 0x12 (CR2)	Current amplitude in RUN mode
EnhBemfEn	Bit 7 – ADDR_0x03 or 0x13 (CR3)	Enhanced BEMF measurement functionality is activated when bit is set
DIAGEN	Bit 6 – ADDR_0x03 or 0x13 (CR3)	Enables automatic diagnostic at rising edge of <MOTEN> bit
EMC[1:0]	Bits [5:4] – ADDR_0x03 or 0x13 (CR3)	Voltage slope defining bits for motor driver switching
SLP	Bit 3 – ADDR_0x03 or 0x13 (CR3)	Places device in sleep mode with low current consumption (when 1)
SM[2:0]	Bits [2:0] – ADDR_0x03 or 0x13 (CR3)	Step mode selection
StTo[7:0]	Bits [7:0] – ADDR_0x04 (CR4)	Max difference between two successive full step next pulse periods (time-out), after this time the BEMF sample is taken to verify stall
SpThr[7:0]	Bits [7:0] – ADDR_0x05 or 0x15 (CR5)	Speed threshold register, BEMF measurement and stall detection is activated when Speed register value is less than or equal to <SpThr> value

U:0]

SPI Status Registers (SR)

Table 20. BIT DEFINITION

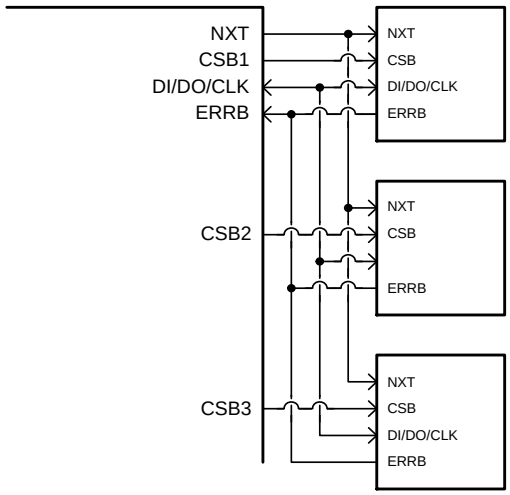
Symbol	MAP Position	Description
MSP[6:0]	Bits [6:0] – ADDR_0x0A or 0x1A (SR3)	Translator micro−step position
PAR	Bit 7 – ADDR_0x0B or 0x1B (SR4)	Parity bit for SR4
BemfCoil	Bit 6 – ADDR_0x0B or 0x1B (SR4)	Last BEMF measurement was done on coil: 0 = X, 1 = Y
Bemfs	Bit 5 – ADDR_0x0B or 0x1B (SR4)	[illegible]
Bemf[4:0]	Bits [4:0] – ADDR_0x0B or 0x1B (SR4)	BEMF value measured during zero crossing

Sp[7:0]Sp[7:0]

APPLICATION EXAMPLES FOR MULTI−AXIS CONTROL

The wiring diagrams below show possible connections of multiple slaves to one microcontroller. In these examples, all movements of the motors are synchronized by means of a common NXT wire. The direction and Run/Hold activation is controlled by means of an SPI bus.

Further I/O reduction is accomplished in case the ERRB is not connected. This would mean that the microcontroller operates while polling the error flags of the slaves. Ultimately, one can operate multiple slaves by means of only 4 SPI connections: even the NXT pin can be avoided if the microcontroller operates the motors by means of the “NXTP” bit.



ELECTRO MAGNETIC COMPATIBILITY

The NCV70514 has been developed using state−of−the−art design techniques for EMC. The overall system performance depends on multiple aspects of the system (IC design & lay−out, PCB design and layout ...) of which some are not solely under control of the IC manufacturer. Therefore, meeting system EMC requirements can only happen in collaboration with all involved parties.

Special care has to be taken into account with long wiring to motors and inductors. A modern methodology to regulate the current in inductors and motor windings is based on controlling the motor voltage by PWM. This low frequency switching of the battery voltage is present at the wiring towards the motor or windings. To reduce possible radiated transmission, it is advised to use twisted pair cable and/or shielded cable.

PCB LAYOUT RECOMMENDATIONS

ORDERING INFORMATION

Device	Marking	Peak Current	Boost Peak Current	End Market/Version	Package*	Shipping†
NCV70514MW003BR2G	N70514−3	800 mA	N.A.	Automotive High Temperature Version	QFNW32 5x5 with step−cut wettable flank (Pb−Free)	5000 / Tape & Reel
NCV70514MW007AR2G**	N70514−7	800 mA	1100 mA		QFNW32 5x5 with step−cut wettable flank (Pb−Free)	5000 / Tape & Reel

DISCONTINUED (Note 29)

NCV70514MW007R2G	N70514−7	800 mA	1100 mA	Automotive High Temperature Version	QFN32 5x5 with wettable flanks (Pb−Free)	5000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

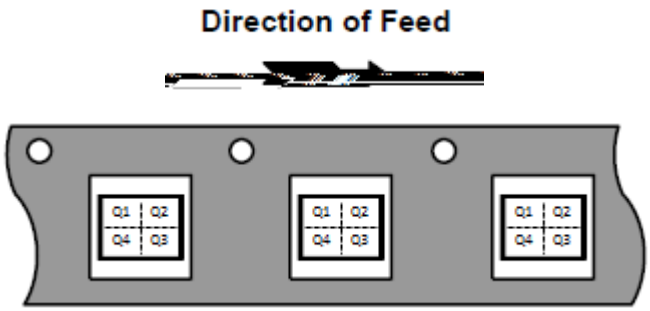
*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

*Devices NCV70514MW003 and NCV70514MW007 have different package mold compound. Please contact **onsemi** for technical details.

**NCV70514MW007A is recommended for new designs.

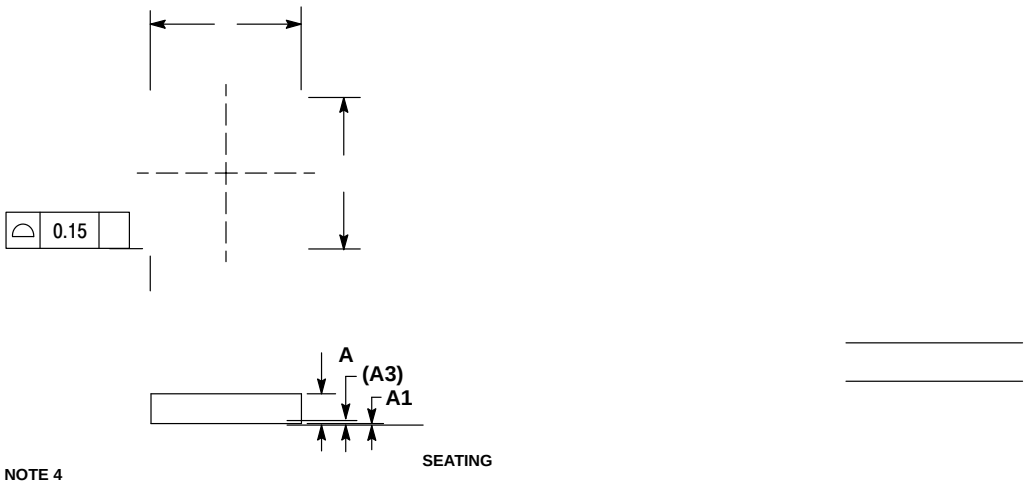
29. **DISCONTINUED:** These devices are not recommended for new design. Please contact your **onsemi** representative for information. The most current information on these devices may be available on www.onsemi.com.

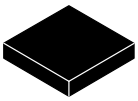
PIN 1 ORIENTATION IN TAPE AND REEL



PACKAGE DIMENSIONS

QFN32 5x5, 0.5P
CASE 488AM
ISSUE A





QFNW32 5x5, 0.5P
CASE 484AB
ISSUE D

DATE 07 SEP 2018

SCALE 2:1