NCT75

Ind S anda d Digi al Tem e a e Sen i h 2- i e In e face

The NCT75 is a two-wire serially programmable temperature sensor with an over-temperature/interrupt output pin to signal out of limit conditions. This is an open-drain pin and can operate in either comparator or interrupt mode. Temperature measurements are converted into digital form using a high resolution (12 bit), sigma-delta, analog-to-digital converter (ADC). The device operates over the –55°C to +125°C temperature range.

Communication with the NCT75 is accomplished via the SMBus/I^{2}C interface. Three address selection pins, A2, A1 and A0, can be used to connect up to 8 NCT75s to a single bus. Through this interface the NCT75s internal registers may be accessed. These registers allow the user to read the current temperature, change the configuration settings and adjust the temperature limits.

The NCT75 has a wide supply voltage range of 3.0 V to 5.5 V. The average supply current is 575 μA at 3.3 V. It also offers a shutdown mode to conserve power. The typical shutdown current is 3 μA.

The NCT75 is available in three, space saving packages – 8-lead DFN, 8-lead Micro8 and 8-lead SOIC and is also fully pin and register compatible with the LM75 and TCN75.

8

CT75
AYW▪
▪

1

Features

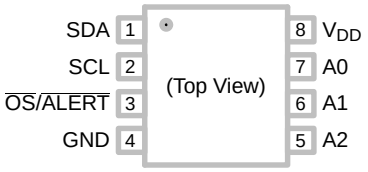
- 12-bit Temperature-to-Digital Converter
- Input Voltage Range from 3.0 V to 5.5 V
- Temperature Range from −55°C to +125°C
- SMBus/I^{2}C Interface
- Overtemperature Indicator
- Support for SMBus/ALER

A = Assembly Location
Y = Year
W = Work Week
▪ = Pb-Free Package

SOIC8
CASE 751

Micro8
CASE 846A

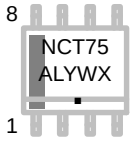
PIN ASSIGNMENT



DFN8

Micro8

(Note: Microdot may be in either location)



SOIC8

A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb-Free Package

Table 2. ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V_{DD}	−0.3 to +7	V
Input Voltage on SCL, SDA, A2, A1, A0 and $\overline{OS}/\overline{ALERT}$.		−0.3 to V_{DD} + 0.3	V
Input Current on SDA, A2, A1, A0 and $\overline{OS}/\overline{ALERT}$.	I_{IN}	−1 to +50	mA
Maximum Junction Temperature	$T_{J(max)}$	150.7	°C
Operating Temperature Range	T_{OP}	−55 to 125	°C
Storage Temperature Range	T_{STG}	−65 to 160	°C
ESD Capability, Human Body Model (Note 1)	ESD_{HBM}	2,000	V
ESD Capability, Machine Model (Note 1)	ESD_{MM}	400	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. This device series incorporates ESD protection and is tested by the following methods:
   ESD Human Body Model tested per AEC−Q100−002 (EIA/JESD22−A114)
   ESD Machine Model tested per AEC−Q100−003 (EIA/JESD22−A115)

Table 3. OPERATING RANGES

Rating	Symbol	Min	Max	Unit
Operating Supply Voltage	V_{IN}	3.0	5.5	V
Operating Ambient Temperature Range	T_A	−55	125	°C

Table 4. SMBus TIMING SPECIFICATIONS

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Serial Clock Frequency	f_{SCL}		DC	−	400	kHz
Start Condition Hold Time	$t_{HD:STA}$		0.6	−	−	μs
Stop Condition Setup Time	$t_{SU:STO}$	90% of SCL to 10% of SDA	100	−	−	ns
Clock Low Period	t_{LOW}		1.3	−	−	μs
Clock High Period	t_{HIGH}		0.6	−	−	μs
Start Condition Setup Time	$t_{SU:STA}$	90% of SCL to 90% of SDA	100	−	−	ns
Data Setup Time	$t_{SU:DAT}$	10% of SDA to 10% of SCL	100	−	−	ns
Data Hold Time (Note 2)	$t_{HD:DAT}$	10% of SCL to 10% of SDA	0	−	76	ns
SDA/SCL Rise Time	t_R		−	300	−	ns
SDA/SCL Fall Time	t_F		−	300	−	ns
Bus Free Time Between STOP and START Conditions	t_{BUF}		1.3			

Table 5. ELECTRICAL CHARACTERISTICS
(T_A = T_{MIN} to T_{MAX}, V_{DD} = 3.0 V to 5.5 V. All specifications for −55°C to +125°C, unless otherwise noted.)

Parameter	Test Conditions	Min

APPLICATION INFORMATION

Functional Description

The NCT75 temperature sensor converts an analog temperature measurement to a digital representation by using an on-chip measurement transistor and a 12 bit

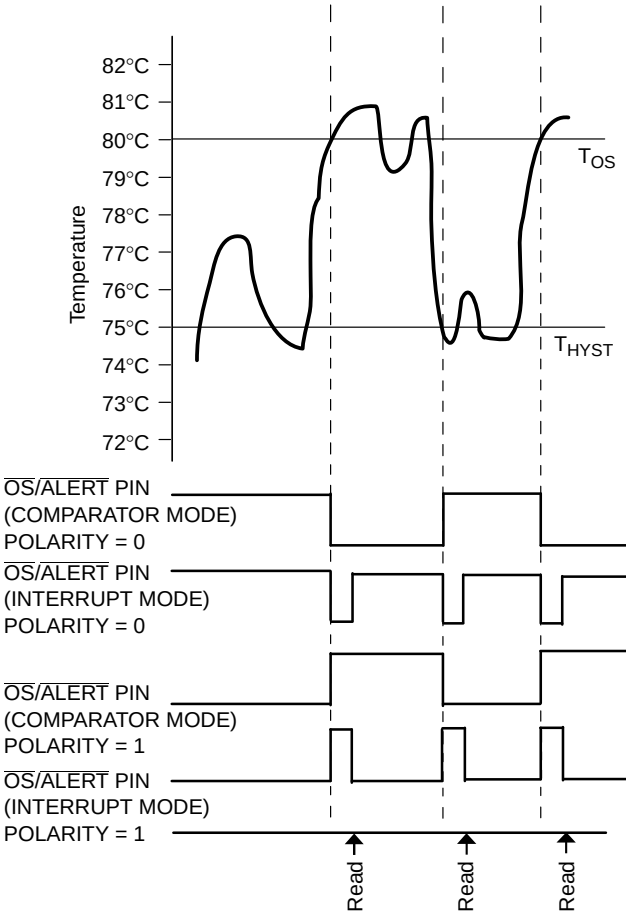


Figure 4. One-shot $\overline{\text{OS}}$/$\overline{\text{ALERT}}$ Pin Operation

Fault Queue

A fault is defined as when the temperature exceeds a pre-defined temperature limit. This limit can be programmed in the T_{HYST} and the T_{OS} setpoint registers. Bits 3 and 4 of the configuration register determine the number of faults necessary to trigger the $\overline{\text{OS}}$/$\overline{\text{ALERT}}$ pin. Up to six faults can be programmed to prevent false tripping when the NCT75 is used in a noisy temperature environment. In order for the $\overline{\text{OS}}$/$\overline{\text{ALERT}}$ output to be set these faults must occur consecutively.

Registers

The NCT75 contains six registers for configuring and reading the teperature: the address pointer register, 4 data registers and a one-shot register. The configuration register, the address pointer register and the one-shot register are all 8 bits wide while the temperature register, T_{HYST} and T_{OS} registers are all 16 bits wide. All registers, except for the temperature register, can be be read from and written to (the temperature register is read only). The power on state and address of each register are listed in Table 9.

Address Pointer Register

The address pointer register is used to select which register is to respond to a read or write operation. The three LSBs (P2, P1 & P0) of this write only register are used to select the appropriate register. On power up this register is loaded with a value of 0x00 and so points to the temperature register. Table 7 shows the bits of the address pointer register and Table 8 shows the pointer address selecting each of the registers available.

Table 7. ADDRESS POINTER REGISTER

	P7	P6	P5	P4	P3	P2	P1	P0
Default	0	0	0	0	0	0	0	0

Table 8. REGISTER ADDRESSES SELECTION

P2	P1	P0	Register Selected
0	0		

Temperature Register

The temperature measured by the parts internal sensor is stored in this 16-bit read only register. The data is stored in twos complement format with the MSB as the sign bit. The 8 MSBs must be read frist followed by the 8 LSBs.

Table 10. TEMPERATURE VALUE REGISTER

MSB															LSB
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	0	0	0	0	0	X	X	X	X

Configuration Register

This 8-bit read/write register is used to configure the NCT75 into its various modes of operation. The different modes are listed in Table 11 and explained in more detail below.

Table 11. CONFIGURATION REGISTER

Bit	Configuration	Default Value
D7	Reserved	0
D6	Reserved	0
D5	One-shot Mode	0
D4	Fault-queue	0
D3	Fault-queue	0
D2	$\overline{OS}$/$\overline{ALERT}$ Pin Polarity	0
D1	Cmp/Int Mode	0
D0	Shutdown Mode	0

D7: Reserved
Write 0 to this bit.

D6: Reserved
Write 0 to this bit.

D5: One-shot Mode
D5 = 0 Part is in normal mode and converting every 60 ms. (Default)
D5 = 1 Setting this bit puts the part into one-shot mode. The part is normally powered down in this mode until the one shot register is written to. Once this register is written to one conversion is performed and the part returns to its shutdown state.

D[4:3]: Fault Queue
D4 D3 These two bits determine how many overtemperature conditions occur before the $\overline{OS}$/$\overline{Alert}$ pin is triggered. This helps to prevent false triggering of the output.
0 0 = 1 Fault (Default)
0 1 = 2 Faults
1 0 = 4 Faults
2 1 = 6 Faults

D2: $\overline{OS}$/$\overline{Alert}$ pin polarity
This selects the polarity of the $\overline{OS}$/$\overline{Alert}$ output pin.
D2 = 0 Output is active low. (Default)
D2 = 1 Output is active high.

D1: Cmp/Int
D1 = 0 Comparator mode. (Default)
D1 = 1 Interrupt mode.

D0: Shutdown
D0 = 0 Normal mode – part is fully powered. (Default)
D0 = 1 Shutdown mode – all circuitry except for the SMBus interface is powered down. Write a 0 to this bit to power up again.

T_{HYST} Register

The T_{HYST} register stores the temperature hysteresis value for the overtemperature output. This value is picked to stop the $\overline{OS}$/$\overline{Alert}$ pin from being asserted and de-asserted in noisy temperature environments. This limit is stored in the 16 bit register in twos complement format. The MSB is the temperature sign bit. The 8 MSBs must be read first followed by the 8 LSBs. The default value is +75°C.

Table 12. T_{HYST} REGISTER

MSB															LSB
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	1	0	1	1	0	0	0	0	X	X	X	X

T_{OS} Register

This register stores the temperature limit at which the part asserts an $\overline{OS}$/$\overline{Alert}$. Once the measured temperature reaches this value an alert or overtemperature output is generated. The data is stored in twos complement format with the MSB as the sign bit. The 8 MSBs must be read frist followed by the 8 LSBs. The default limit +80°C.

Table 13. T_{OS} REGISTER

MSB															LSB
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	0	0	0	0	0	0	0	X	X	X	X

Serial Interface

Control of the NCT75 is carried out via the SMBus/I^{2}C compatible serial interface. The NCT75 is connected to this bus as a slave device, under the control of a master device.

Serial Bus Address

Control of the NCT75 is carried out via the serial bus. The NCT75 is connected to this bus as a slave device under the control of a master device. The NCT75 has a 7-bit serial address. The four MSBs are fixed and set to 1001 while the 3 LSBs can be configured by the user using pins 5, 6 and 7 (A2, A1 and A0). Each of these pins can be configured in one of two ways low or high. This gives eight different address options listed in Table 14 below. The state of these pins is continually sampled and so can be changed after power up.

Table 14. SERIAL BUS ADDRESS OPTIONS

MSBs				LSBs			Address
A6	A5	A4	A3	A2	A1	A0	Hex
1	0	0	1	0	0	0	0x48
1	0	0	1	0	0	1	0x49
1	0	0	1	0	1	0	0x4A
1	0	0	1	0	1	1	0x4B
1	0	0	1	1	0	0	0x4C
1	0	0	1	1	0	1	0x4D
1	0	0	1	1	1	0	0x4E
1	0	0	1	1	1	1	0x4F

The NCT75 also features a SMBus/I^{2}C timeout function whereby the SMBus/I^{2}C interface times out after 22.5 ms of no activity on the SDA line. After this time, the NCT75 resets the SDA line back to its idle state (high impedance) and waits for the next start condition. Note that the timeout function is only active when the SDA line is held low. If the SDA line is held high with no activity for an extended period of time during a transaction, the timeout will not engage and the NCT75 will remain for the remainder of the command.

The serial bus protocol operates as follows:

1. The master initiates data transfer by establishing a start condition, defined as a high to low transition on the serial data line SDA, while the serial clock line SCL remains high. This indicates that an address/data stream is going to follow. All slave peripherals connected to the serial bus respond to the start condition and shift in the next eight bits, consisting of a 7-bit address (MSB first) plus a read/write (R/$\overline{W}$) bit, which determines the direction of the data transfer i.e. whether data is written to, or read from, the slave device. The peripheral with the address corresponding to the transmitted address responds by pulling the data line low during the low period before the ninth clock pulse, known as the acknowledge bit. All other devices on the bus now remain idle while the selected device waits for data to be read from or written to it. If the R/$\overline{W}$ bit is a zero then the master writes to the slave device. If the R/$\overline{W}$ bit is a one then the master reads from the slave device.
2. Data is sent over the serial bus in sequences of nine clock pulses, eight bits of data followed by an acknowledge bit from the receiver of data. Transitions on the data line must occur during the low period of the clock signal and remain stable during the high period, since a low-to-high transition when the clock is high can be interpreted as a stop signal.
3. When all data bytes have been read or written, stop conditions are established. In write mode, the master pulls the data line high during the tenth clock pulse to assert a stop condition. In read mode, the master overrides the acknowledge bit by pulling the data line high during the low period before the ninth clock pulse. This is known as no acknowledge. The master takes the data line low during the low period before the tenth clock pulse, then high during the tenth clock pulse to assert a stop condition.

Any number of bytes of data can be transferred over the serial bus in one operation. However, it is not possible to mix read and write in one operation because the type of operation is determined at the beginning and cannot subsequently be changed without starting a new operation.

Writing Data

There are two types of writes used in the NCT75:

Setting up the Address Pointer Register for a Register Read

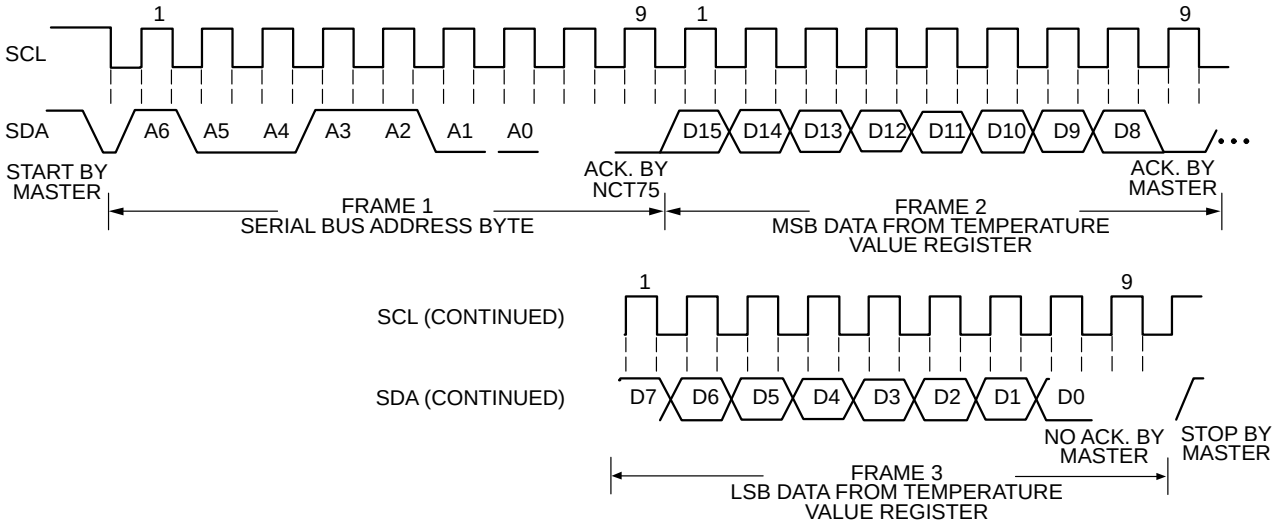
To read data from a particular register, the address pointer register must hold the address of the register being read. To configure the address pointer register a single write operation (shown in Figure 5). It consists of the device address followed by the address being written to the address pointer register. This will then be followed by a read operation.

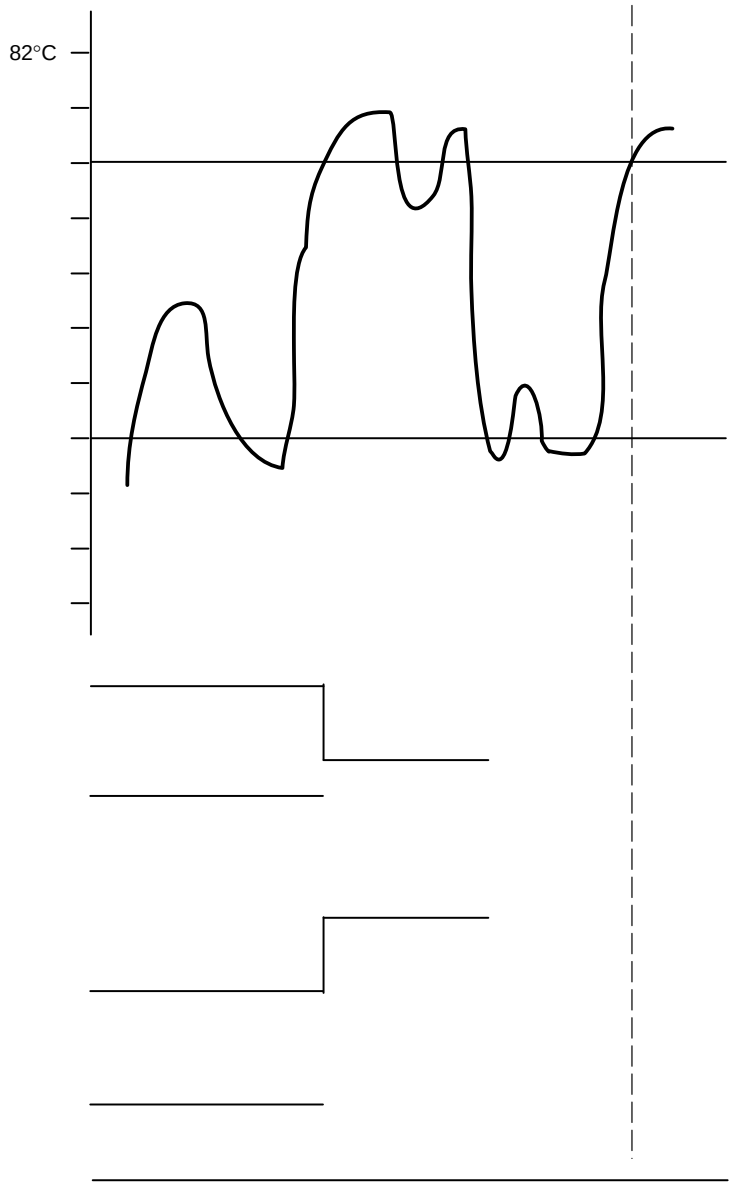
Writing Data to a Register

Due to the different size registers used by the NCT75, there are two types of write operations. One is for the 8 bit wide configuration register and the other for the 16 bit wide limit registers.

Figure 6 shows the sequence required to write to the configuration register. It consists of the device address, the data register being written to and the data being written the selected register.

The two temperature limit registers (T_{HYST} and T_{OS}) are 16 bits wide and require two data bytes to be written to these registers. This sequence is shown in Figure 7. It consists of the device address, the data register being written to and the two data byes being written to the selected register.

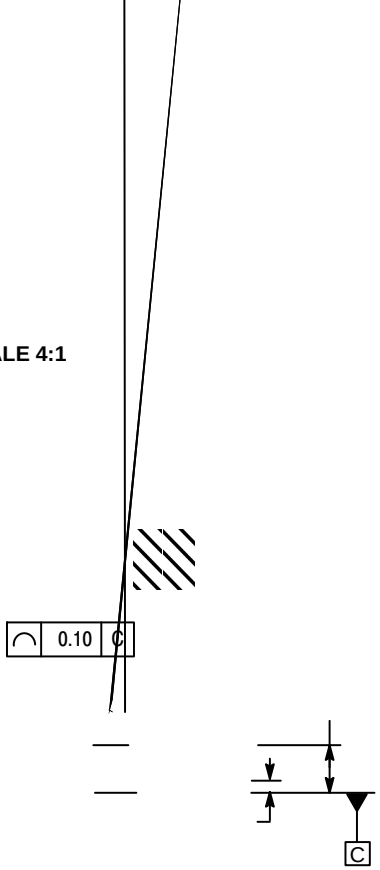

SCL
SDA
1
9
1
9
A6
A5
A4
A3
A2
A1
A0
D15
D14
D13
D12
D11
D10
D9
D8
START BY MASTER
ACK. BY NCT75
ACK. BY MASTER
FRAME 1
SERIAL BUS ADDRESS BYTE
FRAME 2
MSB DATA FROM TEMPERATURE VALUE REGISTER
SCL (CONTINUED)
SDA (CONTINUED)
1
9
D7
D6
D5
D4
D3
D2
D1
D0
NO ACK. BY MASTER
STOP BY MASTER
FRAME 3
LSB DATA FROM TEMPERATURE VALUE REGISTER

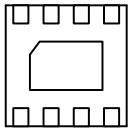

82°C

DFN8 2x2, 0.5P
CASE 506AA−01
ISSUE E

DATE 22 JAN 2010

SCALE 4:1



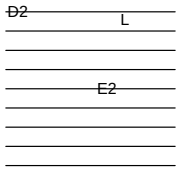


NOTES:
1. DIMENSIONING AND TC618. 0 6 396.E3INCND NOT2 w RRBT/TT2 1 Tf8

A

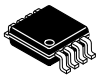
(A3)

SIDE VIEW



BOTTOM VIEW

SOIC−8 NB



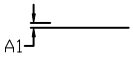
SCALE 2:1

Micro8
CASE 846A−02
ISSUE K

DATE 16 JUL 2020

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.10 mm IN EXCESS OF



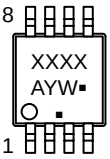
NSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIO

⌓|0.038 (0.0015)|

DIM	MILLIMETER		
	MIN.	NOM.	
A	---	---	
A1	0.05	0.08	
c	0.13	0.18	
E			

RECOMMENDED
MOUNTING FOOTPRINT

GENERIC
MARKING DIAGRAM*



XXXX = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

STYLE 1:
PIN 1. SOURCE
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 2:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. DRAIN 2
7. DRAIN 1
8. DRAIN 1

STYLE 3:
PIN 1. N-SOURCE
2. N-GATE
3. P-SOURCE
4. P-GATE
5. P-DRAIN
6. P-DRAIN
7. N-DRAIN
8. N-DRAIN