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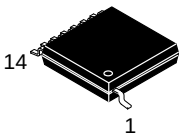
MARKING DIAGRAM



A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

The NCS37020 is an UL943B compliant signal processor for ALCI applications with self−test. The device integrates a 12 V shunt power supply, tiered differential fault detection and self−test per the UL943B standard. Self−test is monitored at start up and every 12 minutes.

Features

- Meets UL943B Self−test ALCI Requirements
- 12 V Shunt Regulator
- Precision Bandgap
- 3.3 V LDO Linear Regulator
- CT Sense Amplifier V_{OS} Dynamic Cancellation
- Oscillator Frequency Trimmed to AC Input
- Tiered GF Trip Times
- Built−In Noise Filter
- LED EOL Indicator
- SCR Gate Driver
- Adjustable Sensitivity
- Minimum External Components
- Low Quiescent Current
- 14 Pin TSSOP Package

Typical Applications

- Personal Care Products
- Non Grounded Neutral Electrical Outlets, Circuit Breakers and Power Cords Requiring Ground Fault Safety Features
- ALCI and RCCB Circuits

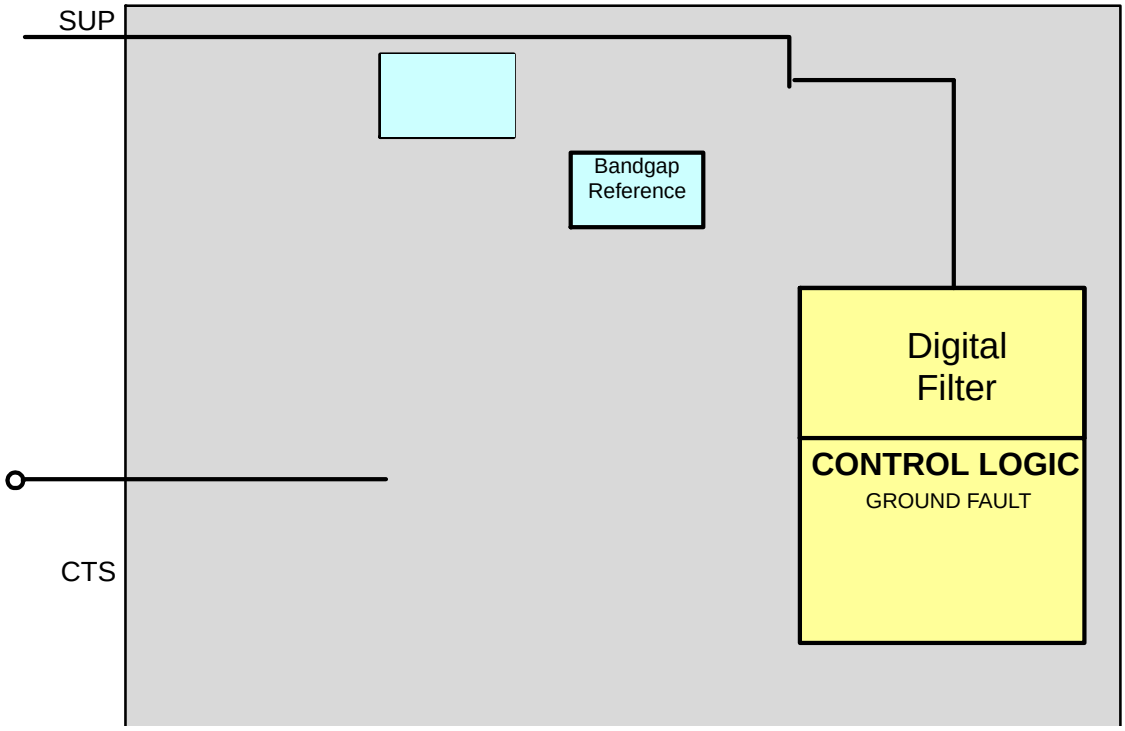


Figure 1. Simplified Block Diagram

Table 2. ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage Range	Vs	13.5	V
Supply Current	Is	10	mA
Input Voltage Range (Note 3)	V_{in}	−0.3 to 3.6	V
Output Voltage Range	V_{out}	−0.3 to 3.6 V or (V_{in} + 0.3), whichever is lower	V
Maximum Junction Temperature	$T_{J(max)}$	140	°C
Storage Temperature Range	T_{STG}	−65 to 150	°C
ESD Capability, Human Body Model (Note 4)	ESD_{HBM}	2	kV
ESD Capability, Charge Device Model (Note 4)	ESD_{CDM}	500	V
Lead Temperature Soldering Reflow (SMD Styles Only), Pb−Free Versions (Note 5)	T_{SLD}	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Functional operation above the Recommended Operating Conditions is not implied. Extended
2. Exposure to stresses above the Recommended Operating Conditions may affect device reliability.

APPLICATIONS INFORMATION

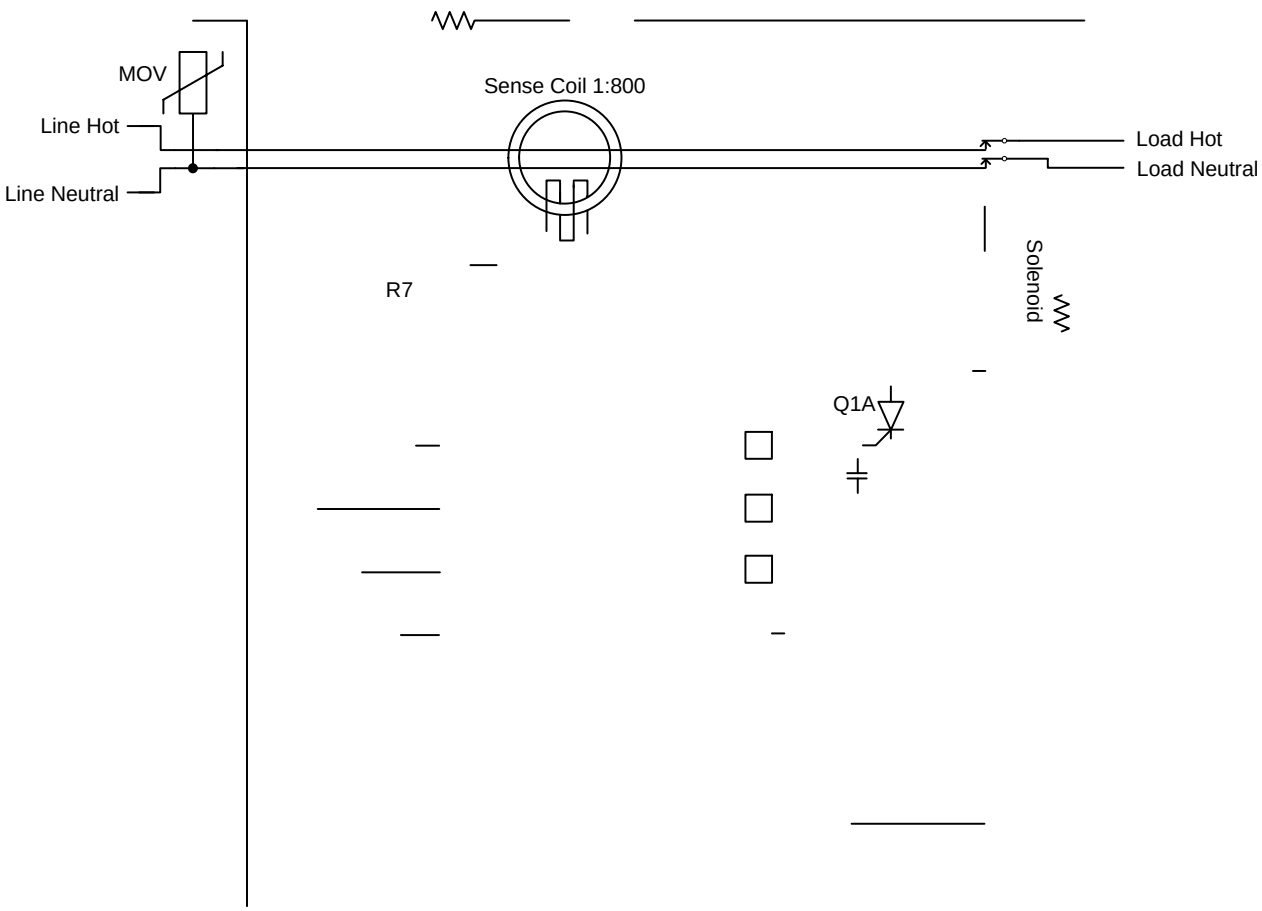


Figure 2. ALCI Application Diagram*

Table 5. RECOMMENDED EXTERNAL COMPONENTS

Component Type	Instance	Value	Note

Functional Description (refer to application circuit, Figure 2)

The NCS37020 provides for a single IC controller solution for ground fault protection and self−test auto monitoring per UL standard UL943B.

The key internal blocks include: 12 V shunt regulator, precision bandgap reference, two 3.3 V linear regulators (one for the digital and one for the analog circuit), CT sense amplifier with V_{OS} dynamic cancellation, 1.65 V reference for the CT, 2 MHz oscillator dynamically trimmed to the AC line frequency, 8 bit SAR ADC, comparators, digital filters and digital control logic.

The internal shunt regulator clamps the SUP pin voltage at 12 volts. This provides the bias voltage for the analog and digital internal circuitry via two 3.3 V linear regulators. The NCS37020 controller can be biased full wave or half wave. Figure 2 shows a half wave bias application. Half wave bias allows for lower wattage bias resistors (R1A and R1B) and less redundant bias diodes. The D1−4 diodes are biased so that only during the positive half cycle the capacitor C1 will be charged to 12 volts. During the negative half cycle, C1 will supply the bias current for the NCS37020. To minimize the NCS37020 bias current during the negative half cycle, the SCR and LED outputs will only be enabled during the positive half cycle. The D1−4 diodes and R1A−R1B resistors include redundant components to pass the UL943B standard.

At POR (power on reset) detection (SUP>4 V) the logic is reset and the bias circuitry is enabled. The Phase pin continually checks for an input signal. There is a 1 μA pull down internal current source connected to this pin so a floating or open pin will be biased low. If there is no 50/60 Hz signal detected on this pin for greater than 32 ms due to an open solenoid or open R2 resistor, a “no clock” End of Life (EOL) fault will occur. After ~150 ms, the LED indicator logic will be enabled and blink at 4 Hz. The SCR will be enabled for one positive half cycle every 4 seconds. The “no clock” EOL logic state will continue until a POR occurs or a 50/60 Hz signal is detected on the Phase pin. When a 50/60 Hz signal is detected, the no clock EOL state will be reset and a ST (self−test) cycle will occur after 75 ms. If this ST cycle passes, the next ST cycle will occur in 12 minutes. If four consecutive no clock ST cycles fail, a ST EOL fault will occur. During a no clock EOL state, the phase information will be detected by the shunt regulator’s bias circuitry. The shunt regulator will detect an AC zero cross by monitoring the Shunt regulator’s clamp current. When the VAC voltage crosses ~80 volts, a zero cross is registered by the shunt regulator’s circuitry.

Note, the “no clock” EOL logic can be used in production testing for generation of an EOL state and enabling the LED indicator. If a DC voltage greater than ~75 volts is applied to the Line Hot input, the NCS37020 will be biased correctly but will not see a zero cross signal and a “no clock” ST EOL failure will occur. The LED will be enabled within 150 ms.

The first self−test (ST) cycle will occur at one second and thereafter every 12 minutes. During the ST cycle, the Fault Test pin will be enabled during the positive half cycle and the

The ground fault detection circuit has different levels of time delay before the SCR is enabled:

6 mA to 15 mA	≤150 ms
15 mA to 30 mA	≤100 ms
30 mA to 100 mA	≤40 ms
>100 mA	≤25 ms

If a very high GF occurs and a greater than 250 mV signal

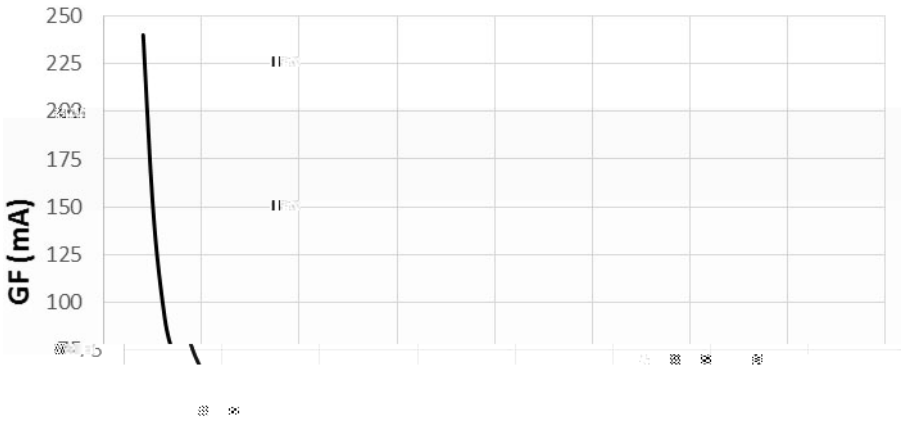
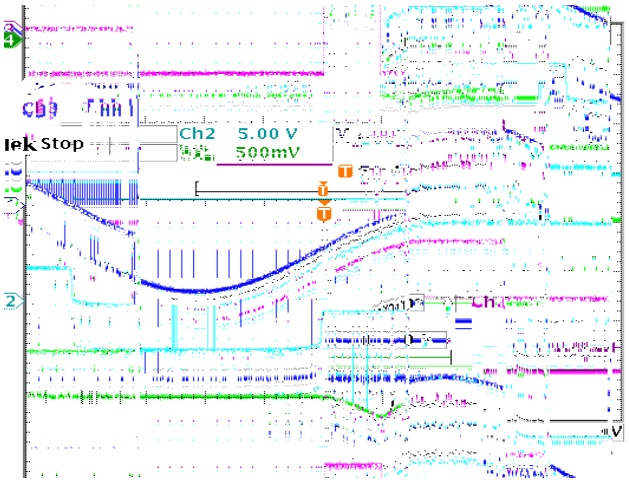
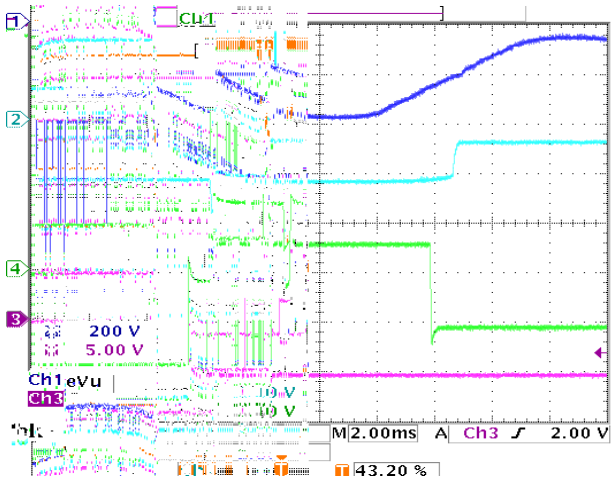


Figure 3. Typical GF Current vs. Trip Time



Passing Self Test
GF Test
Ch1: VAC 120V_{RMS}
Ch2: Phase (Pin 8)
Ch3: Fault Test (Pin 13)
Ch4: IDF (Pin 5)

Figure 4. Passing Self Test − GF

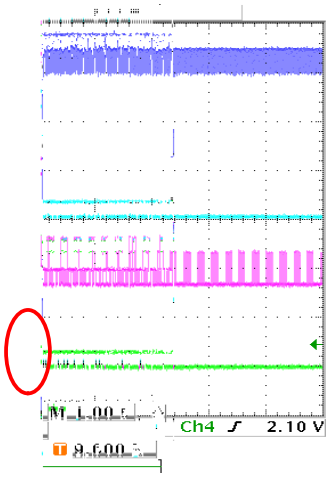


Passing Self Test
SCR Test
Ch1: VAC 120V_{RMS}
Ch2: Phase (Pin 8)
Ch3: SCR (Pin 14)
Ch4: SCR Test (Pin 1)

Figure 5. Passing Self Test − SCR

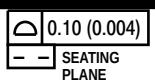
Failing Self Test
No Clock
Ch1: Supply (Pin 9)
Ch2: Phase (Pin 8)
Ch3: LED (Pin 11) @ 114 ms

Figure 9. Failing Self Test − No Clock



Failing Self Test
No Clock
Ch1: Supply (Pin 9)
Ch2: Phase (Pin 8)
Ch3: LED (Pin 11)
Ch4: SCR (Pin 14) @ 3.8 seconds

Figure 10. Failing Self Test − No Clock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SEATING
PLANE