

Self Test Ground Fault Circuit Interrupter (GFCI)

NCS37015

The NCS37015 is a UL943 compliant signal processor for GFCI applications with self test. The device integrates a flexible power supply (including a 12 V shunt and two 3.3 V internal series regulators), differential fault, and grounded—neutral detection circuits. Self test is monitored at start up and then every 17 minutes.

Features

• Meets UL943 Self-test GFCI Requirements

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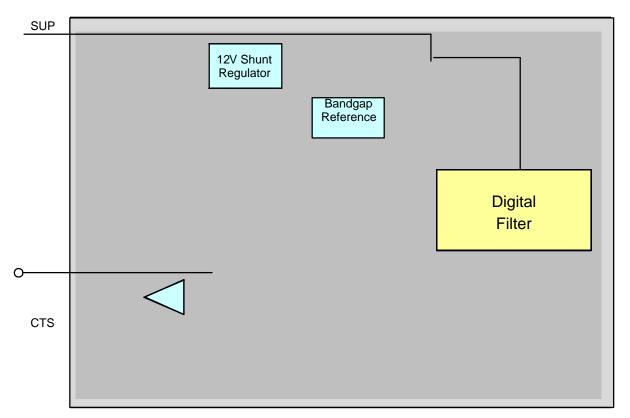


Figure 1. Simplified Block Diagram

Table 2. ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage Range	Vs	13.5	V
Supply Current	Is	10	mA
Input Voltage Range (Note 3)	V _{in}	-0.3 to 3.6	V
Output Voltage Range	V _{out}	-0.3 to 3.6 V or (V _{in} + 0.3), whichever is lower	V
Maximum Junction Temperature	T _{J(max)}	140	°C
Storage Temperature Range	TSTG	-65 to 150	°C
ESD Capability, Human Body Model (Note 4)	ESD _{HBM}	2	kV
ESD Capability, Charge Device Model (Note 4)	ESD _{CDM}	500	V
Lead Temperature Soldering Reflow (SMD Styles Only), Pb–Free Versions (Note 5)	T _{SLD}	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

- 1. Functional operation above the Recommended Operating Conditions is not implied. Extended
- Exposure to stresses above the Recommended Operating Conditions may affect device reliability.
 Refer to ELECTRICAL CHARACTERISTICS and APPLICATION INFORMATION for Safe Operating Area.
- 4. This device series incorporates ESD protection and is tested by the following methods:

 - ESD Human Body Model tested per JS-001-2012 ESD Charge Device Model tested per JESD22-C101-F
 - Latchup Current Maximum Rating: ≤ 100 mA per JEDEC standard: JESD78D
- 5. For information, please refer to our Soldering and Mounting Techniques Reference Manual, SOLDERRM/D

Table 3. THERMAL CHARACTERISTICS

Rating	Symbol	Value	Unit
Thermal Characteristics, QFN16, 3x3.3 mm (Note 6) Thermal Resistance, Junction–to–Air (Note 7)	$R_{\theta JA}$	64	°C/W

- 6. Refer to ELECTRICAL CHARACTERISTICS and APPLICATION INFORMATION for Safe Operating Area.
- 7. Values based on copper area of 645 mm² (or 1 in²) of 1 oz copper thickness and FR4 PCB substrate.

Table 4. OPERATING RANGES (Unless otherwise noted, $I_{SUP} = 3$ mA, MLD input = 60 Hz, Refer to Figure 2)

Parameter	Conditions	Min	Тур	Max	Units
Operating Temperature	Ambient	-40		95	С
Shunt Regulator Voltage	SUP to GND, I _{SUP} = 1 mA		12	13	V
Shunt Regulator Current	I _{SUP}			10	mA
Quiescent Current	I _{SUP} , SUP = 10.5 V				

APPLICATIONS INFORMATION

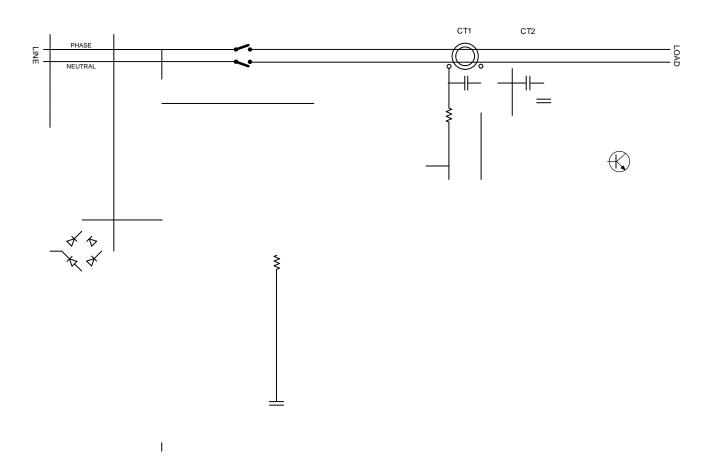


Figure 2. Portable GFCI Application Diagram (example)

Table 5. RECOMMENDED EXTERNAL COMPONENTS

Component Type	Instance	Value	Note
NPN	Q1A, Q1B, Q2	_	MMBT6517LT1-D
Diode Bridge	DB	-	
Diode	D2, D4	-	1N4007
LED	D3	-	LED for self test failure
Capacitor	C1	33 nF	Differential current filter capacitor
Capacitor	C2	56 nF	Anti–aliasing filter (1 kHz corner frequency)
Capacitor	C3	10 μF	Solenoid firming capacitor
Capacitor	•	•	•

Functional Description (refer to application circuit)

The NCS37015 provides for a single IC controller solution for ground fault, grounded neutral and self-test protection per UL standard UL943 for GFCI applications.

The key internal blocks include: 12 V shunt regulator, precision bandgap reference, two 3.3 V linear regulators (one for the digital and one for the analog circuit) sense amplifier with V_{OS} cancellation, 1.65 V reference for the CT, 2 MHz oscillator dynamically trimmed to the AC line frequency, 8 bit SAR ADC, comparators, digital filters and digital control logic.

To work more easily with portable GFCI applications the SCR pin will assert high on power—up. If a fault is detected or self—test fails the SCR pin will drive low and remain in this state until the part goes through a power on reset.

The internal shunt regulator clamps the SUP pin voltage at 12 volts. This provides the bias voltage for the analog (vda) and digital (vdd) internal circuitry via two 3.3 V linear regulators.

At POR detection (vda>2.475) the logic is reset and the bias circuitry is enabled, the LED pin will blink once for 250 ms. The MLD pin is continually checked for an input signal greater than 25 Hz. If the MLD signal is greater than 25 Hz, this test passes. If it fails, the LED blinking logic will be enabled. A six minute timer will start and if no MLD signal is detected, the SCR will be enabled. If a MLD signal occurs before the six minute timer and is longer than one minute, the timer will be reset.

The first self test (ST) cycle will occur at two seconds and thereafter every 17 minutes. During the ST cycle the GFT pin will be enabled and the CT current (set at 8 mA, R2) will be verified for two half cycles. If a ST cycle fails due to a low GF detection or a GF signal greater than 30 mA, the LED blinking logic will enable and the SCR pin will assert low.

The CT is biased at 1.65 volts. The sense amplifier monitors the ground fault current. This current is converted to a voltage level at the CTO pin which is the input to the ADC (IDF pin). The resistor R8 sets the GF threshold per the following equation:

$$I_{diff} = 0.203 \times CT_1 \times (R_{CT1} + R_1)$$

The TE pin is used for internal production testing only. A 50 k Ω pull down resistor is connected to this pin. This pin						



QFN16 3x3, 0.5P CASE 485FQ ISSUE B

DATE 12 JUL 2022

RECOMMENDED MOUNTING FOOTPRI

GENERIC
MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot

Y = Year
W = Work Week
Pb-Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb–Free indicator, "G" or microdot "=", may or may not be present. Some products may not follow the Generic Marking.

