QFN PIN DESCRIPTION

Pin #	Name	Pad Description
0	Ground	QFN center slug
1	MLD	Mains Level Detect (Zero Cross)
2	CtresGN	Determines IV converter gain for detection threshold / matched to CT turns ratio (Ground−Neutral)
3	Ctbias	Direct connection to the CT
4	Ctstim	Direct connection to the CT
5	CTresD	Determines IV converter gain for detection threshold / matched to CT turns ratio (Differential Current)
6	IDF	Front end noise filter capacitor
7	GFtst	Output to induce external differential current.
8	GnEN	Ground−Neutral fault detection enable pin.
9	SCRtstEN	SCR/solenoid self test enable pin.
10	TE	Tie to Ground or leave floating.
11	PTT	Push to test input.
12	LObar	Load monitor input.
13	LED[0]	LED[0] output driver.
14	LO	Lockout SCR output driver.
15	SCRdrv	Used to trigger the solenoid at a fault detection
16	Supply	Power supply

TSSOP PIN DESCRIPTION

Pin #	Name	Pad Description
1	CTstim	Differential and ground to neutral stimulus point for the current transformer.
2	Ground	Ground connection efefr 379.720 0 8 120.7559 373.8331 TmBT8 0 0 8 75 9 PIN DESCTc(Pad Description)TjET173.31 399

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage Range	Vs	6.0 to 12	V
Input Voltage Range (Note 1)	V_{in}	−0.3 to 6.0	V
Output Voltage Range	V_{out}	−0.3 to 6.0 V or (V_{in} + 0.3), whichever is lower	V
Maximum Junction Temperature	$T_{J(max)}$	140	°C
Storage Temperature Range	T_{STG}	−65 to 150	°C
ESD Capability, Human Body Model (Note 2)	ESD_{HBM}	2	kV
ESD Capability, Machine Model (Note 2)	ESD_{MM}	200	V
Lead Temperature Soldering Reflow (SMD Styles Only), Pb−Free Versions (Note 3)	T_{SLD}	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Refer to ELECTRICAL CHARACTERISTICS and APPLICATION INFORMATION for Safe Operating Area.
2. This device series incorporates ESD protection and is tested by the following methods:
   ESD Human Body Model tested per AEC−Q100−002 (EIA/JESD22−A114)
   ESD Machine Model tested per AEC−Q100−003 (EIA/JESD22−A115)
   Latchup Current Maximum Rating: ≤150 mA per JEDEC standard: JESD78
3. For information, please refer to our Soldering and Mounting Techniques Reference Manual, SOLDERRM/D

THERMAL CHARACTERISTICS

Rating	Symbol	Value	Unit
Thermal Characteristics, QFN16, 3x3.3 mm (Note 4) Thermal Resistance, Junction−to−Air (Note 5)	$R_{\theta JA}$	64	°C/W
Thermal Characteristics, TSSOP−20 (Note 4) Thermal Resistance, Junction−to−Air (Note 5)	$R_{\theta JA}$	See note above.	°C/W

4. Refer to ELECTRICAL CHARACTERISTICS and APPLICATION INFORMATION for Safe Operating Area.
5. Values based on copper area of 645 mm^2 (or 1 in^2) of 1 oz copper thickness and FR4 PCB substrate.

OPERATING RANGES (Note 6)

Parameter	Conditions	Min	Typ	Max	Unit
Operating Temperature		−40		85	C
IDD in typical power state			2		mA
Stimulus Generator Frequency	Tri−tone	3.1		3.4	kHz
SCR Trigger Current				8	mA
SCR Trigger output voltage	With 5 V supply	4.5		5.5	V
Fault Current Sensitivity	Programmable with CTresD	4.6	4.8	5	mA
Ground Fault Response Time	[redacted]		150		ms
Ground Fault Response Time	20 − 40 mA				

APPLICATIONS INFORMATION

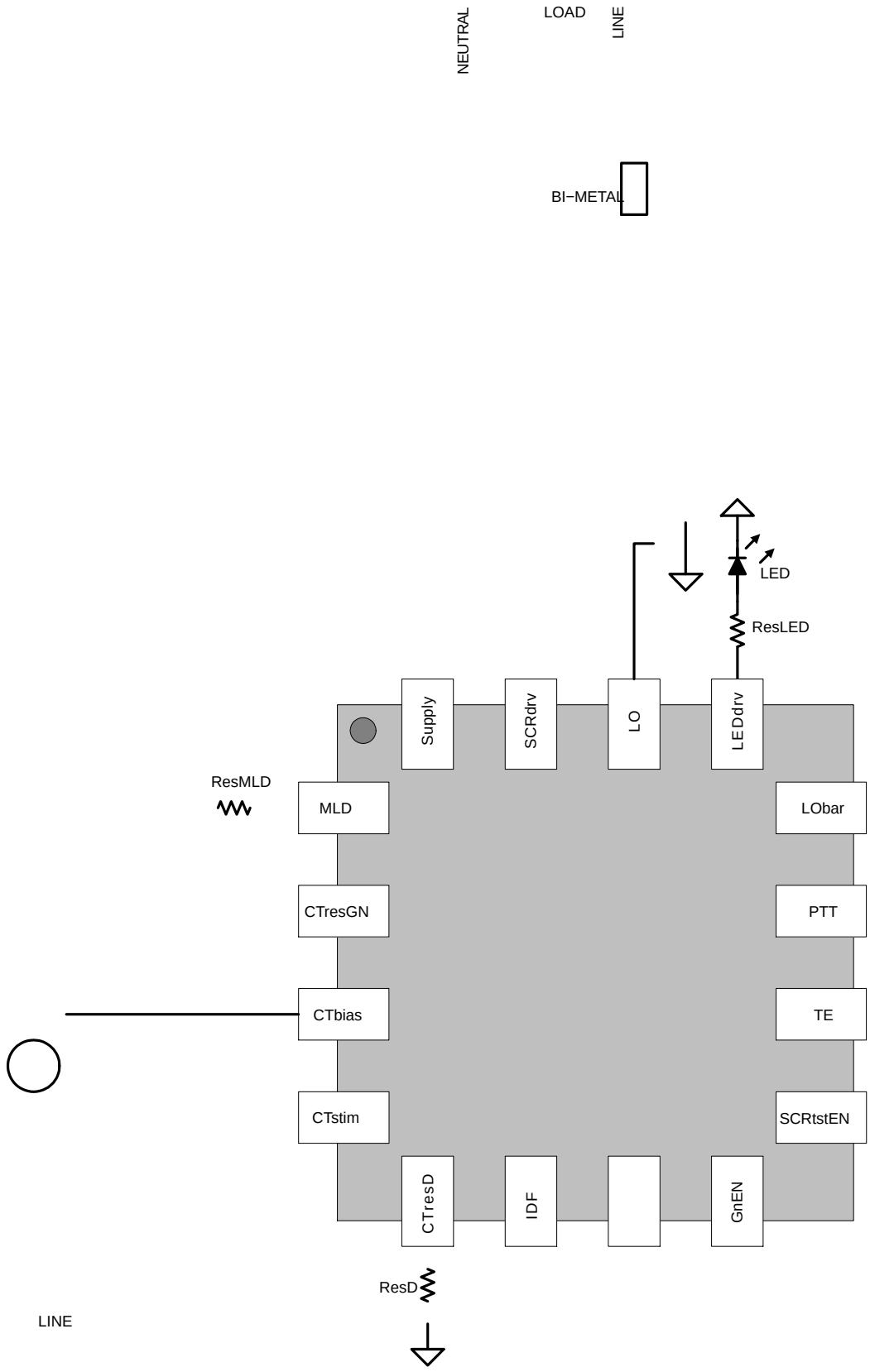
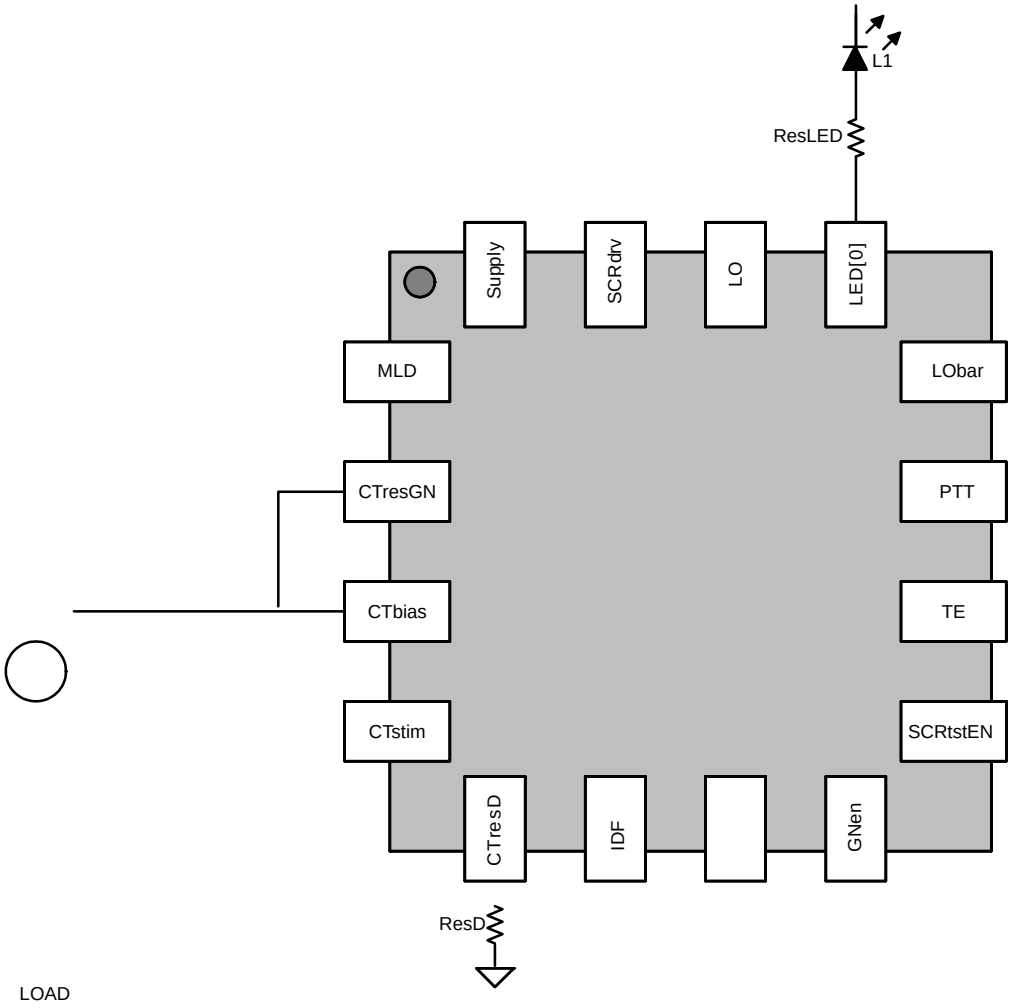


Figure 2. Self Test GFCI Breaker with Lockout


L1
ResLED
Supply
SCRdrv
LO
LED[0]
MLD
LObar
CTresGN
PTT
CTbias
TE
CTstim
SCRtstEN
CTresD
IDF
GNen
ResD
LOAD

RECOMMENDED EXTERNAL COMPONENTS:

Component Type	Instance	Value	Note
SCR	Q2−Q3	−	ON−MCR08
Diode	Dx	−	ON−1N4007
NPN	Q1	−	ON−

Filtering

The analog signal capture portion of the IC includes a single pole filter that can be set externally with Cidf. This provides an additional layer of protection against false tripping under steady state noise conditions. High frequency steady state noise is common with pumps, motors or other cyclic noise generators.

$$Cidf = 220\ nF = 1\ kHz\ low\ pass.$$

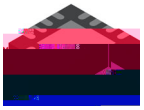
For additional filtering suggestions please contact ON Semiconductor.

Setting Trip Sensitivity

The CTresD resistor sets the threshold for the differential current fault levels. Increasing CTresD causes the fault levels to trip at lower differential currents. CT efficiency at 60 Hz must be considered.

$$CTresD = 200 * \#Turns - Subject\ CT\ efficiency\ at\ 60\ Hz$$

The CTresGN resistor sets the threshold for ground to neutral fault detection. The Rt parameter is the desired ground to neutral resistance trip level. Higher CTresGN values will cause the part to trip at higher ground to neutral



QFN16 3x3, 0.5P
CASE 485FQ
ISSUE B

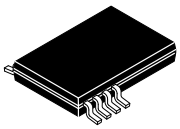
DATE 12 JUL 2022

RECOMMENDED
MOUNTING FOOTPRI

GENERIC MARKING DIAGRAM*

XXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package
(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.



SCALE 2:1

TSSOP−20 WB
CASE 948E
ISSUE D

DATE 17 FEB 2016