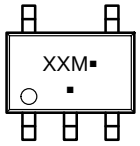
C). The rail-to-rail input and output operation allows the use of the entire supply voltage range. Thus, this series of op amps offers superior performance over many industry standard parts. These devices are AEC-Q100 qualified when denoted by the NCV prefix.

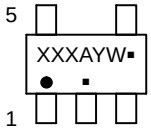
With low current consumption and low supply voltage operation in industry standard packages, the NCS20161 series is ideal for sensor signal conditioning and low voltage current sensing applications in automotive, consumer and industrial markets.

MARKING DIAGRAMS

Single Channel Configuration
NCS20161, NCV20161

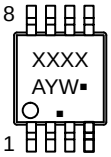


SC70 ï5
CASE 419A

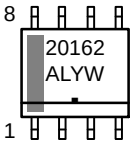


TSOP ï5/SOT23 ï5
CASE 483

Dual Channel Configuration
NCS20162, NCV20162

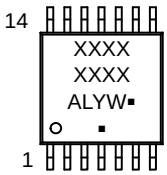


Micro8 /MSOP8
CASE 846A

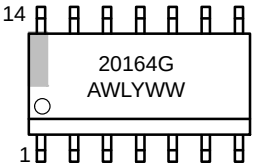


SOIC ï8
CASE 751

Quad Channel Configuration
NCS20164, NCV20164



TSSOP ï14
CASE 948G



SOIC ï14
CASE 751A

XXXXX	= Specific Device Code
A	= Assembly Location
WL, L	= Wafer Lot
Y	= Year
WW, W	= Work Week
G or ▪	= Pb Free Package

(Note: Microdot may be in either location)

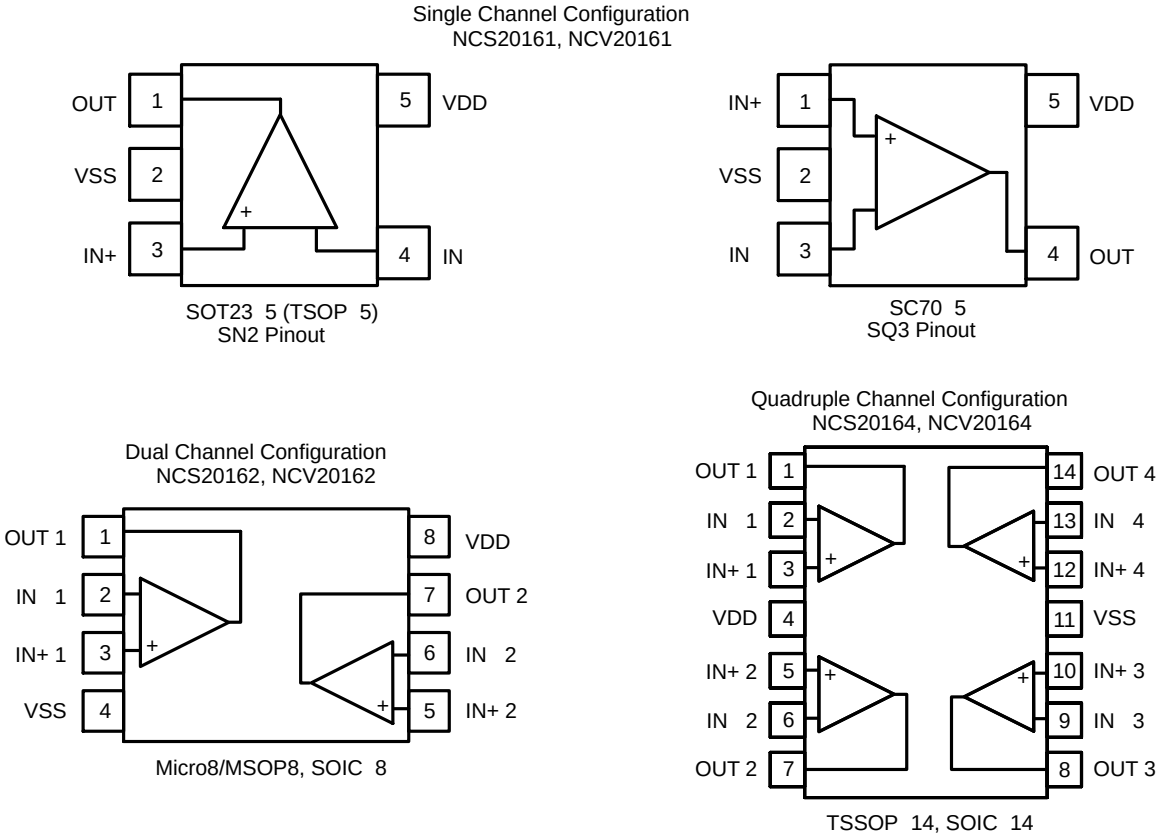


Figure 1. Pin Connections

ORDERING INFORMATION

Device*	Configuration	Automotive	Marking	Package	Shipping †
NCS20161SQ3T2G**	Single	No	TBD	SC70	3000 / Tape and Reel
NCS20161SN2T1G**			TBD	SOT23 5/TSOP 5	3000 / Tape and Reel
NCV20161SQ3T2G**		Yes	TBD	SC70	3000 / Tape and Reel
NCV20161SN2T1G**			TBD	SOT23 5/TSOP 5	3000 / Tape and Reel
NCS20162DMR2G**	Dual	No	TBD	Micro8/MSOP8	4000 / Tape and Reel
NCS20162DR2G			20162	SOIC 8	2500 / Tape and Reel
NCV20162DMR2G**		Yes	TBD	Micro8/MSOP8	4000 / Tape and Reel
NCV20162DR2G			20162	SOIC 8	2500 / Tape and Reel
NCS20164DR2G	Quad	No	20164G	SOIC 14	2500 / Tape and Reel
NCS20164DTBR2G**			TBD	TSSOP 14	2500 / Tape and Reel
NCV20164DR2G		Yes	20164G	SOIC 14	2500 / Tape and Reel
NCV20164DTBR2G**			TBD	TSSOP 14	2500 / Tape and Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC Q100 Qualified and PPAP Capable.

**In Development. Contact local sales office for more information.

ABSOLUTE MAXIMUM RATINGS (Note 1)

Rating	Symbol	Limit	Unit
Supply Voltage (V_{DD} – V_{SS})	V_S	0.3 to 6	V
Common Mode Input Voltage	V_I	V_{SS} 0.3 to V_{DD}+0.3	V
Differential Input Voltage	V_{ID}	V_{DD} – V_{SS}+0.2	V
Maximum Input Current	I_I	±10	mA
Maximum Output Current (Note 2)	I_O	±100	mA
Continuous Total Power Dissipation (Note 2)	P_D	200	mW
Maximum Junction Temperature	T_J	150	°C
Storage Temperature Range	T_{STG}	65 to 150	°C
Mounting Temperature (Infrared or Convection – 20 sec)	T_{mount}	260	°C
ESD Capability (Note 3) Human Body Model Charge Device Model	HBM CDM	2500 1500	V
Latch Up Current (Note 4)	I_{LU}	100	mA
Moisture Sensitivity Level (Note 5)	MSL	Level 1	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Refer to ELECTRICAL CHARACTERISTICS for Safe Operating Area.
2. Continuous short circuit operation to ground at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C. Output currents in excess of the maximum output current rating over the long term may adversely affect reliability. Shorting output to either VDD or VSS will adversely affect reliability.
3. This device series incorporates ESD protection and is tested by the following methods:
   ESD Human Body Model tested per JEDEC standard Js 001 2017 (AEC Q100 002)
   ESD Charged Device Model tested per JEDEC standard JS 002 2014 (AEC Q100 011)
4. Latch up Current tested per JEDEC standard JESD78E (AEC Q100 004)
5. Moisture Sensitivity Level tested per IPC/JEDEC standard: J STD 020A

OPERATING RANGES

Parameter	Symbol	Min	Max	Unit
Operating Supply Voltage (V_{DD} V_{SS})	V_S	1.8	5.5	V
Differential Input Voltage	V_{ID}		V_S	V
Common Mode Input Voltage Range	V_{CM}	V_{SS} – 0.1	V_{DD} + 0.1	V
Ambient Temperature	T_A	40	125	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

THERMAL CHARACTERISTICS (Note 6)

Package	Junction ïto ïAmbient Thermal Resistance JA	Junction ïto ïCase Top Thermal Resistance JT	Junction ïto ïBoard Thermal Resistance JB	Unit

.565 .90707 re f BT rf>Tj /T29fm -.00b3A>Tj /TT4 1 Tf .5808 0 TD -.0032 T7If any of8.309 .90709 34.f B96e f 59.754 636.832 272.58 .9255BT 2 f BT 8 0 0 89

ELECTRICAL CHARACTERISTICS AT V_S = 1.8 V to 5.5 V
T_A = 25°C; R_L 10 k connected to mid ïsupply; V_{CM} = V_{OUT} = mid ïsupply unless otherwise noted.
Boldface limits apply over the specified temperature range, T_A = ï40°C to 125°C. (Note 7)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Input Offset Voltage	V_{OS}	V_S = 5 V	ï	±0.3	±2.1	mV
		V_S = 5 V	ï	ï	±2.6	mV
Offset Voltage Drift	dV_{OS}/dT	V_S = 5 V	ï	±1.5	ï	V/°C
Input Bias Current (Note 7)	I_{IB}		ï	±5	ï	pA
Input Offset Current (Note 7)	I_{OS}		ï	±5	ï	pA
Channel Separation		DC	ï	100	ï	dB
Input Capacitance	C_{IN}		ï	4	ï	pF
Common Mode Rejection Ratio	CMRR	V_S = 5.5 V, V_{CM} = V_{SS} ï 0.1 V to V_{DD} ï 1.4 V	80	103	ï	dB
		V_S = 5.5 V, V_{CM} = –0.1 V to 5.6 V	57	79	ï	
		V_S = 1.8 V, V_{CM} = V_{SS} ï 0.1 V to V_{DD} ï 1.4 V	ï	91	ï	
		V_S = 1.8 V, V_{CM} = –0.1 V to 1.9 V	ï	71	ï	
OUTPUT CHARACTERISTICS						
Open Loop Voltage Gain	A_{VOL}	V_S = 1.8 V, V_{SS} + 0.04 V < V_O < V_{DD} – 0.04 V, R_L = 10 k	ï	100	ï	dB
		V_S = 5.5 V, V_{SS} + 0.05 V < V_O < V_{DD} – 0.05 V, R_L = 10 k	101	108	ï	
		V_S = 1.8 V, V_{SS} + 0.06 V < V_O < V_{DD} – 0.06 V, R_L = 2 k	ï	97	ï	
		V_S = 5.5 V, V_{SS} + 0.15 V < V_O < V_{DD} – 0.15 V, R_L = 2 k	ï	113	ï	
Short Circuit Current	I_{SC}	Output sourcing current V_S = 5 V	ï	40	ï	mA
		Output sinking current, V_S = 5 V	ï	50		
Output Voltage Swing from V_{DD}	V_{DD} ï V_{OH}	V_S = 5.5 V, R_L = 10 k	ï	3	20	mV
		V_S = 5.5 V, R_L = 2 k	ï	ï	60	
Output Voltage Swing from V_{SS}	V_{OL} ï V_{SS}	V_S = 5.5 V, R_L = 10 k	ï	3	20	mV
		V_S = 5.5 V, R_L = 2 k	ï	ï	60	
AC CHARACTERISTICS						
Unity Gain Bandwidth	UGBW	V_S = 5 V, G = +1	ï	8	ï	MHz
Slew Rate at Unity Gain	SR	V_S = 5 V, G = +1	ï	3.5	ï	V/ s
Phase Margin	m	V_S = 5 V, G = +1	ï	52	ï	
Gain Margin	A_m		ï	11	ï	dB
Settling Time to 0.1%	t_S	V_S = 5 V, V_{IN} = 2 V step, G = +1, C_L = 100 pF	ï	0.5	ï	µs
Settling Time to 0.01%	t_S	V_S = 5 V, V_{IN} = 2 V step, G = +1, C_L = 100 pF	ï	1	ï	µs
Overload Recovery Time	t_{OR}	V_S = 5 V, V_{IN} x gain > V_S	ï	1	ï	µs
Open Loop Output Impedance	Z_{OL}	V_S = 5 V, f = 10 MHz	ï	240	ï	

ELECTRICAL CHARACTERISTICS AT V_S = 1.8 V to 5.5 V (continued)
T_A = 25°C; R_L 10 k connected to mid supply; V_{CM} = V_{OUT} = mid supply unless otherwise noted.
Boldface limits apply over the specified temperature range, T_A = 40°C to 125°C. (Note 7)

TYPICAL CHARACTERISTICS

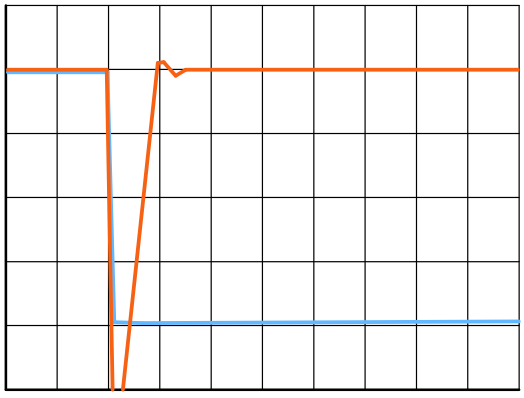
(AT T_A = 25°C, V_{CM} = MID SUPPLY, C_L = 20 PF, R_L = 10 K TO MID

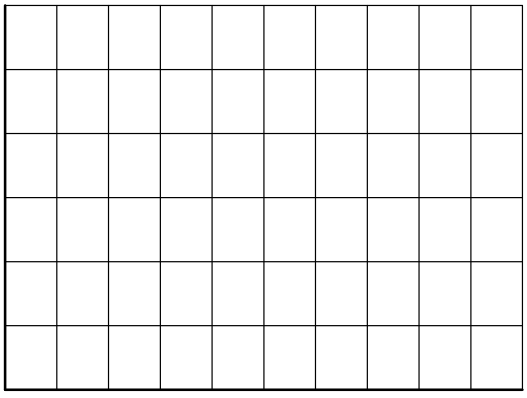
TYPICAL CHARACTERISTICS

(AT T_A = 25°

TYPICAL CHARACTERISTICS

(AT T_A = 25°C, V_{CM} = MID SUPPLY, C_L = 20 PF, R_L = 10 K TO MID SUPPLY, UNLESS OTHERWISE NOTED)





TYPICAL CHARACTERISTICS

(AT T_A = 25°C, V_{CM} = MID SUPPLY, C_L = 20 PF, R_L = 10 K TO MID

TYPICAL CHARACTERISTICS

(AT T_A = 25°C, V_{CM} = MID SUPPLY, C_L = 20 PF, R_L = 10 K TO MID SUPPLY, UNLESS OTHERWISE NOTED)

APPLICATION INFORMATION

The NCS20161 family of operational amplifiers is manufactured using **onsemi**'s CMOS process. Products in this class are general purpose, unity gain stable amplifiers and include single, dual and quad configurations.

Rail ïto ïRail Input with No Phase Reversal

The NCS2016x operational amplifiers are designed to prevent phase reversal or any similar issues when the input pins potential exceed the supply voltages by up to 100 mV.

The input stage of the NCS20161 family consists of two differential CMOS input stages connected in parallel: the first is constructed using paired PMOS devices and it operates at low common mode input voltages (V_{CM}), the second stage is build using paired NMOS devices to operate at high V_{CM}. The transition between the two input stages occurs at a common mode input voltage of approximately V_{DD} ï1.3V.

Limiting Input Voltages

In order to prevent damage and/or improper operation of these amplifiers, the application circuit must never expose the input pins to voltages or currents higher than the Absolute Maximum Ratings.

The internal ESD structure includes special diodes to protect the input stages while maintaining a low input bias current (I_B). The input protection circuitry clamp the inputs when the signals applied exceed more than one diode drop below VSS or one diode drop above VDD. Very fast ESD events (within the limits specified) trigger the protection structure so the operational amplifier is not damaged.

In order to safe guard against excessive voltages across the op amp's inputs, external clamp diodes can be used as shown in Figure 40. The four low ïdrop fast diodes (Schottky preferred) are used in parallel with the internal structure to divert the excessive energy to the supply rails where it can be easily dissipated or absorbed by the supply capacitors. The application designer should also take into account that these external diodes add leakage currents and parasitic capacitance that must be considered when evaluating the end ïto ïendperformance of the amplifier stage.

Limiting Input Currents

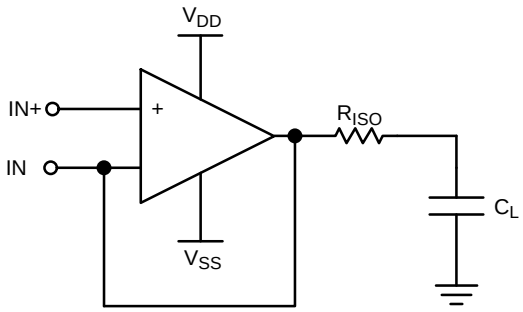


Figure 41. Driving Capacitive Loads

Simulating the application with **onsemi**'s Spice model is a good starting point for selecting the isolation resistor's value. Bench testing the frequency and step response can be used to fine−tune the value according to the desired characteristic.

Unity Gain Bandwidth

Interfacing a high impedance sensor's output to a relatively low−impedance ADC input usually requires an intermediate stage to avoid unwanted interference of the two devices, and this stage needs to have a high input impedance, a low output impedance, and high output current.

The unity gain buffer is recommended here (Figure 42). The ADC's internal sampling capacitor requires a buffer front−end to recharge it faster than the sampling time, and this problem is even worse if more channels are sampled by the same ADC using an internal multiplexer. In order to achieve a settling time shorter than the multiplexed sampling rate, an RC stage is recommended between the buffer and the ADC input. The R_{ISO} resistor's value should be low enough to charge the capacitor quickly, but at the same time large enough to isolate the capacitive load from the amplifier output to preserve phase margin. When transients are generated by the sensor's output, first the two amplifier inputs see a high differential voltage between them, then the output settles and brings the inverting input back to the correct voltage.

Let us take an example of a 0.1 V to 4 V sensor signal. To successfully accommodate it, the differential input range of the NCS2016x is close to the supply range and the output will match the input. The differential input voltage is limited only by the ESD protection structure and not by back−to−back diodes between inputs.

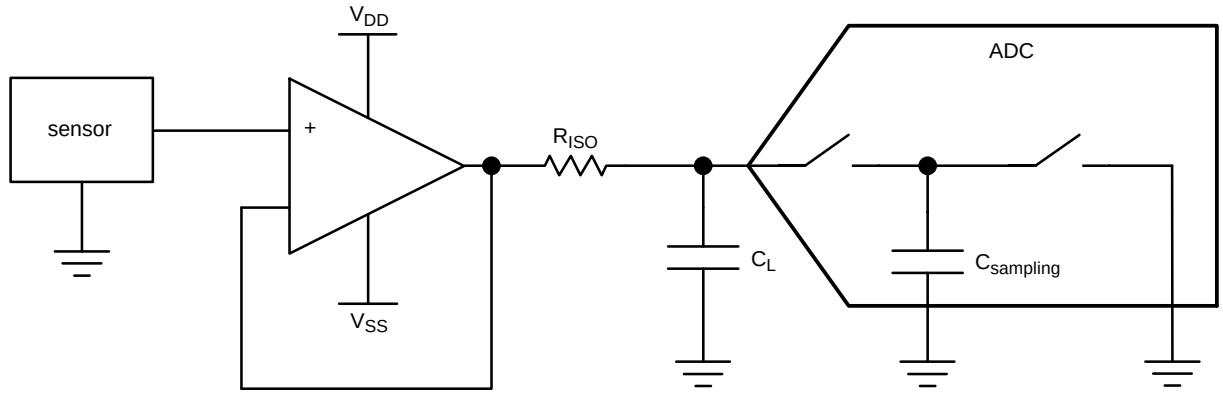


Figure 42. Unity Gain Buffer Stage for Sampling with ADC

Power Supply Bypassing

For AC, the power supply pins (VDD and VSS for split supply, VDD for single supply) should be bypassed locally with a quality capacitor in the range of 100 nF as close as possible to the amplifier supply pins. Ceramic capacitors are recommended for their low ESR and good high frequency response.

For DC, a bulk capacitor in the range of 1 μF placed within inches distance from the op amp can provide the additional current needed to drive higher loads.

Unused Operational Amplifiers

Occasionally not all the op amp channels offered in the quad packages are needed for a specific application. They can be connected as "buffering ground" as shown in Figure 43, a solution that does not need any extra parts. Connecting them differently (inputs split to rails, left floating, etc.) can sometimes cause unwanted oscillation, crosstalk, increased current consumption, or add noise to the supply rails.

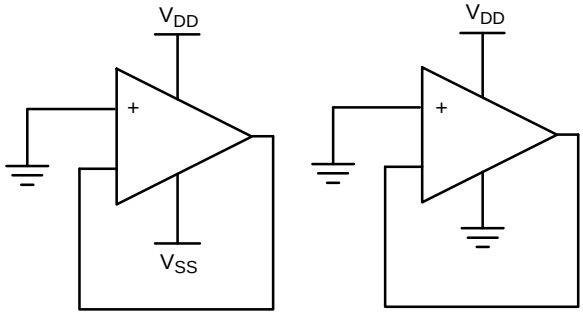
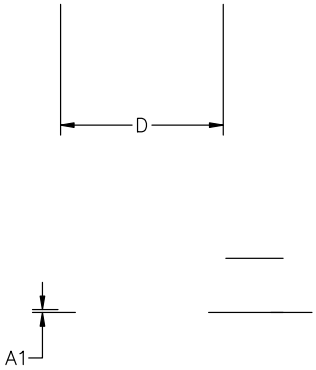


Figure 43. Unused Operational Amplifiers

PACKAGE DIMENSIONS

PACKAGE DIMENSIONS

TSOP ï5 3.00x1.50x0.95, 0.95P
CASE 483
ISSUE P



PACKAGE DIMENSIONS

Micro8
CASE 846A 02
ISSUE K

NOTES:

DIM	MILLIMETERS		
	MIN.	NOM.	
A	---	---	
A1	0.05	0.08	
c	0.13	0.18	
E			

RECOMMENDED
MOUNTING FOOTPRINT