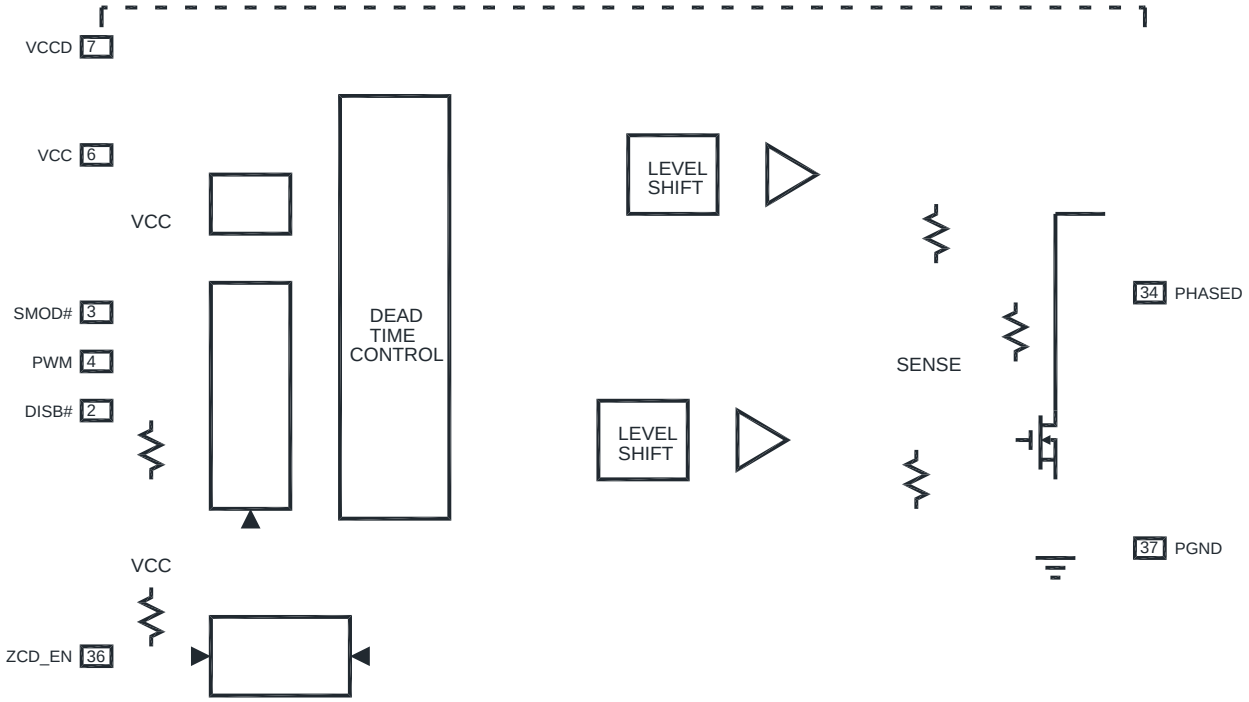


Figure 2. Block Diagram

PIN LIST AND DESCRIPTIONS (continued)

Pin No.	Symbol	Description
19	PGND	Power Ground
20	PGND	Power Ground
21	PGND	Power Ground
22	PGND	Power Ground
23	PGND	Power Ground
24	PGND	Power Ground
25	VIN	Conversion Supply Power Input
26	VIN	Conversion Supply Power Input
27	VIN	Conversion Supply Power Input
28	VIN	Conversion Supply Power Input
29	VIN	Conversion Supply Power Input
30	VIN	Conversion Supply Power Input
31	PGND	Power Ground
[redacted]	PHASEF	

THERMAL INFORMATION

Rating	Symbol	Value	Unit
Thermal Resistance	JA	22	°C/W
	$R\Psi_{J-BT}$	2	°C/W
	$R\Psi_{J-CT}$	4	°C/W
Operating Junction Temperature Range (Note 2)	T_J	−40 to +150	°C
Operating Ambient Temperature Range		−40 to +125	°C
Maximum Storage Temperature Range	T_{STG}	−40 to +150	°C
Maximum Power Dissipation		10	W
Moisture Sensitivity Level	MSL	3	

2. The maximum package power dissipation must be observed.
3. JESD 51−5 (1S2P Direct−Attach Method) with 0 LFM
4. JESD 51−7 (1S2P Direct−Attach Method) with 0 LFM

RECOMMENDED OPERATING CONDITIONS

Parameter	Pin Name	Conditions	Min	Typ	Max	Unit
Supply Voltage Range	VCC, VCCD		4.5	5.0	5.5	V
Conversion Voltage						

ELECTRICAL CHARACTERISTICS (continued)
(V_{VCC} = V_{VCCD} = 5.0 V, V_{VIN} = 12 V, $V_{DISB\#}$ = 2.0 V, C_{VCCD} = C_{VCC} = 0.1 μF unless specified otherwise) Min/Max values are valid for the temperature range −40°C ≤ T_A ≤ 125

ELECTRICAL CHARACTERISTICS (continued)
(V_{VCC} = V_{VCCD} = 5.0 V, V_{VIN} = 12 V, $V_{DISB\#}$ = 2.0 V, C_{VCCD} = C_{VCC} = 0.1 μF unless specified otherwise) Min/Max values are valid for the temperature range −40°C ≤ T_A ≤ 125°C unless noted otherwise, and are guaranteed by test, design or statistical correlation.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
ZCD_EN INPUT						
ZCD_EN Propagation Delay, Rising	T_{ZCD_EN,PD_R}	SMOD# = High, ZCD_EN = High to GL = 10%	−	40	45	ns
ZCD_EN Propagation Delay, Falling	T_{ZCD_EN,PD_F}	SMOD# = High, ZCD_EN = Low to GL = 90%	−	25	40	ns
ZCD FUNCTION						
Zero Cross Detect Threshold	V_{ZCD}		−	−6.5	−	mV
ZCD Blanking + Debounce Time	t_{BLNK}		−	330	−	ns
NON−OVERLAP DELAYS						
Non−overlap Delay, Leading Edge	$tpdh_{GH}$	GL Falling = 1 V to GH−VSW Rising = 1 V	−	13	−	ns
Non−overlap Delay, Trailing Edge	$tpdh_{GL}$	GH−VSW Falling = 1 V to GL Rising = 1 V	−	12	−	ns
THERMAL WARNING & SHUTDOWN						
Thermal Warning Temperature	T_{THWN}	Temperature at Driver Die	−	150	−	°C
Thermal Warning Hysteresis	T_{THWN_HYS}		−	15	−	°C
Thermal Shutdown Temperature	T_{THDN}	Temperature at Driver Die	−	180	−	°C
Thermal Shutdown Hysteresis	T_{THDN_HYS}		−	25	−	°C
THWN Open Drain Current	I_{THWN}		−	−	5	mA
BOOSTSTRAP DIODE						
Forward Voltage		Forward Bias Current = 2.0 mA	−	300	−	mV

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

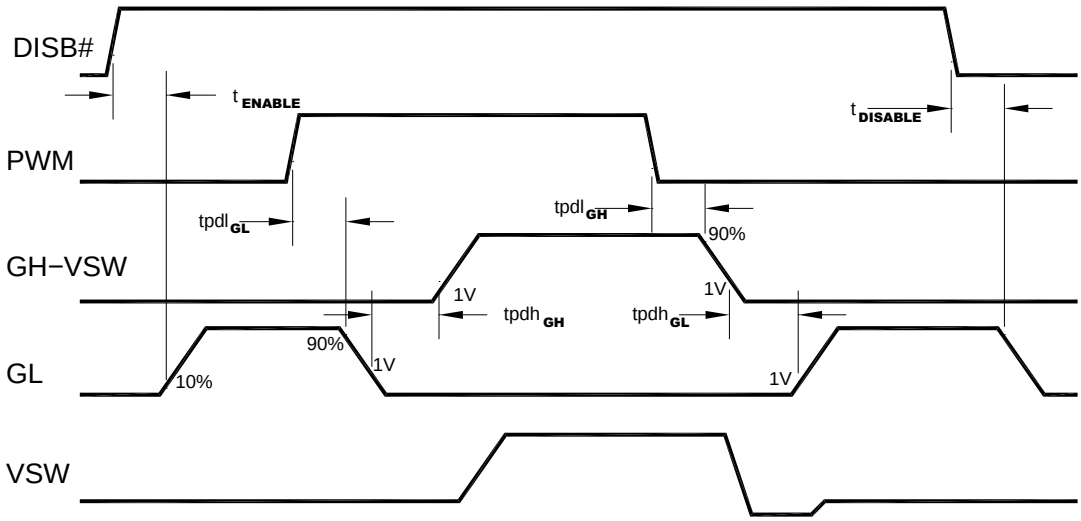


Figure 3. Timing Diagram

Table 1. LOGIC TABLE

INPUT TRUTH TABLE					
DISB#	**PWM**	**SMOD#** (Note 5)	**ZCD_EN**	**GH**	**GL**
L	X				

If $V_{SMOD\#\_LO}$ < SMOD# < $V_{SMOD\#\_HI}$ (Mid−State), internal resistances will set undriven PWM pin voltage to Mid−State.

Disable Input (DISB#)

The DISB# pin is used to disable the GH to the High−Side FET to prevent power transfer. The pin has a pull−down resistance to force a disabled state when it is left unconnected. DISB# can be driven from the output of a logic device or set high with a pull−up resistance to VCC.

VCC Undervoltage Lockout

The VCC pin is monitored by an Undervoltage Lockout Circuit (UVLO). VCC voltage above the rising threshold enables the NCP81382.

Table 2. UVLO/DISB# LOGIC TABLE

UVLO	DISB#	Driver State
L	X	Disabled (GH = GL = 0)
H	L	Disabled (GH = GL = 0)
H	H	Enabled (See Table x)
H	Open	Disabled (GH = GL = 0)

Thermal Warning/Thermal Shutdown Output

The THWN pin is an open drain output. When the temperature of the driver exceeds T_{THWN}, the THWN pin will be pulled low indicating a thermal warning. At this point, the part continues to function normally. When the temperature drops T_{THWN_HYS} below T_{THWN}, the THWN pin will go high. If the driver temperature exceeds T_{THDN}, the part will enter thermal shutdown and turn off both MOSFETs. Once the temperature falls T_{THDN_HYS} below T_{THDN}, the part will resume normal operation.

Skip Mode Input (SMOD#)

The SMOD# tri−state input pin has an internal pull−up resistance to VCC. When driven high, the SMOD# pin enables the low side synchronous MOSFET to operate independently of the internal ZCD function. When the SMOD# pin is set low during the PWM cycle it disables the low side MOSFET to allow discontinuous mode operation.

The NCP81382 has the capability of internally connecting a resistor divider to the PWM pin. To engage this mode, SMOD# needs to be placed into mid−state. While in SMOD# mid−state, the IC logic is equivalent to SMOD# being in the high state.

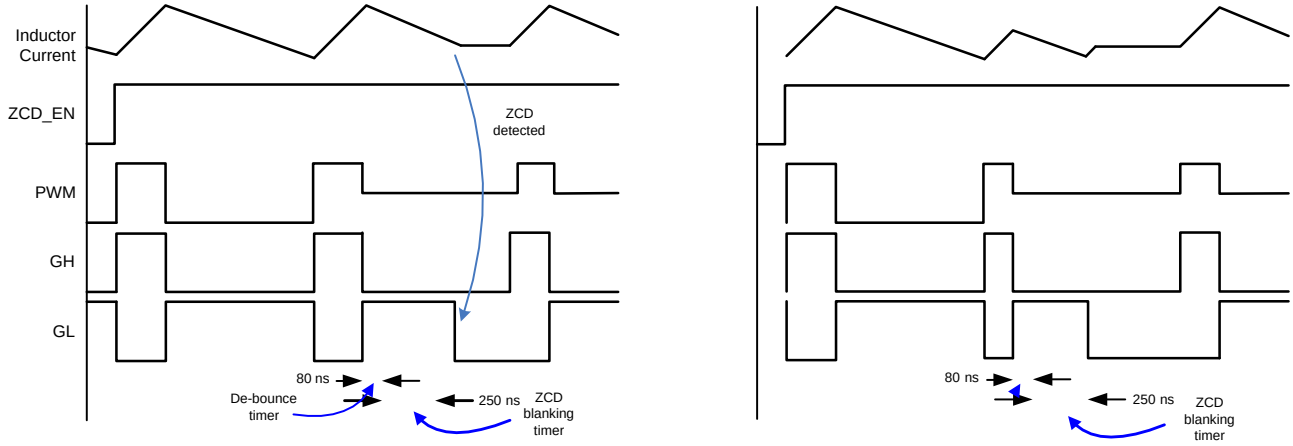


Figure 6. PWM Timing Diagram

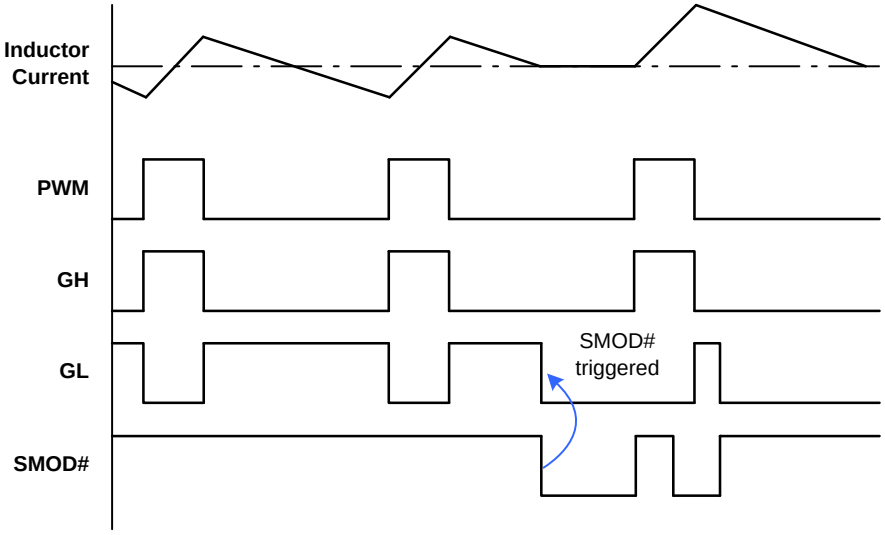


Figure 7. SMOD# Timing Diagram

NOTE: If the SMOD# input is driven low at any time after the GL has been driven high, the SMOD# Falling edge will trigger the GL to go low.
If the SMOD# input is driven low while the GH is high, the SMOD# input is ignored.

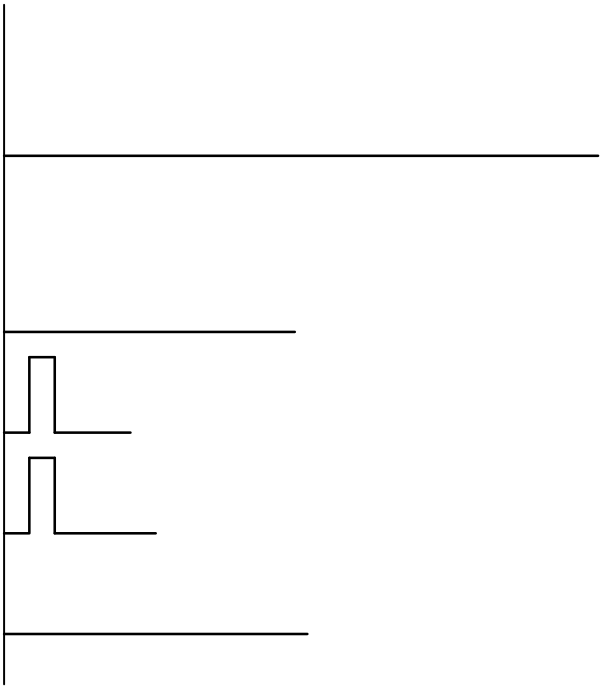


Figure 8. ZCD_EN Timing Diagram

For Use with Controllers with 3−State PWM and No Zero Current Detection Capability:

Table 3. LOGIC TABLE − 3−STATE PWM CONTROLLERS WITH NO ZCD

PWM	SMOD#	ZCD_EN	GH	GL
H	H	H	ON	OFF
M	H	H	OFF	ZCD
L	H	H		

For Use with Controllers with 2−Level PWM and Zero Current Detection Capability:

Table 5. LOGIC TABLE − 2−STATE PWM CONTROLLERS WITH ZCD

PWM	SMOD#	ZCD_EN	GH	GL
H	L	X	ON	OFF
L	L	H	OFF	ON
L	L	L	OFF	OFF

This section describes operation with controllers that do not have 3−level PWM output capability but are capable of zero current detection during discontinuous conduction mode (DCM).

The SMOD# pin needs to be pulled low (below $V_{SMOD\#\_LO}$).

When PWM is high, GH will always be in the high state and GL will always be in the low state, regardless of the state ZCD_EN is in.

When PWM is in the low state, the state of ZCD_EN determines whether the converter is placed into diode emulation mode. When the controller detects positive inductor current, ZCD_EN should be in the high state, allowing the LS FET to be on and conducting. Once the controller detects zero or negative current, ZCD_EN should be placed into the low state, turning off the LS FET. With the LS FET turned off, the body diode of the LS FET allows any positive current that may still be flowing to reach zero, but prevents the current from flowing in the negative direction.

Figure 11. Timing Diagram − 2−state PWM Controller, with ZCD

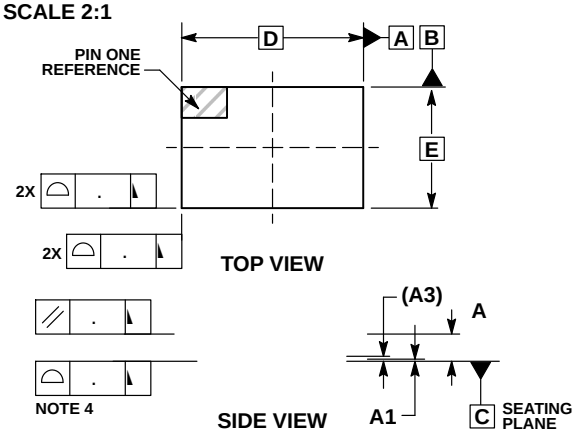
Recommended PCB Layout
(viewed from top)

QFN36 6x4, 0.4P
CASE 485DZ
ISSUE A

1 36

DATE 19 JUN 2015

SCALE 2:1



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.25 MM FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS	
DIM	**MIN**	**MAX**
A	0.90	1.20
A1	0.00	0.05
A3	0.20 REF	
b	0.15	0.25
D	6.00 BSC	
D2	4.95	5.05

E	4.00 BSC	
E2	2.44	2.54

e	0.40 BSC	
G	0.52	0.62

*For additional information on our Pb−Free strategy and soldering details, please download the