81380

The NCP81380 integrates a MOSFET driver, high−side MOSFET and low−side MOSFET into a single package.

The driver and MOSFETs have been optimized for high−current DC−DC buck power conversion applications. The NCP81380 integrated solution greatly reduces package parasitics and board space compared to a discrete component solution.

www.onsemi.com

Features

- Capable of Average Currents up to 15 A
- Capable of Switching at Frequencies up to 2 MHz
- Capable of Peak Currents up to 40 A
- Compatible with 3.3 V or 5 V PWM Input
- Responds Properly to 3−level PWM Inputs
- Option for Zero Cross Detection with 3−level PWM
- ZCD_EN Input for Diode Emulation with 2−level PWM
- Internal Bootstrap Diode
- Undervoltage Lockout
- Supports Intel® Power State 4
- Thermal Warning output
- Thermal Shutdown
- This is a Pb−Free Device

Applications

- Desktop & Notebook Microprocessors

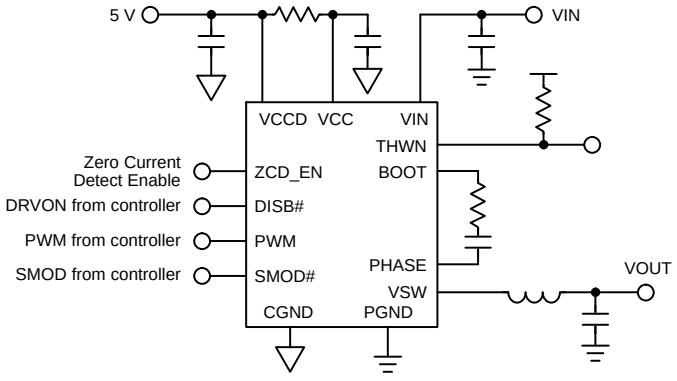


Figure 1. Application Schematic

ORDERING INFORMATION

Device	Package	Shipping†

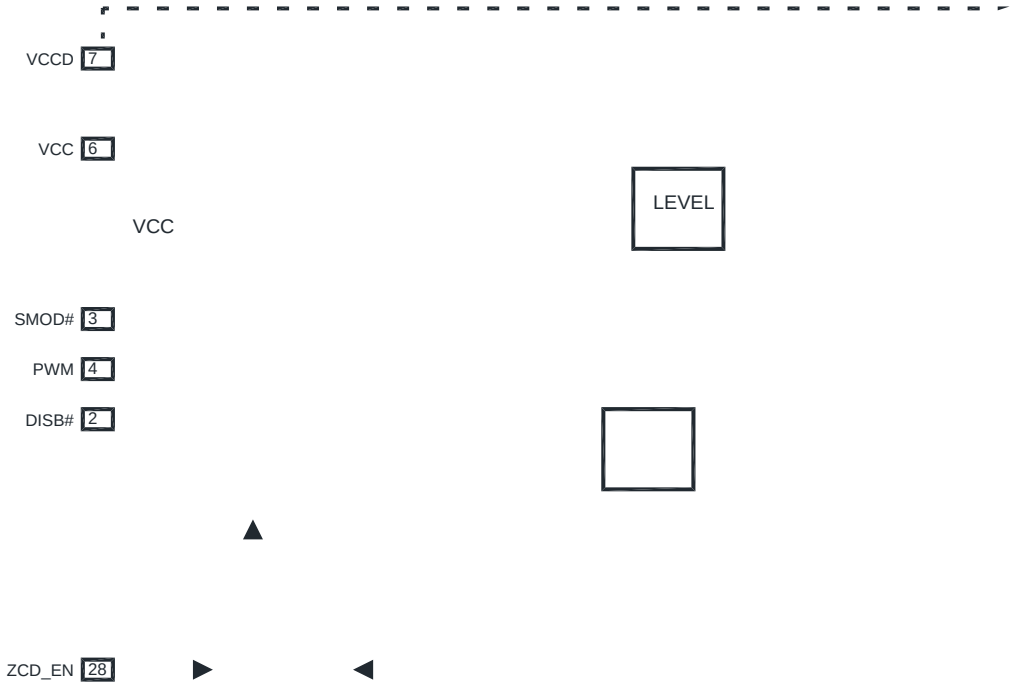


Figure 2. Block Diagram

PIN LIST AND DESCRIPTIONS

Pin No.	Symbol	Description
18	PGND	Power Ground
19	PGND	Power Ground
20	VSW	Switchnode Output
21	VSW	Switchnode Output
22	VSW	Switchnode Output
23	VSW	Switchnode Output
24	VSW	Switchnode Output
25	PHASE	Connection for Bootstrap Network
26	GH	High Side FET Gate Access
27	BOOT	Connection for Bootstrap Network
28	ZCD_EN	PWM drive logic and zero current detection enable. 3−state input: PWM = High → GH is high, GL is low. PWM = Mid → Diode emulation mode. PWM = Low → GH is low. State of GL is dependent on states of SMOD# and ZCD_EN (see Table 1 LOGIC TABLE).
29	PGND	Power Ground
30	TEST	No connection should be made to this pin. No pad is needed on the PCB footprint

ABSOLUTE MAXIMUM RATINGS (Electrical Information − all signals referenced to PGND unless noted otherwise) (Note 1)

Pin Name	Min	Max	Unit
VCC, VCCD	−0.3	6.5	V
GH to PHASE (DC)	−0.3	$V_{BOOT} - V_{SW} + 0.3$	V
GH to PHASE (< 50 ns)	−5	7.7	V
VIN	−0.3	30	V
BOOT (DC)			

THERMAL INFORMATION

Rating	Symbol	Value	Unit
Thermal Resistance	θ_{JA}	28.7	°C/W
	$R\Psi_{J-BT}$		

ELECTRICAL CHARACTERISTICS (continued)
(V_{VCC} = V_{VCCD} = 5.0 V, V_{VIN} = 12 V, $V_{DISB\#}$ = 2.0 V, C_{VCCD} = C_{VCC} = 0.1 μF unless specified otherwise) Min/Max values are valid for the temperature range −40°C ≤ T_A ≤ 125°C unless noted otherwise, and are guaranteed by test, design or statistical correlation.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
VCCD SUPPLY CURRENT						
Operating		DISB# = 5 V, ZCD_EN = 5 V, PWM = 400 kHz	–	–	12	mA
Enabled, No switching		DISB# = 5 V, PWM = 0 V, V_{PHASE} = 0 V	–	175	300	μA
Disabled		DISB# = 0 V	–	0.1	1	μA
DISB# INPUT						
Input Resistance		To Ground, @ 25°C	–	461	–	kΩ
Upper Threshold	V_{UPPER}		–	–	2.0	V
Lower Threshold	V_{LOWER}		0.8	–	–	V
Hysteresis		V_{UPPER} – V_{LOWER}	200	–	–	mV
Enable Delay Time	t_{ENABLE}	Time from DISB# transitioning HI to when VSW responds to PWM.	–	–	40	μs
Disable Delay Time	$t_{DISABLE}$	Time from DISB# transitioning LOW to when both output FETs are off.	–	25	50	ns
PWM INPUT						
Input High Voltage	V_{PWM_HI}		2.65	–	–	V
Input Mid−state Voltage	V_{PWM_MID}		1.4	–	2.0	V
Input Low Voltage	V_{PWM_LO}		–	–	0.7	V
Input Resistance	R_{PWM_HIZ}	SMOD# = $V_{SMOD\#\_HI}$ or $V_{SMOD\#\_LO}$	10	–	–	MΩ
Input Resistance	R_{PWM_BIAS}	SMOD# = $V_{SMOD\#\_MID}$	–	63	–	kΩ
PWM Input Bias Voltage	V_{PWM_BIAS}	SMOD# = $V_{SMOD\#\_MID}$	–	1.7	–	V
PWM Propagation Delay, Rising	$tpdl_{GL}$	PWM = 2.25 V to GL = 90%; SMOD# = LOW	–	25	35	ns
PWM Propagation Delay, Falling	$tpdl_{GH}$	PWM = 0.75 V to GH = 90%	–	15	25	ns
Exiting PWM Mid−state Propagation Delay, Mid−to−Low	$T_{PWM\_EXIT\_L}$	PWM = Mid−to−Low to GL = 10%, ZCD_EN = High	–	13	25	ns
Exiting PWM Mid−state Propagation Delay, Mid−to−High	$T_{PWM\_EXIT\_H}$	PWM = Mid−to−High to GH = 10%	–	13	25	ns
SMOD# INPUT						
SMOD# Input Voltage High	V_{SMOD_HI}		2.65	–	–	V
SMOD# Input Voltage Mid−state	$V_{SMOD\#\_MID}$		1.4	–	2.0	V
SMOD# Input Voltage Low	V_{SMOD_LO}		–	–	0.7	V
SMOD# Input Resistance	$R_{SMOD\#\_UP}$	Pull−up resistance to VCC	–	440	–	kΩ
SMOD# Propagation Delay, Falling	$T_{SMOD\#\_PD\_F}$	SMOD# = Low to GL = 90%, PWM = Low	–	26	30	ns
SMOD# Propagation Delay, Rising	$T_{SMOD\#\_PD\_R}$	SMOD# = High to GL = 10%, ZCD_EN = High, PWM = Low	–	15	30	ns
ZCD_EN INPUT						
ZCD_EN Input Voltage High	$V_{ZCD\_EN\_HI}$		2.0	–	–	V
ZCD_EN Input Voltage Low	$V_{ZCD\_EN\_LO}$		–	–	0.8	V
ZCD_EN Hysteresis	$V_{ZCD\_EN\_HYS}$		–	250	–	mV

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

ELECTRICAL CHARACTERISTICS (continued)
(V_{VCC} = V_{VCCD} = 5.0 V, V_{VIN} = 12 V, $V_{DISB\#}$ = 2.0 V, C_{VCCD} = C_{VCC} = 0.1 μF unless specified otherwise) Min/Max values are valid for the temperature range −40°C ≤ T_A ≤ 125°C unless noted otherwise, and are guaranteed by test, design or statistical correlation.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
ZCD_EN INPUT						
ZCD_EN Input Resistance	$R_{ZCD\_EN\_PU}$	to VCC	−	270	−	kΩ
ZCD_EN Propagation Delay, Rising	T_{ZCD_EN,PD_R}	SMOD# = High, ZCD_EN = High to GL = 10%	−	40	45	ns
ZCD_EN Propagation Delay, Falling	T_{ZCD_EN,PD_F}	SMOD# = High, ZCD_EN = Low to GL = 90%	−	25	40	ns
ZCD FUNCTION						
Zero Cross Detect Threshold	V_{ZCD}		−	−6.5	−	mV
ZCD Blanking + Debounce Time	t_{BLNK}		−	330	−	ns
NON−OVERLAP DELAYS						
Non−overlap Delay, Leading Edge	$tpdh_{GH}$	GL Falling = 1 V to GH−VSW Rising = 1 V	−	13	−	ns
Non−overlap Delay, Trailing Edge	$tpdh_{GL}$	GH−VSW Falling = 1 V to GL Rising = 1 V	−	12	−	ns
THERMAL WARNING & SHUTDOWN						
Thermal Warning Temperature	T_{THWN}	Temperature at Driver Die	−	150	−	°C
Thermal Warning Hysteresis	T_{THWN_HYS}		−	15	−	°C
Thermal Shutdown Temperature	T_{THDN}	Temperature at Driver Die	−	180	−	°C
Thermal Shutdown Hysteresis	T_{THDN_HYS}		−	25	−	°C
THWN Open Drain Current	I_{THWN}		−	−	5	mA
BOOSTSTRAP DIODE						
Forward Voltage		Forward Bias Current = 2.0 mA	−	300	−	mV

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

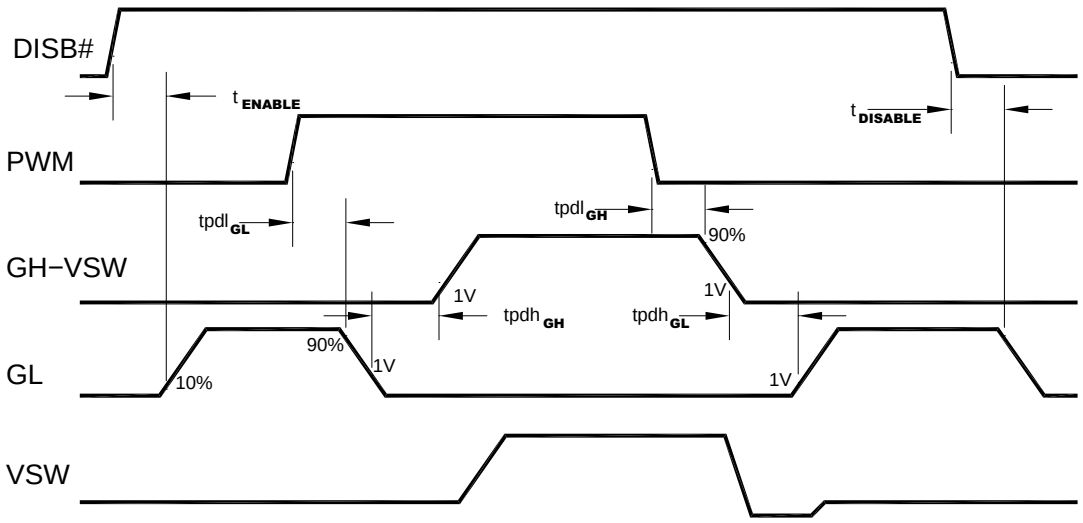


Figure 3. Timing Diagram

Table 1. LOGIC TABLE

INPUT TRUTH TABLE					
DISB#	**PWM**	**SMOD#** (Note 5)	**ZCD_EN**	**GH**	**GL**
L	X	X	X	L	L
H	H	X	X	H	L
H	L	X	L	L	L
H	L	X	H	L	H
H	MID	H or MID	H	L	ZCD (Note 6)
H	MID	X	L	L	L (Note 7)
H	MID	L	X	L	L (Note 7)

5. PWM input is driven to mid−state with internal divider resistors when SMOD# is driven to mid−state and PWM input is undriven externally.
6. GL goes low following 80 ns de−bounce time, 250 ns blanking time and then SW exceeding ZCD threshold.
7. There is no delay before GL goes low.

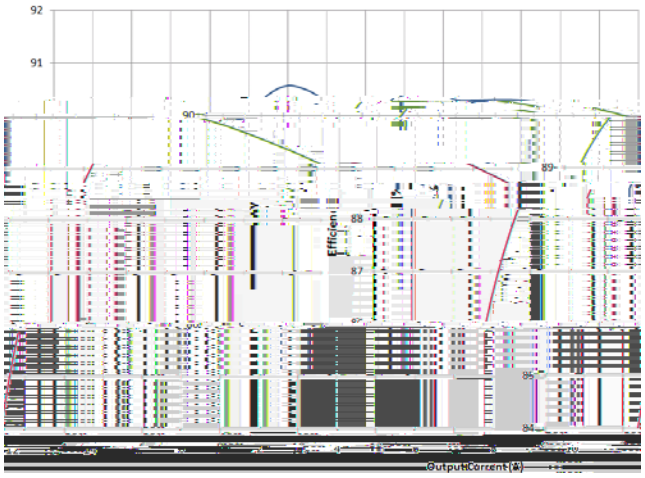


Figure 4. Efficiency − 12 V Input, 1.2 V Output, 500 kHz

Figure 5. Efficiency − 19 V Input, 1.2 V Output, 500 kHz

APPLICATIONS INFORMATION

Theory of Operation

The NCP81380 is an integrated driver and MOSFET module designed for use in a synchronous buck converter topology. The NCP81380 supports numerous application control definitions including ZCD (Zero Current Detect)

If $V_{SMOD\#\_LO}$ < SMOD# < $V_{SMOD\#\_HI}$ (Mid−State), internal resistances will set undriven PWM pin voltage to Mid−State.

Disable Input (DISB#)

The DISB# pin is used to disable the GH to the High−Side FET to prevent power transfer. The pin has a pull−down resistance to force a disabled state when it is left unconnected. DISB# can be driven from the output of a logic device or set high with a pull−up resistance to VCC.

VCC Undervoltage Lockout

The VCC pin is monitored by an Undervoltage Lockout Circuit (UVLO). VCC voltage above the rising threshold enables the NCP81380.

Table 2. UVLO/DISB# LOGIC TABLE

UVLO	DISB#	Driver State
L	X	Disabled (GH = GL = 0)
H	L	Disabled (GH = GL = 0)
H	H	Enabled (See Table x)
H	Open	Disabled (GH = GL = 0)

Thermal Warning/Thermal Shutdown Output

The THWN pin is an open drain output. When the temperature of the driver exceeds T_{THWN}, the THWN pin will be pulled low indicating a thermal warning. At this point, the part continues to function normally. When the temperature drops T_{THWN_HYS} below T_{THWN}, the THWN pin will go high. If the driver temperature exceeds T_{THDN}, the part will enter thermal shutdown and turn off both MOSFETs. Once the temperature falls T_{THDN_HYS} below T_{THDN}, the part will resume normal operation.

Skip Mode Input (SMOD#)

The SMOD# tri−state input pin has an internal pull−up resistance to VCC. When driven high, the SMOD# pin enables the low side synchronous MOSFET to operate independently of the internal ZCD function. When the SMOD# pin is set low during the PWM cycle it disables the low side MOSFET to allow discontinuous mode operation.

The NCP81380 has the capability of internally connecting a resistor divider to the PWM pin. To engage this mode, SMOD# needs to be placed into mid−state. While in SMOD# mid−state, the IC logic is equivalent to SMOD# being in the high state.

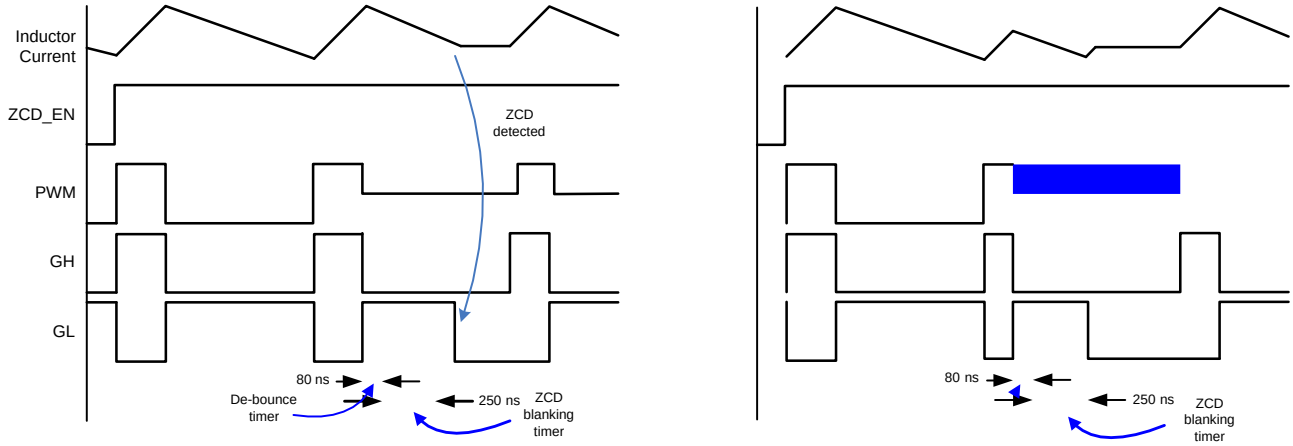


Figure 6. PWM Timing Diagram

For Use with Controllers with 3−State PWM and No Zero Current Detection Capability:

Table 3. LOGIC TABLE − 3−STATE PWM CONTROLLERS WITH NO ZCD

PWM	SMOD#	ZCD_EN	GH	GL
H	H	H	ON	OFF
M	H	H	OFF	ZCD
L	H	H	OFF	ON

This section describes operation with controllers that are capable of 3 states in their PWM output and relies on the NCP81380 to conduct zero current detection during discontinuous conduction mode (DCM).

The SMOD# pin needs to either be set to 5 V or left disconnected. The NCP81380 has an internal pull−up resistor that connects to VCC that sets SMOD# to the logic high state if this pin is disconnected.

The ZCD_EN pin needs to either be set to 5 V or left disconnected. The NCP81380 has an internal pull−up resistor connected to VCC that will set ZCD_EN to the logic high state if this pin is left disconnected.

To operate the buck converter in continuous conduction mode (CCM), PWM needs to switch between the logic high and low states. To enter into DCM, PWM needs to be switched to the mid−state.

For Use with Controllers with 3−state PWM and Zero Current Detection Capability:

Table 4. LOGIC TABLE − 3−STATE PWM CONTROLLERS WITH ZCD

PWM	SMOD#	ZCD_EN	GH	GL
H	L	H	ON	OFF
M	L	H	OFF	OFF
L	L	H	OFF	ON

This section describes operation with controllers that are capable of 3 PWM output levels and have zero current detection during discontinuous conduction mode (DCM).

The SMOD# pin needs to be pulled low (below $V_{SMOD\#\_LO}$).

The ZCD_EN pin needs to either be set to 5 V or left

Recommended PCB Layout
(viewed from top)

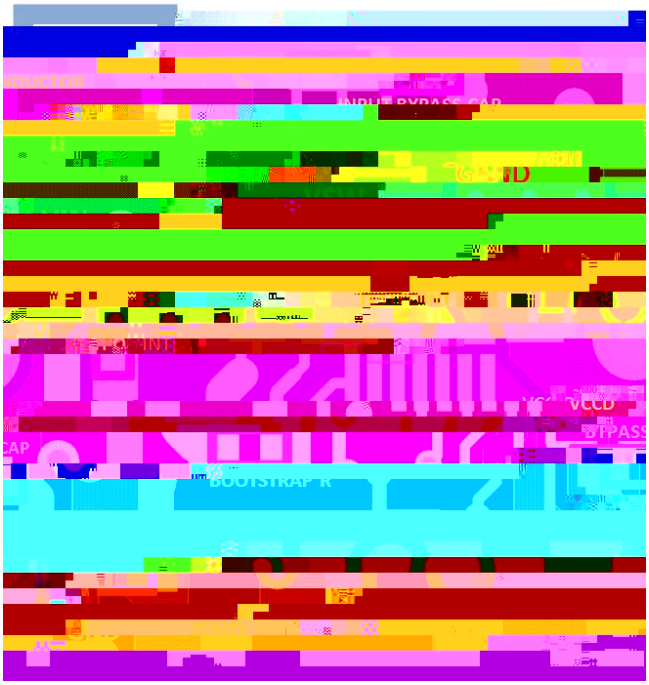


Figure 12. Top Copper Layer

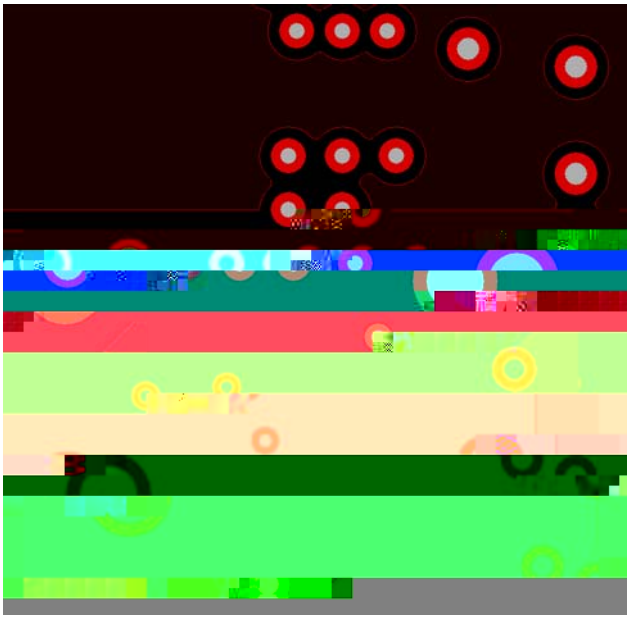


Figure 13. Bottom Copper Layer

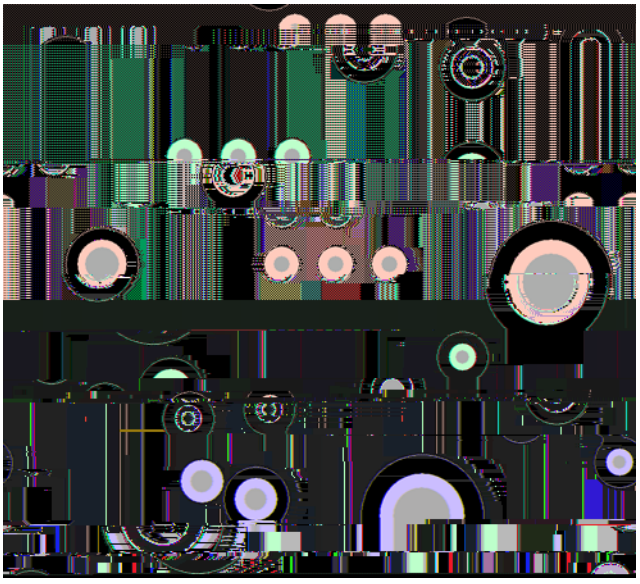


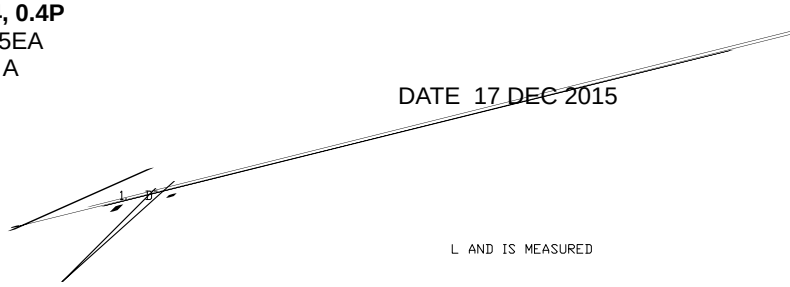
Figure 14. Layer 2 Copper Layer (Ground Plane)

QFN28 4x4, 0.4P
CASE 485EA
ISSUE A

LATED TERMINA

SCALE 2:1

DATE 17 DEC 2015



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