

NCP5369N

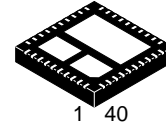
Integrated Driver and MOSFET

The NCP5369N integrates a MOSFET driver, high-side MOSFET and low-side MOSFET into a 6 mm x 6 mm 40-pin QFN package. The driver and MOSFETs have been optimized for high-current DC-DC buck power conversion applications. The NCP5369N integrated cs Ia lo m x 6discrete cs Indust ledOx integratFTDeures1 Tf1 0 0 6 1268.7112 685.8142551.79201 Tc(€ Tf10 0 0 10 68.7118



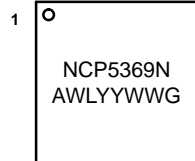
ON Semiconductor

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**QFN40
MN SUFFIX
CASE 485AZ**

MARKING DIAGRAM



- A = Assembly Location
- WL = Wafer Lot
- YY = Year
- WW = Work Week
- G = Pb-Free Package

- These are Pb-Free Devices

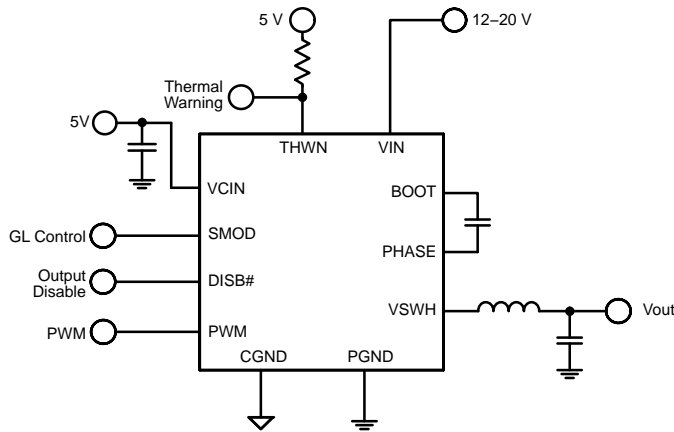


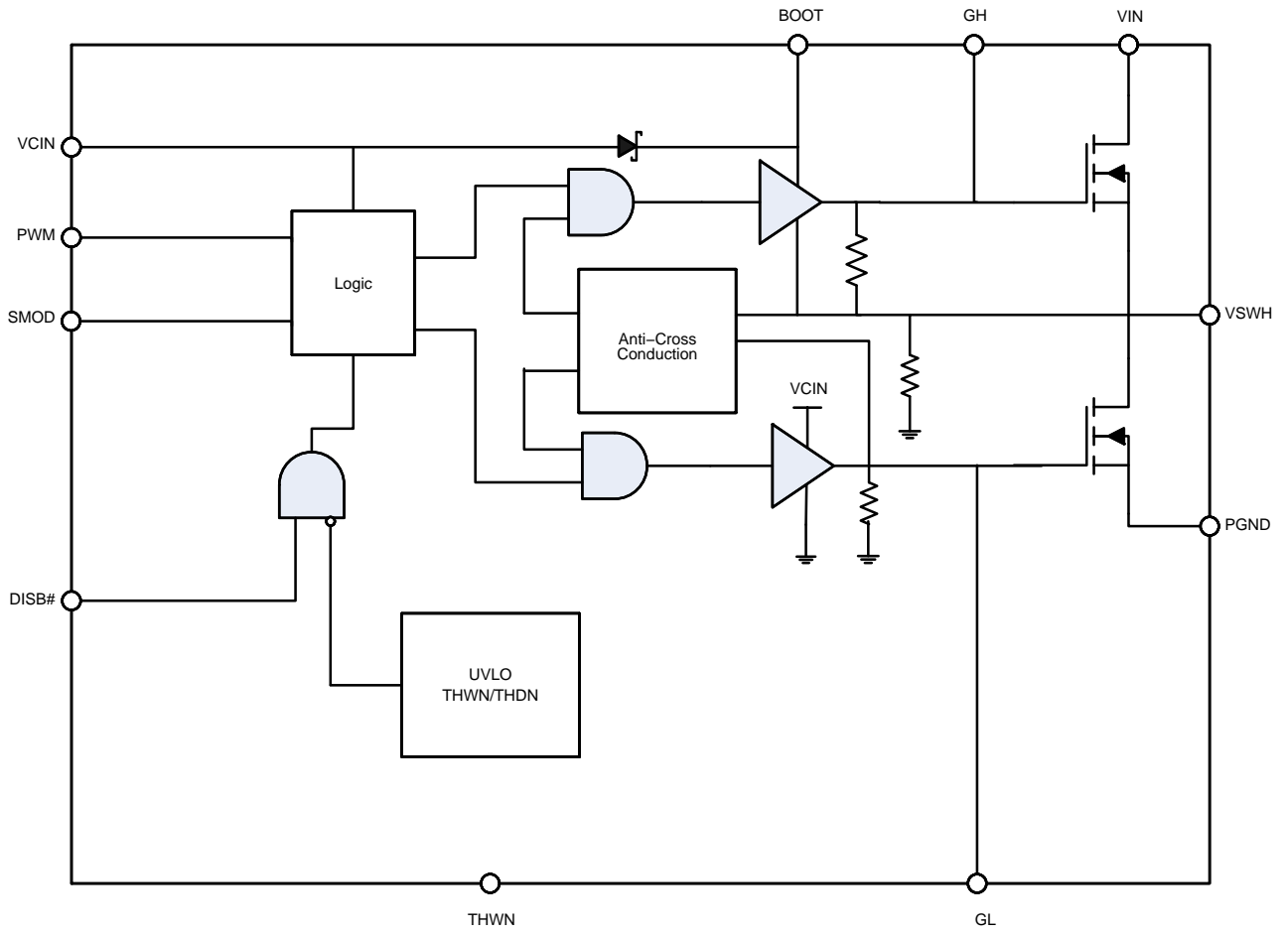
Figure 1. Application Schematic

ORDERING INFORMATION

Device	Package	Shipping†
NCP5369NMNTXG	QFN40 (Pb-Free)	2500/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

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Table 1. PIN FUNCTION DESCRIPTION

Pin No.	Pin Name	Description
1	SMOD	GL Control
2	VCIN	Control Input Voltage
3, 8	NC	No Connect
4	BOOT	Bootstrap Voltage
5, 37, FLAG 41	CGND	Control Signal Ground
6	GH	High Side FET Gate Access
7		

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Table 3. OPERATING RANGES

Rating	Symbol	Min	Typ	Max	Unit
Control Input Voltage	VCIN	4.5	5	5.5	V
Input Voltage	VIN	4.5	12	25	V

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

ELECTRICAL CHARACTERISTICS (Note 1) (VCIN = 5 V, VIN = 12 V, TA = -10°C to +100°C, unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
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SUPPLY CURRENT

VCIN Current (normal mode)	-	DISB# = 5 V, PWM = OSC, FSW = 400 kHz		14	20	mA
VCIN Current (shutdown mode)	-	DISB# = GND		15	30	μA

UNDERVOLTAGE LOCKOUT

UVLO Startup	-		3.8	4.35	4.5	V
UVLO Hysteresis	-		150	200		

APPLICATIONS INFORMATION

Theory of Operation

The NCP5369N is an integrated driver and MOSFET module designed for use in a synchronous buck converter topology. A single PWM input signal is all that is required to properly drive the high-side and low-side MOSFETs.

Low-Side Driver

The low-side driver is designed to drive a ground-referenced low $R_{DS(on)}$ N-Channel MOSFET. The voltage rail for the low-side driver is internally connected to VCIN and PGND.

High-Side Driver

The high-side driver is designed to drive a floating low $R_{DS(on)}$ N-channel MOSFET. The gate voltage for the high side driver is developed by a bootstrap circuit referenced to Switch Node (VSWH) pin.

The bootstrap circuit is comprised of the internal diode and an external bootstrap capacitor. When the NCP5369N is starting up, the VSWH pin is at ground, so the bootstrap capacitor is charged to PGND (High).

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Power Supply Decoupling

The NCP5369N can source and sink relatively large current to the gate pins of the MOSFETs. In order to maintain a constant and stable supply voltage (V_{CIN}) a low ESR capacitor should be placed near the power and ground pins. A $1\ \mu\text{F}$ to $4.7\ \mu\text{F}$ multi layer ceramic capacitor (MLCC) is usually sufficient.

Bootstrap Circuit

The bootstrap circuit uses a charge storage capacitor (C_{BST}) and the internal diode. The bootstrap capacitor must have a voltage rating that is able to withstand twice the maximum supply voltage. A minimum 50 V rating is recommended. A bootstrap capacitance greater than 100 nF and a minimum 50 V rating is recommended. A good quality ceramic capacitor should be used.

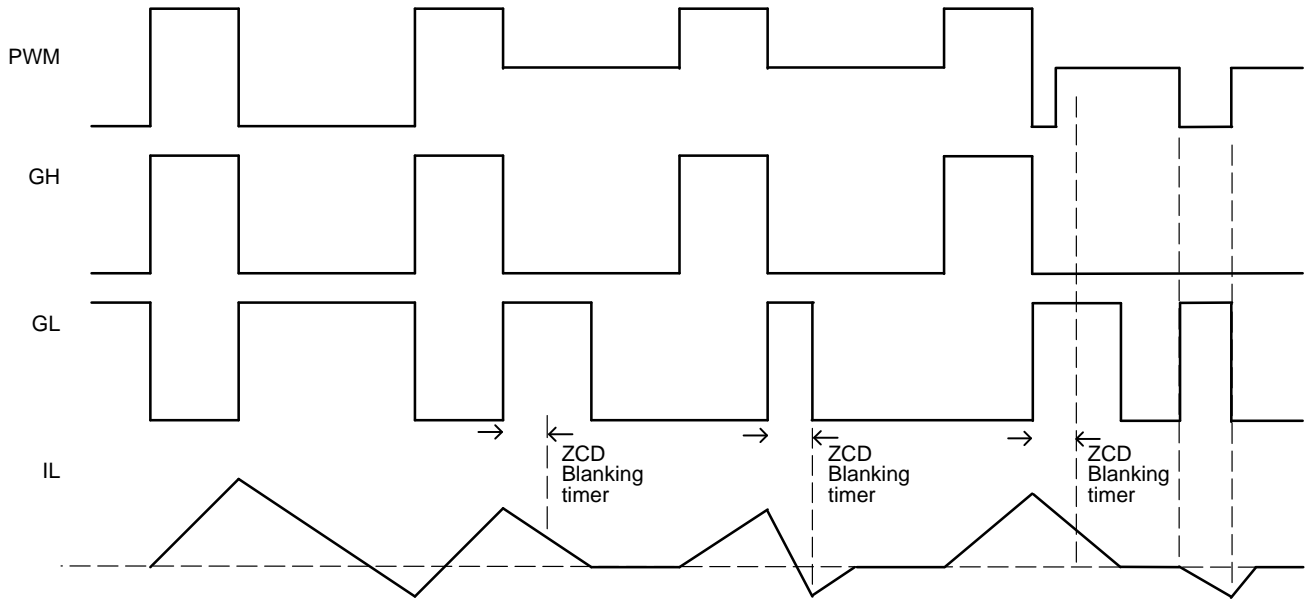


Figure 4. Zero Current Detection

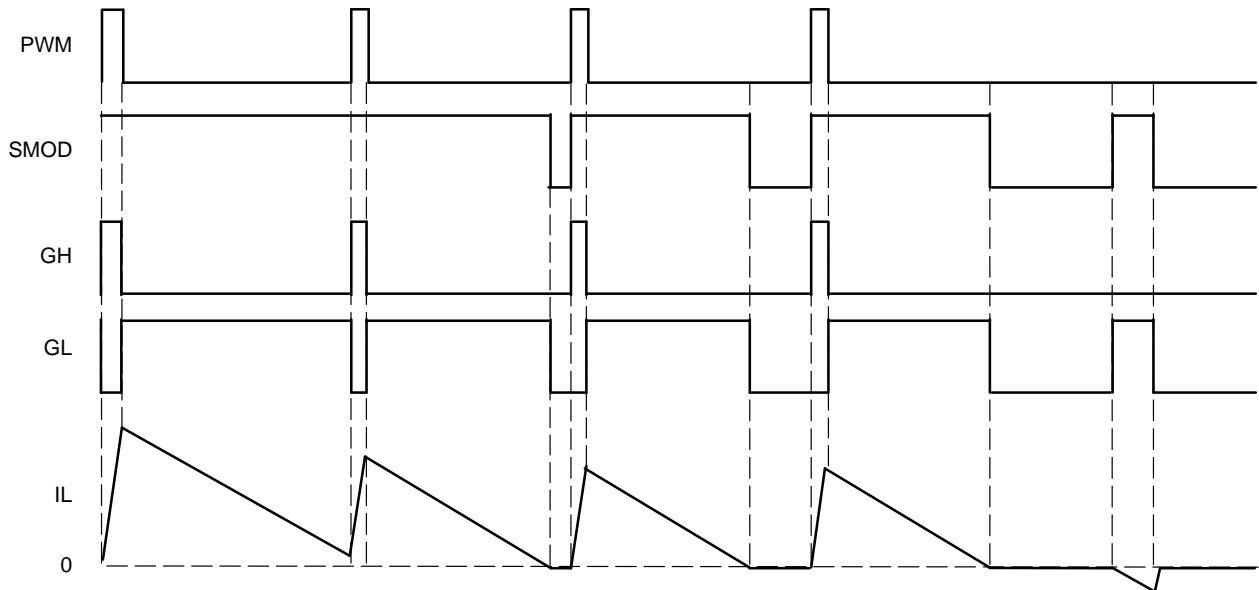
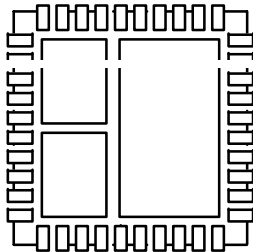
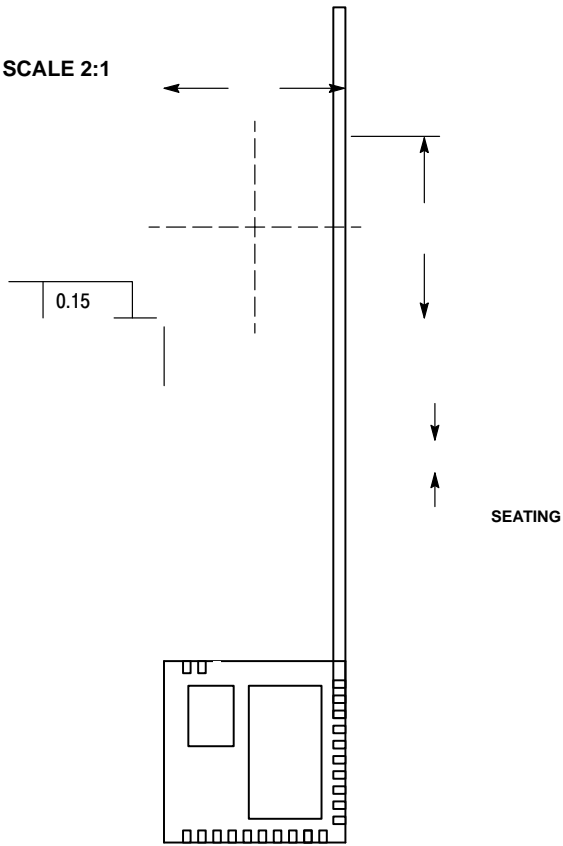


Figure 5. SMOD Control

QFN40 6x6, 0.5P
CASE 485AZ
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