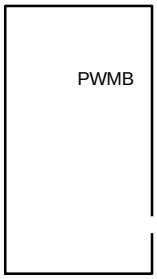
TYPICAL APPLICATION CIRCUIT



FUNCTIONAL TABLE

INPUT					UVLO			GATE DRIVE OUTPUT	
ENA/DIS (Note 3)						Output Side			
ENABLE	**DISABLE**	**ANB**	**INA**	**INB**	**Input Side (V_{DD})**	**Channel A (V_{CCA})**	**Channel B (V_{CCB})**	**OUTA**	**OUTB**
X	X	X	X	X	Active	X	X	L	L
X	X	X	X	X	X	Active	Active	L	L
H	L								

PIN CONNECTIONS

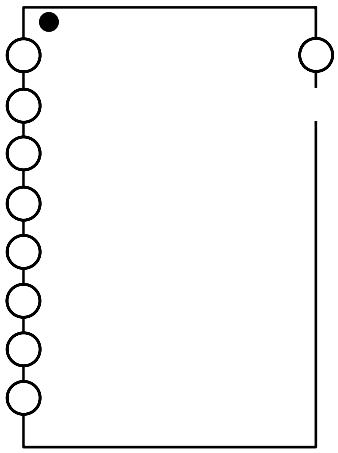


Figure 3. Pin Connections − SOIC−16 WB (Top View)

SAFETY AND INSULATION RATINGS

Symbol	Parameter		Min	Typ	Max	Unit
	Installation Classifications per DIN VDE 0110/1.89 Table 1 Rated Mains Voltage	<150 V_{RMS}	−	I−IV	−	
		<300 V_{RMS}	−	I−IV	−	
		<450 V_{RMS}	−			

	ax	Unit
	3	mW
	12	
	00	
	0	°C

		Unit
		V
		V
	0.3, 0.3	V
	0.3, 0.3	V
		V
		V
		V
		V
	0.3	

RECOMMENDED OPERATING CONDITIONS

Symbol	Rating		Min	Max	Unit
V_{DD}	Power Supply Voltage – Input Side		3.0	5.0	V
V_{CCA}, V_{CCB}	Power Supply Voltage – Driver Side	5−V UVLO Version	6.5	30	V
		8−V UVLO Version	9.5	30	V
		13−V UVLO Version	14.5	30	V
		17−V UVLO Version	18.5	30	V
V_{IN}	Logic Input Voltage at Pins INA, INB, and ANB		0	18	V
$V_{ENA/DIS}$	Logic Input Voltage at Pin ENA/DIS		0	5.0	V
T_A	Ambient Temperature		−40	+125	°C
T_J	Junction Temperature		−40	+125	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

THERMAL CHARACTERISTICS

Symbol	Rating	Condition	Value	Unit
$R_{\theta JA}$	*Thermal* , (Note 13) Thermal Resistance Junction−Air 16−SOIC−WB	100 mm^2, 1 oz Copper, 1 Surface Layer (1S0P)	120	°C/W
		100 mm^2, 2 oz Copper, 1 Surface Layer (1S0P)	81	
R_{qJC}	Thermal Resistance Junction−case	100 mm^2, 1 oz Copper, 1 Surface Layer (1S0P)	38	°C/W
ψ_{JT}	Thermal Resistance Junction−to−top		18	°C/W
ψ_{JB}	Thermal Resistance Junction−to−board		55	°C/W
P_D	*Power Dissipation* (Note 13) 16−SOIC−WB	100 mm^2, 1 oz Copper, 1 Surface Layer (1S0P)	0.8	W
		100 mm^2, 2 oz Copper, 1 Surface Layer (1S0P)	1.5	

12. ReferTING RANGES and/or APPLICATION INFORMATION for Safe Operating parameters.
13. JEDEC standard: JESD51−2, and JESD51−3.

ISOLATION CHARACTERISTICS

Symbol	Parameter	Condition	Min	Typ	Max	Unit
$V_{ISO,INPUT}$ TO OUTPUT	Inputoltage	T_A = 25°C, Relative Humidity < 50%, t = 1.0 minute, I_{I-O} 10 (Note 14, 15, 16)	5000	−	−	V_{RMS}
$V_{ISO,OUTA}$ TO OUTB	OUTAoltage	Impulse Test > 10 ms (Note 14, 15)	1850	−	−	V_{DC}
R_{ISO}	Isolation Resistance	V_{I_O} = 500 V (Note 14)	10^{11}	−	−	Ω

14. Devsce i considered a two−terminal device: pins 1 to 8 are shorted together and pins 9 to 16 are shorted together for input to output isolation test, and pins 9 to 11 are shorted together and pins 14 to 16 are shorted together for between channel isolation test.
15. 5,000 V_{RMS} for 1−minute duration is equivalent to 6,000 V_{RMS} for 1−second duration for input to output isolation test, and Impulse Test > 10 ms; sample tested for between channel isolation test.
16. The input−s0258pm(mf.5768 0 TD-9.(V4est, and pins)(9lr)4.3(Safe)]TJn9D.j6.5 0 ( )Tjlevplesafety specific 0 TD0)ÐIN VDETm08841.1055 TD-0079.441est, a

ELECTRICAL CHARACTERISTICS (V_{DD} = 5 V, V_{CCA} = V_{CCB} = 12 V, or 20 V (Note 18) and VSSA

DYNAMIC ELECTRICAL CHARACTERISTICS (V_{DD} = 5 V, V_{CCA} = V_{CCB} = 12 V, or 20 V (Note 21) and VSSA = VSSB, for typical values T_J = T_A = 25°C, for min/max values T_J = −40°C to +125°C, unless otherwise specified. (Note 20))

Symbol	Parameter	Condition	Min	Typ	Max	Unit
t_{PDON}	Turn−					

TYPICAL CHARACTERISTICS

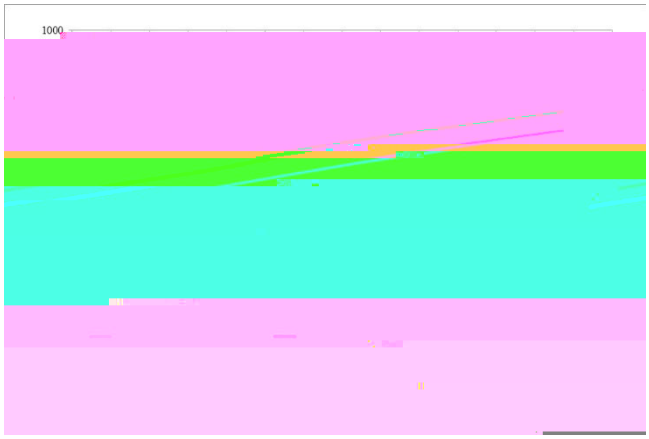


Figure 6. Quiescent V_{DD} Supply Current vs. Temperature (V_{DD} = 5 V, INA = INB = 0 V, ENA/DIS = 5 V or , INA = INB = 5 V, ENA/DIS = 0 V and No Load)

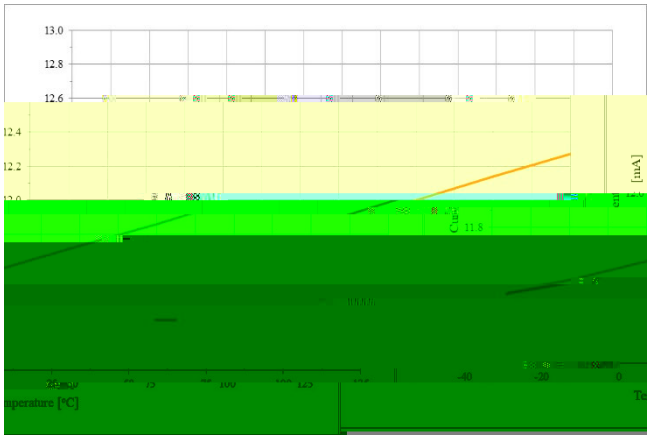


Figure 7. Quiescent V_{DD} Supply Current vs. Temperature (V_{DD} = 5 V, INA = INB = ENA/DIS = 5 V and No Load)

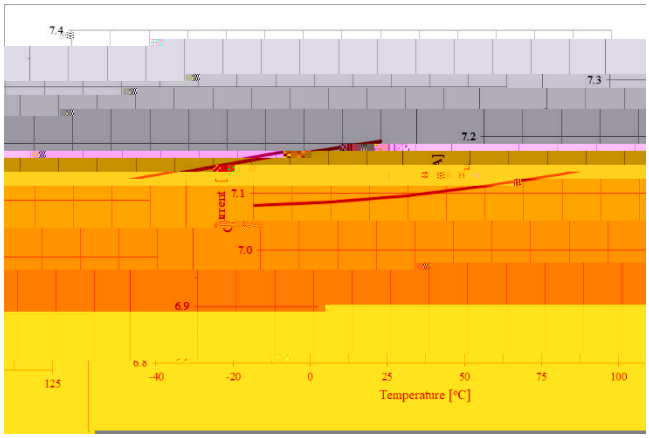


Figure 8. V_{DD} Operating Current vs. Temperature (V_{DD} = 5 V, No Load, and Switching Frequency = 500 kHz)

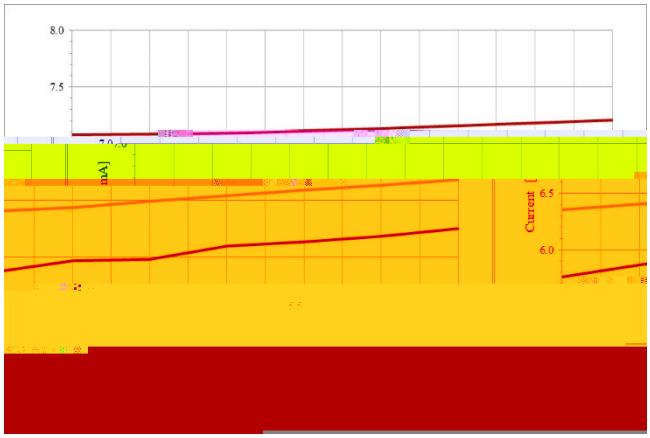


Figure 9. V_{DD} Operating Current vs. Temperature (V_{DD} = 5 V, No Load, and Different Switching Frequency)

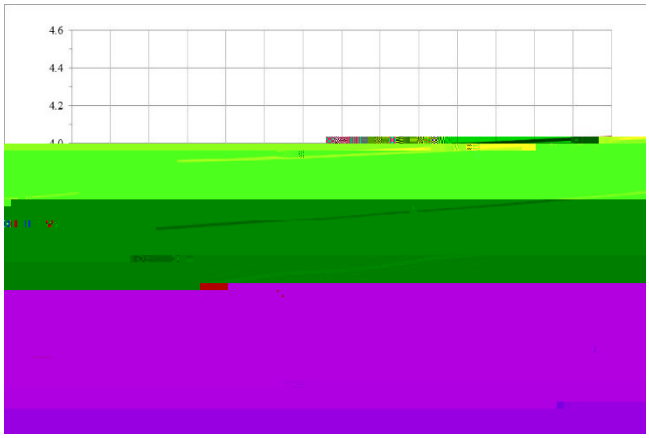


Figure 10. Per Channel V_{DD} Operating Current vs. Temperature (V_{DD} = 5 V, No Load, and Different Switching Frequency

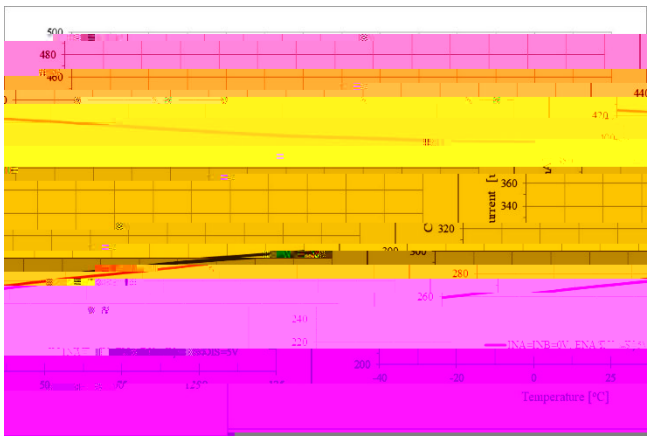


Figure 11. Per Channel Quiescent V_{CC} Supply Current vs. Temperature (INA = INB = 0 V or 5 V, ENA/DIS = 5 V and No Load)

TYPICAL CHARACTERISTICS (CONTINUED)

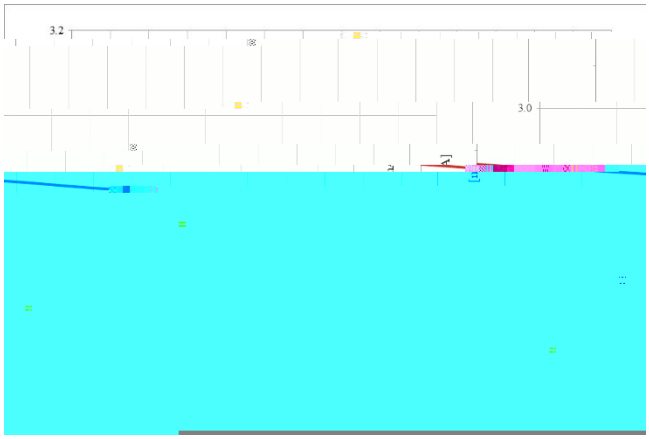


Figure 12. Per Channel V_{CC} Operating Current vs. Temperature (No Load and Switching Frequency = 500 kHz

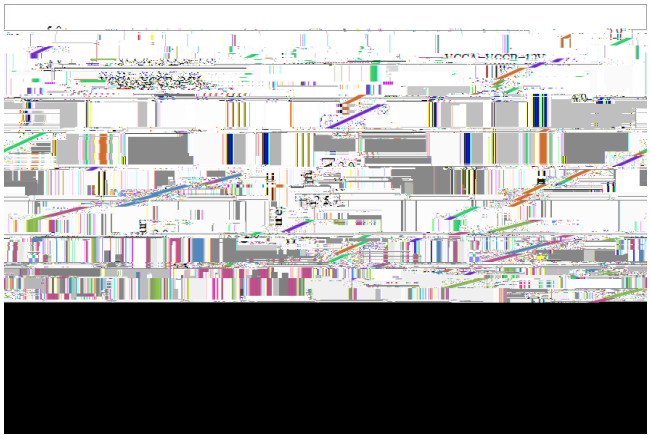


Figure 13. Per Channel Operating Current vs. Frequency (No Load, V_{CCA} = V_{CCB} = 12 V, or 25 V)

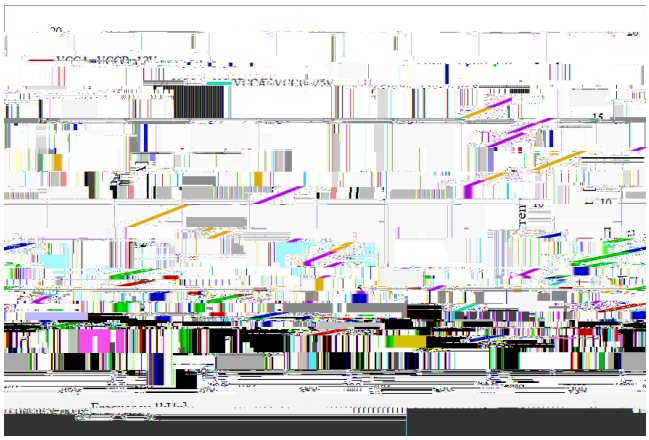


Figure 14. Per Channel Operating Current vs. Frequency (C_{LOAD} = 1 nF, V_{CCA} = V_{CCB} = 12 V, or 25 V)

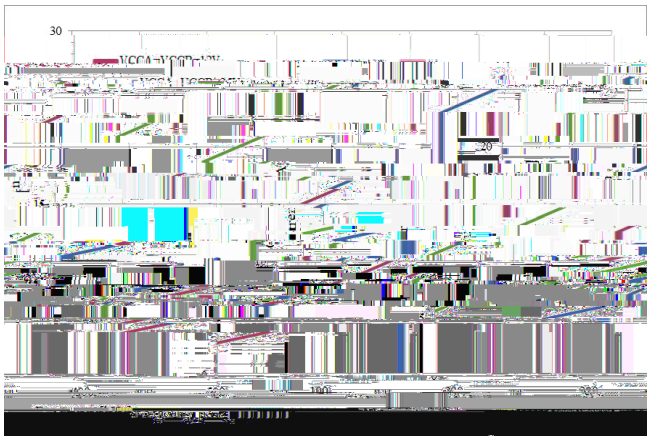


Figure 15. Per Channel Operating Current vs. Frequency (C_{LOAD} = 1.8 nF, V_{CCA} = V_{CCB} = 12 V, or 25 V)

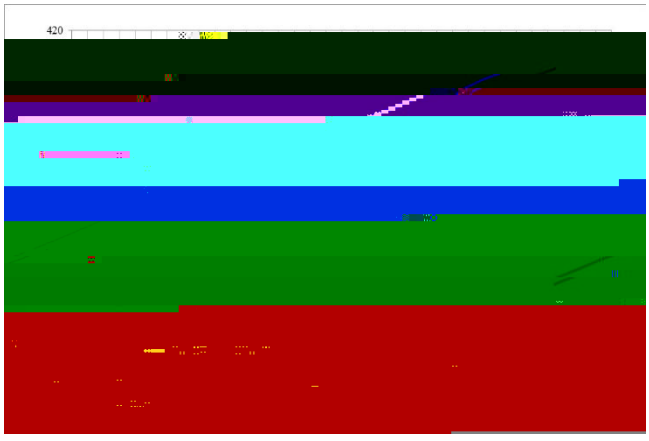


Figure 16. Per Channel V_{CC} Quiescent Current vs. V_{CC} Supply Voltage (INA = INB = 0 V, ENA = 5 V)

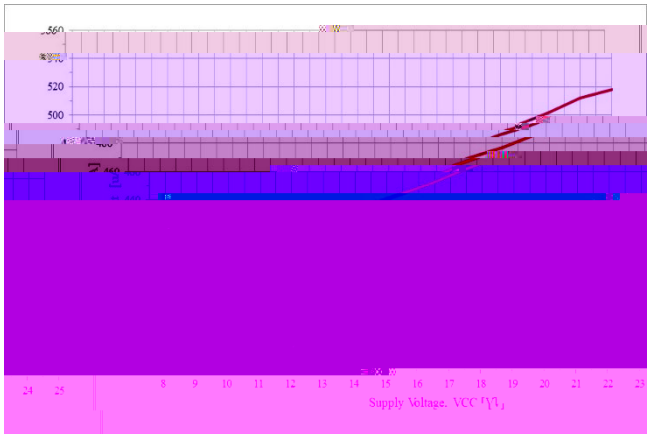
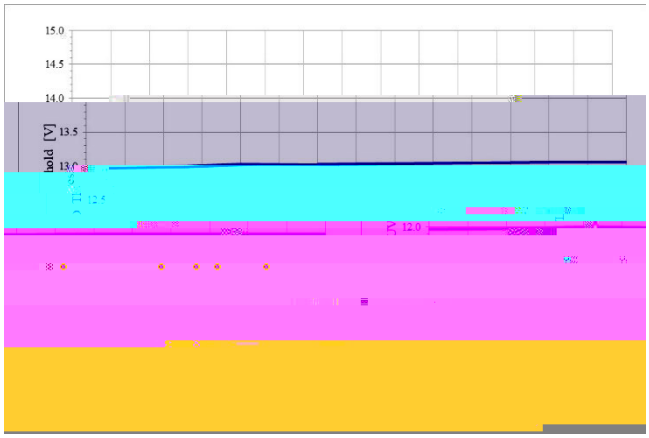
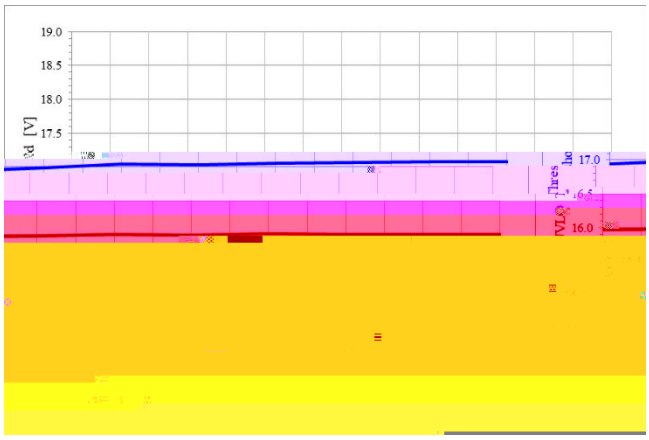
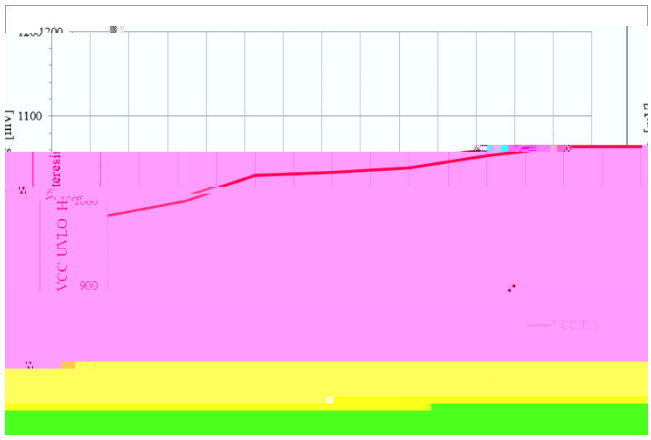


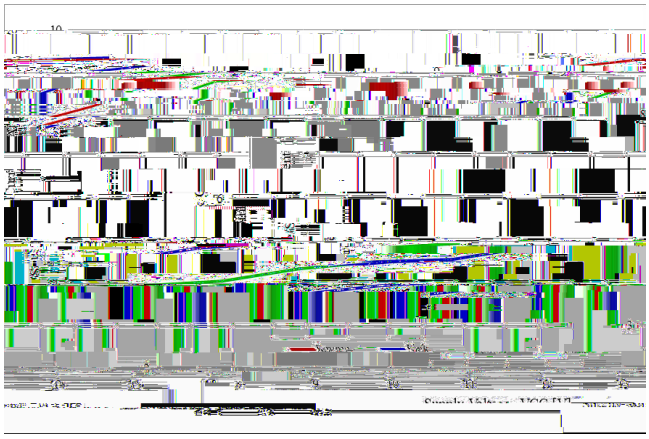
Figure 17. Per Channel V_{CC} Quiescent Current vs. V_{CC} Supply Voltage (INA = INB = 5 V, ENA = 5 V)

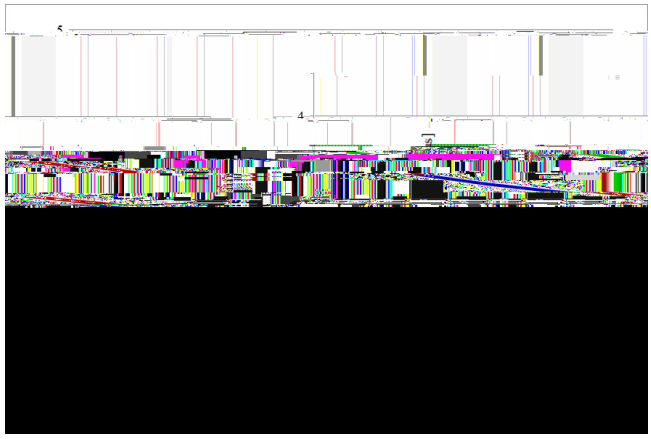
TYPICAL CHARACTERISTICS (CONTINUED)











TYPICAL CHARACTERISTICS (CONTINUED)

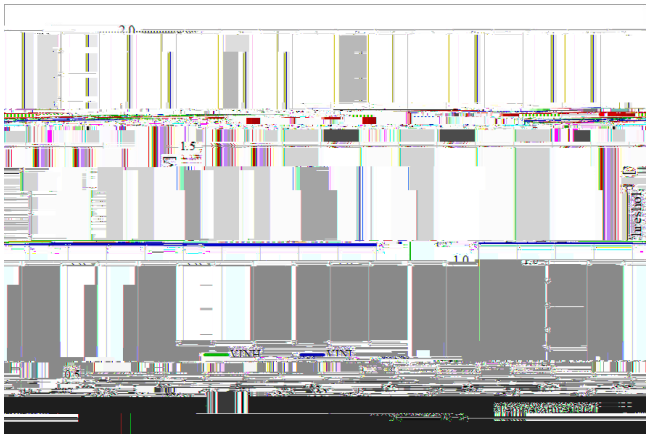


Figure 30. Input Logic Threshold vs. Temperature (INA, INB, and ANB)

Figure 31. Input Logic Hysteresis vs. Temperature (INA, INB, and ANB)

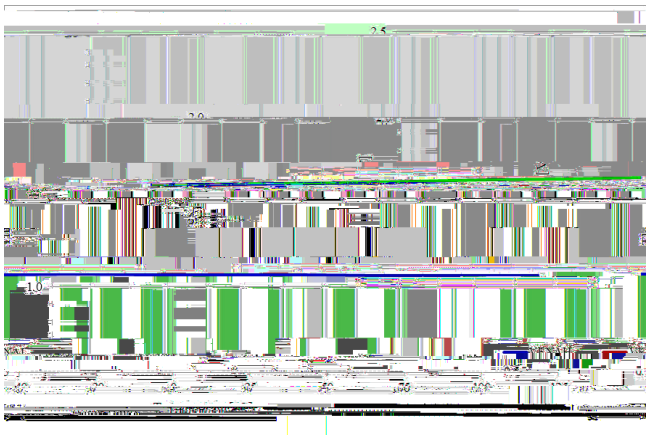


Figure 32. ENA/DIS Threshold vs. Temperature (ENABLE, and DISABLE)

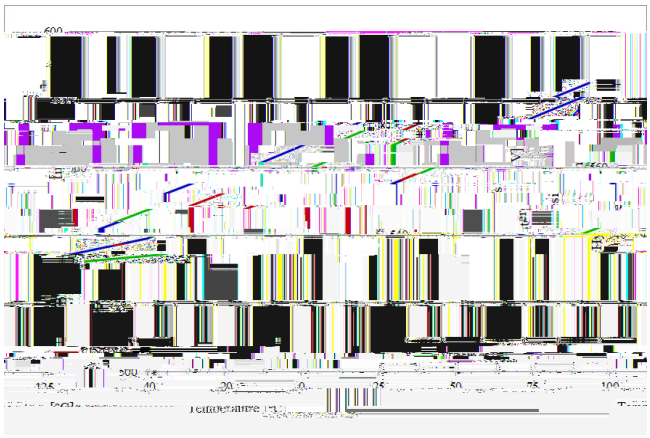


Figure 33. ENA/DIS Hysteresis vs. Temperature (ENABLE, and DISABLE)

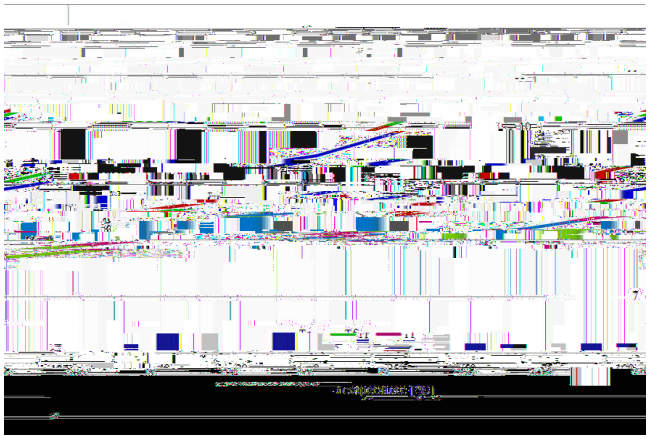


Figure 34. Rise/Fall Time vs. Temperature (C_{LOAD} = 1.8 nF)

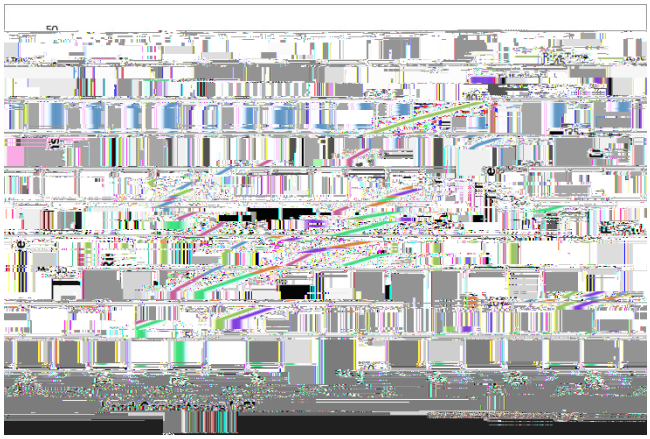


Figure 35. Rise/Fall Time vs. Temperature (V_{CCA} = V_{CCB} = 12 V, and Different Load)

TYPICAL CHARACTERISTICS (CONTINUED)

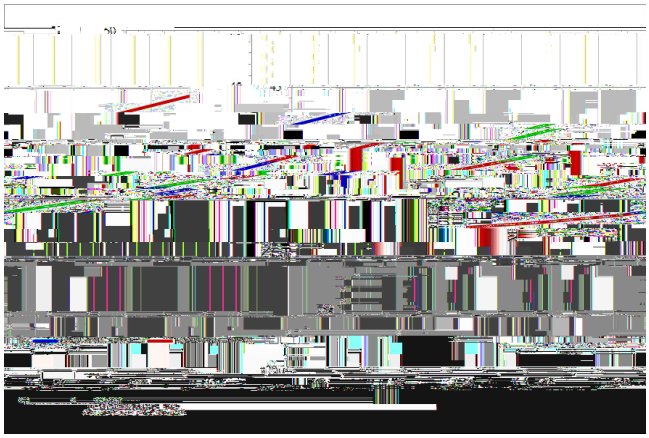


Figure 36. ENA/DIS Delay Time vs. Temperature

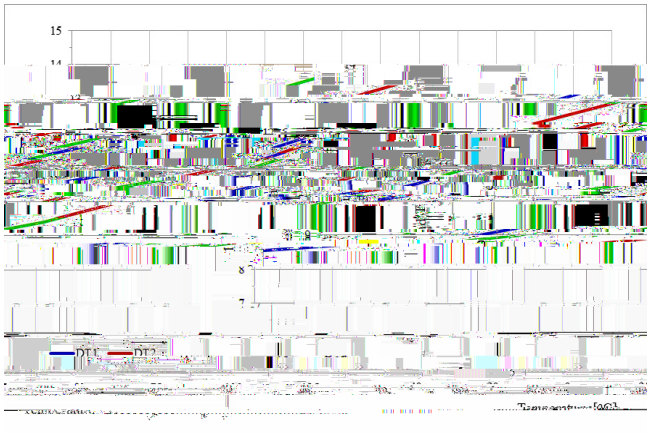


Figure 37. Dead Time vs. Temperature (R_{DT} = Open)

Figure 38. Dead Time vs. Temperature (R_{DT} = 20 kΩ)

Figure 39. Dead Time vs. Temperature (R_{DT} = 100 kΩ)

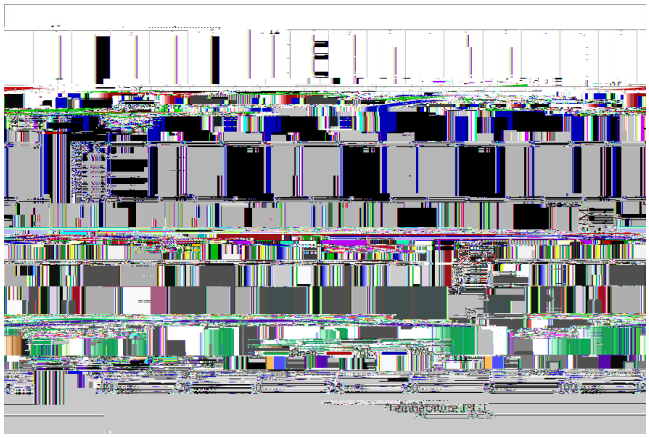


Figure 40. Dead Time Mismatching vs. Temperature

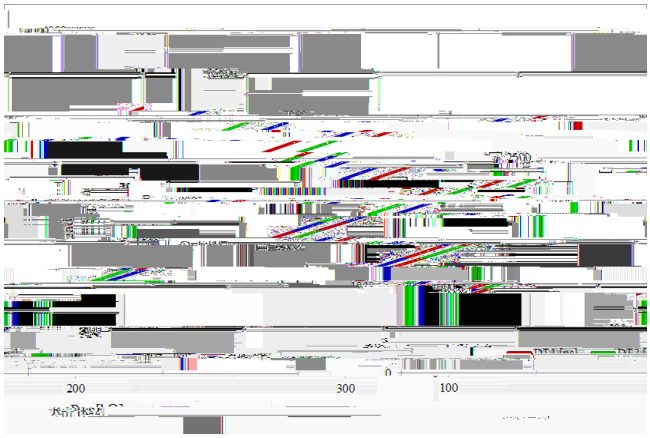


Figure 41. Dead Time vs. R_{DT}

TYPICAL CHARACTERISTICS (CONTINUED)

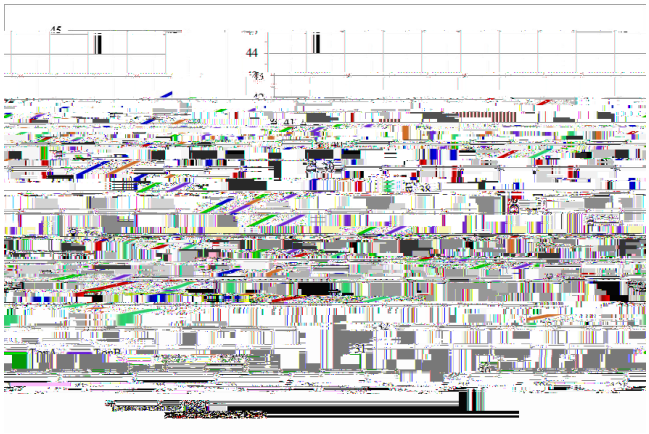


Figure 42. Turn−on Propagation Delay vs. Temperature

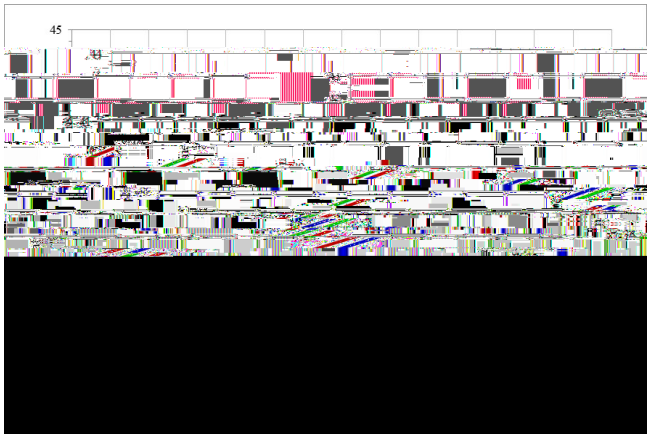
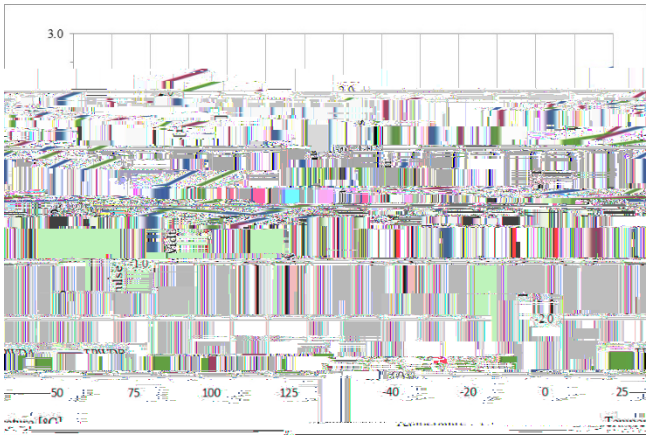
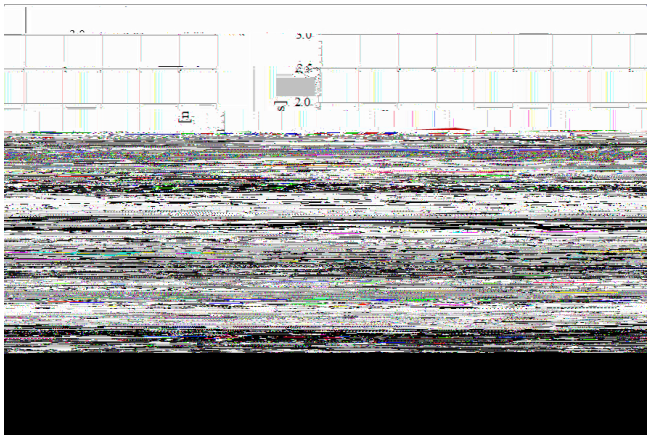


Figure 43. Turn−off Propagation Delay vs. Temperature





Programmable Dead−Time

Dead time is automatically inserted whenever the dead time of the external two input signals (between INA and INB signals) is shorter than internal setting dead times (DT1 and DT2). Otherwise, if the external input signal dead times are larger than internal dead− time, the dead time is not modified by the gate driver and internal dead−time definition as shown in Figure 50.

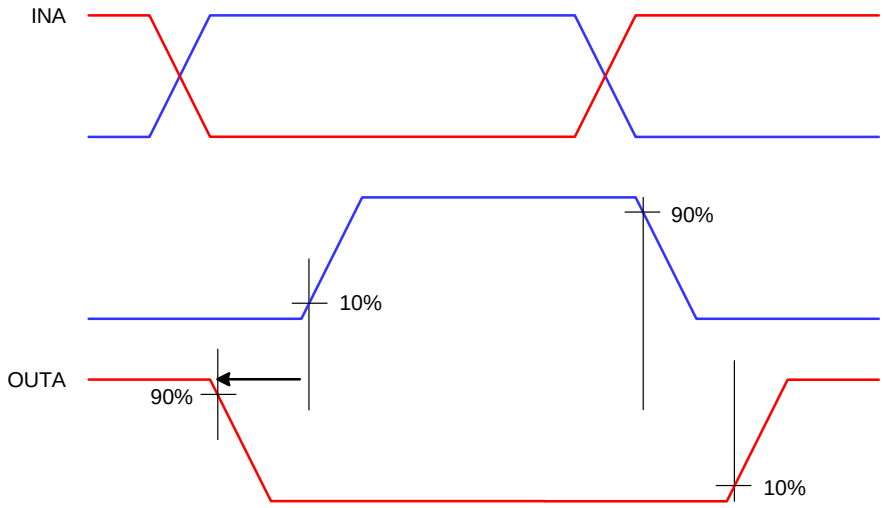


Figure 50. Internal Dead−Time Definitions

Input to Output Operation Definitions

The NCP51563 provides important protection functions such as independent under−voltage lockout for both gate driver; enable or disable function and dead−time control function. Figure 52 shows an overall input to output timing diagram when shutdown mode via ENA/DIS pin in the *CASE−A*, and Under−Voltage Lockout protection on the primary− and secondary−sides power supplies events in the *CASE−B*. The gate driver output (OUTA and OUTB) were turn−off when cross−conduction event at the dead time control mode in the *CASE−C*.

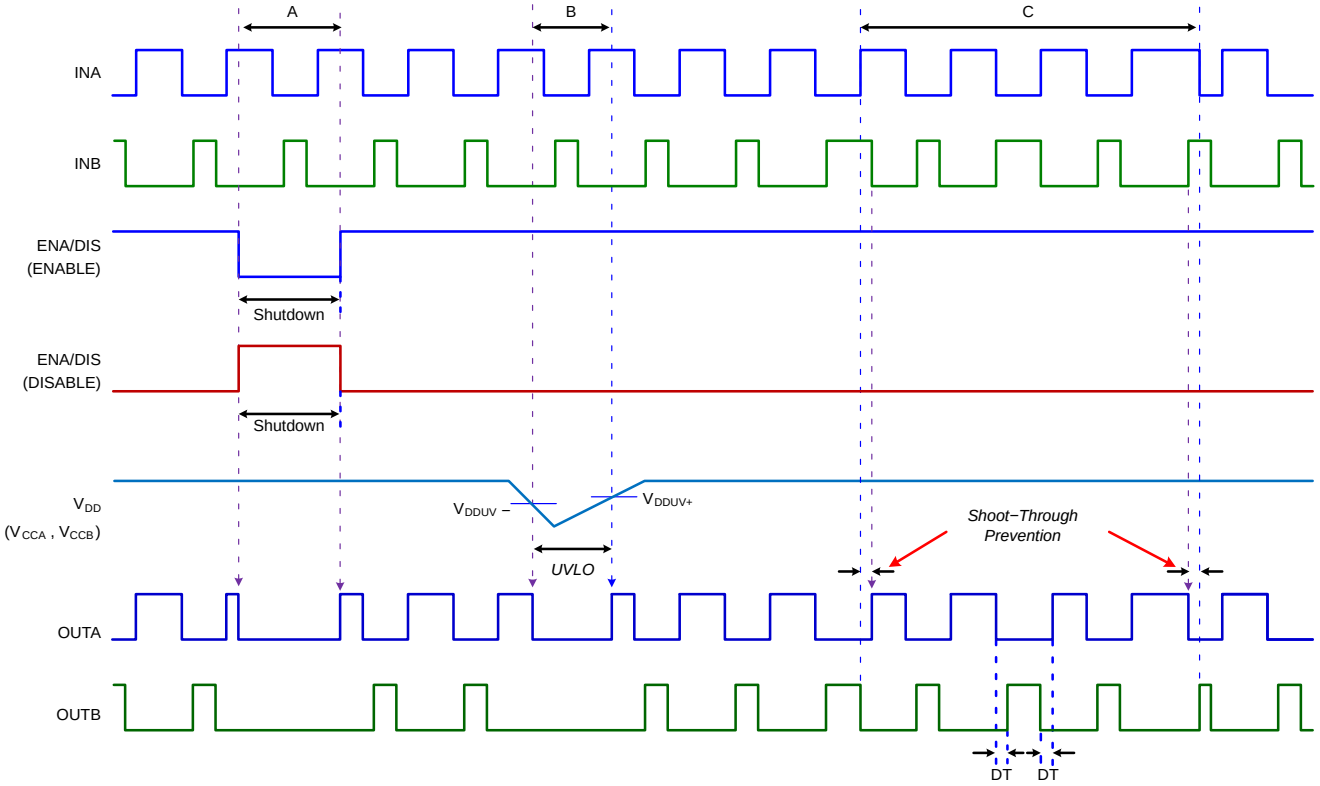


Figure 52. Overall Operating Waveforms Definitions at the Dead−Time Control Mode

Input and Output Logic Table

Table 1 shows an input to output logic table according to the dead time control modes and an enable or disable operation mode.

Table 1. INPUT AND OUTPUT LOGIC TABLE

INPUT				OUTPUT		
		ENA/DIS				
INA	INB	ENABLE	DISABLE	OUTA	OUTB	NOTE
L	L	H or Left open	L or Left open	L	L	Programmable dead time control with R_{DT}.
L	H	H or Left open	L or Left open	L	H	
H	L	H or Left open	L or Left open	H	L	
H	H	H or Left open	L or Left open	L	L	DT pin is left open Or programmed with R_{DT}.
H	H	H or Left open	L or Left open	H	H	DT pin pulled to V_{DD}.
Left open	Left open	H or Left open	L or Left open	L	L	
X	X	L	H	L	L	

23. “X” means L, H or left open.

Input Signal Configuration

The NCP51563 allows to set the input signal configuration through the ANB pin for user convenience. There are four operating modes that allow to change the configuration of the input to output channels (e.g. single input – dual output, or dual input – dual output), and select the shutdown function (e.g. Disable or Enable mod below Table 2. Unused input pins (e.g. INA, INB, and AI should be tied to GND to achieve better noise immun In addition, the ANB pin has an internal filter ti typically 3.3μs to achieve the noise immunity.

Table 2. INPUT SIGNAL CONFIGURATION LOGIC TABLE

Mode	
1	

Figure 53 shows an operating timing chart of input to output and shutdown function according to the ANB and ENA/DIS pins setting. The ENA/DIS and ANB pins are only functional when V_{DD} stays above the specified UVLO threshold. It is recommended to tie these pins to Ground if the ENA/DIS and ANB pins are not used to achieve better noise immunity, and it is recommended to bypass using a 1 nF low ESR/ESL capacitor close to these pins for the DISABLE (e.g. NCP51563xB) mode.

When it is not possible to connect ANB to GND t external pulli

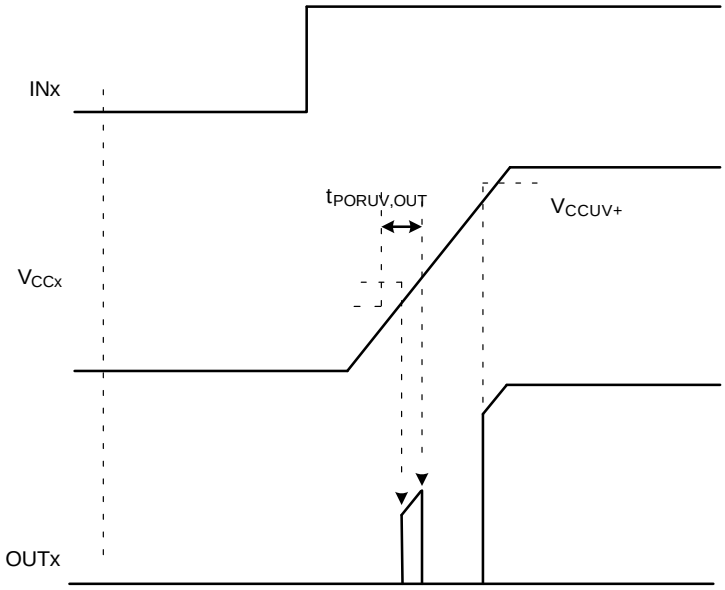
PROTECTION FUNCTION

The NCP51563 provides the protection features include enable or disable function, Cross Conduction Protection, and Under−Voltage Lockout (UVLO) of power supplies on primary−side (V_{DD}), and secondary−

V_{CCX} Power−Up and IN_X Signal

To provide a variety of Under−Voltage Lockout (UVLO) thresholds NCP51563 has a power−up delay time during initial V_{CCX} start−up or after POR event.

In case IN_X pins are active when V_{CCX} is above 4.7 V, outputs would occur until settling time has elapsed as shown in Figure 55 (A). If IN_X are only active after settling time has expired, outputs won't be active until V_{CCX} cross NCP51561 specific V_{CCUV+} as shown in Figure 55 (B).



A. Power up with PWM signals during Preset

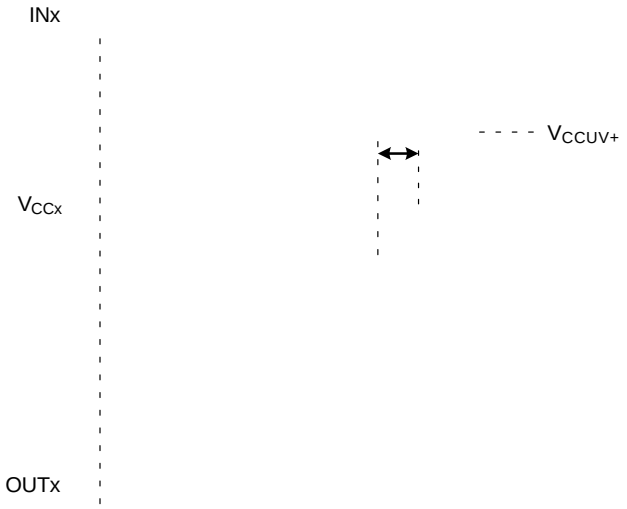


Figure 55. V_{CCX} Power−up

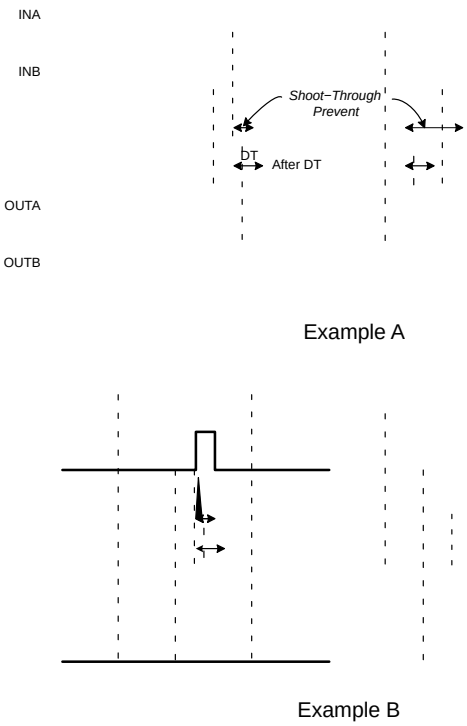


Figure 56. Concept of Shoot−Through Prevention

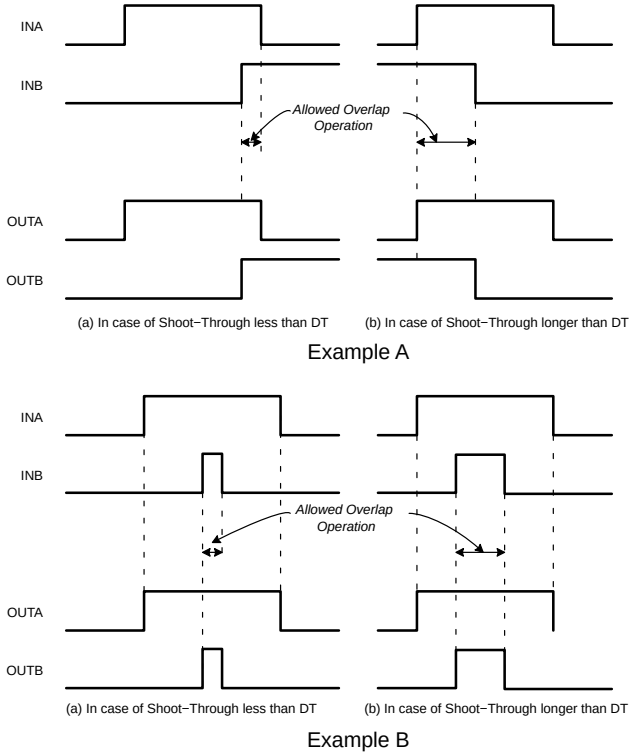


Figure 57. Concept of Allowed the Shoot−Through

Common Mode Transient Immunity Testing

Figure 59 is a simplified diagram of the Common Mode Transient Immunity (CMTI) testing configuration.

CMTI is the maximum sustainable common−mode voltage slew rate while maintaining the correct output.

CMTI applies to both rising and falling common−mode voltage edges. CMTI is tested with the transient generator connected between GND and V_{SSA} and V_{SSB}. (V_{CM} = 1500 V).

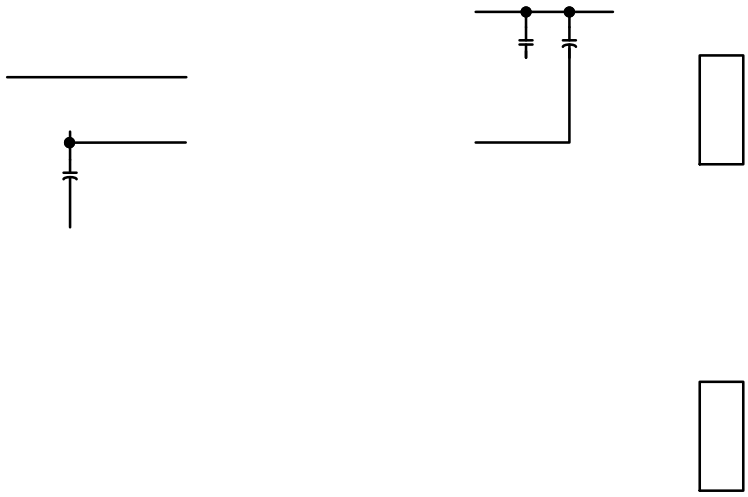


Figure 59. Common Mode Transient Immunity Test Circuit

APPLICATION INFORMATION

This section provides application guidelines when using the NCP51563.

Power Supply Recommendations

It is important to remember that during the Turn−On of switch the output current to the gate is drawn from the V_{CCA} and V_{CCB} supply pins. The V_{CCA} and V_{CCB} pins should be bypassed with a capacitor with a value of at least ten times the gate capacitance, and no less than 100 nF and located as close to the device as possible for the purpose of decoupling. A low ESR, ceramic surface mount capacitor is necessary. We recommend using 2 capacitors; a 100 nF ceramic surface−mount capacitor which can be very close to the pins of the device, and another surface−mount capacitor of few microfarads added in parallel.

In addition, it is recommended to provide various V_{CCX} Under−Voltage Lockout voltage options (e.g. 8−V, or 13−V), the V_{CCX} rising time from 5−V to 6−V should be at least 16 μs or above at initial start−up.

Input Stage

The input signal pins (INA, INB, ANB, and ENA/DIS) of the NCP51563 are based on the TTL compatible input−threshold logic that is independent of the V_{DD} supply voltage. The logic level compatible input provides a typically high and low threshold of 1.6 V and 1.1 V respectively. The input signal pins impedance of the NCP51563 is 200 kΩ typically and the INA, INB, and ANB pins are pulled to GND pin and ENA/DIS pin is pulled to V_{DD} pin for an ENABLE version as shown in Figure 60.

Consideration of Driving Current Capability

Peak source and sink currents (I_{SOURCE}, and I_{SINK}) capability should be larger than average current ($I_{G, AV}$) as shown in Figure 62.

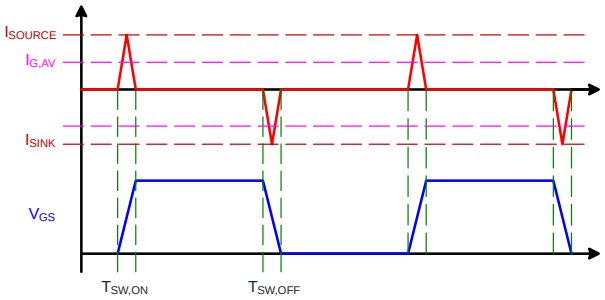


Figure 62. Definition of Current Driving Capability

The approximate maximum gate charge Q_G that can be switched in the indicated time for each driver current rating may be calculate: Needed driver current ratings depend on what gate charge Q_G must be moved in what switching time $t_{SW-ON/OFF}$ because average gate current during switching is I_G.

$$I_{G.AV} = \frac{Q_G}{t_{SW,ON/OFF}} \quad \text{(eq. 1)}$$

The approximate gate driver source and sink peak currents can be calculated as below equations.

At turn−on (Sourcing current)

$$I_{SOURCE} \geq 1.5 \times \frac{Q_G}{t_{SW,ON}} \quad \text{(eq. 2)}$$

At turn−off (Sinking current)

$$I_{SINK} \geq 1.5 \times \frac{Q_G}{t_{SW,OFF}} \quad \text{(eq. 3)}$$

where, Q_G = Gate charge at $V_{GS} = V_{CC}$
$t_{SW, ON/OFF}$ = Switch On / Off time
1.5 = empirically determined factor
(Influenced by $I_{G,AV}$ vs. I_{DRV}, and circuit parasitic)

Consideration of Gate Resistor

The gate resistor is also sized to reduce ringing voltage by parasitic inductances and capacitances. However, it limits the current capability of the gate driver output. The limited current capability value induced by turn−on and off gate resistors can be obtained with below equation.

$$I_{SOURCE} = \frac{V_{CC} - V_{OH}}{R_{G,ON}}$$

$$I_{SINK} = \frac{V_{CC} - V_{OL}}{R_{G,OFF}} \quad \text{(eq. 4)}$$

where:
I_{SOURCE}: Source peak current
I_{SINK}: Sink peak current.
V_{OH}: High level output voltage drop
V_{OL}: Low level output voltage drop

Application Circuits with Output Stage Negative Bias

SiC MOSFET unique operating characteristics need to be carefully considered to fully benefits from SiC characteristics. The gate driver needs to be capable of providing +20 V and −2 V to −5 V negative bias with minimum output impedance and high current capability.

When parasitic inductances are introduced by non−ideal PCB layout and long package leads (e.g. TO−220 and TO−247 type packages), there could be ringing in the gate−source drive voltage of the power transistor during high di/dt and dv/dt switching. If the ringing is over the threshold voltage, there is the risk of unintended turn−on and even shoot−through. Applying a negative bias on the gate drive is a popular way to keep such ringing below the threshold. Negative voltage can improve the noise tolerance of SiC MOSFET to suppress turning it unintentionally. The negative gate−source voltage makes the capacitance of Cgd becoming lower, which can reduce the ringing voltage.

Below are a few examples of implementing negative gate drive bias. The first example with negative bias with two isolated−bias power supplies as shown in Figure 63.

Power supply VHx determines the positive drive output voltage and VLx determines the negative turn−off voltage for each channels. This solution requires more power supplies than the conventional bootstrapped power supply example; however, it provides more flexibility when setting the positive, VHx, and negative, VLx, rail voltages.

Figure 63. Negative Bias with Two Isolated−Bias Power Supplies

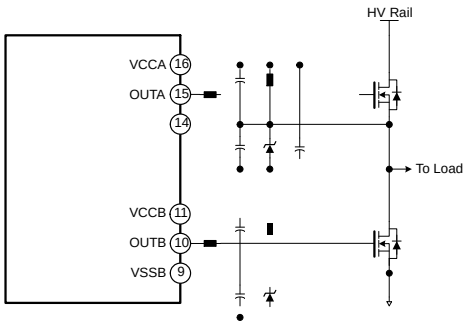


Figure 64. Negative Bias with Zener Diode on Single Isolated−Bias Power Supply

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