USB Positive Overvoltage Protection Controller with Internal PMOS FET and Overcurrent Protection

The NCP361 disconnects systems at its output when wrong VBUS operating conditions are detected at its input. The system is positive over−voltage protected up to +20 V.

Thanks to an integrated PMOS FET, no external device is necessary, reducing the system cost and the PCB area of the application board.

The NCP361 is able to instantaneously disconnect the output from the input if the input voltage exceeds the overvoltage threshold (5.675 V). Thanks to an overcurrent protection, the integrated PMOS is turning off when the charge current exceeds current limit (see options in ordering information).

The NCP361 provides a negative going flag ($\overline{\text{FLAG}}$) output, which alerts the system that voltage, current or overtemperature faults have occurred.

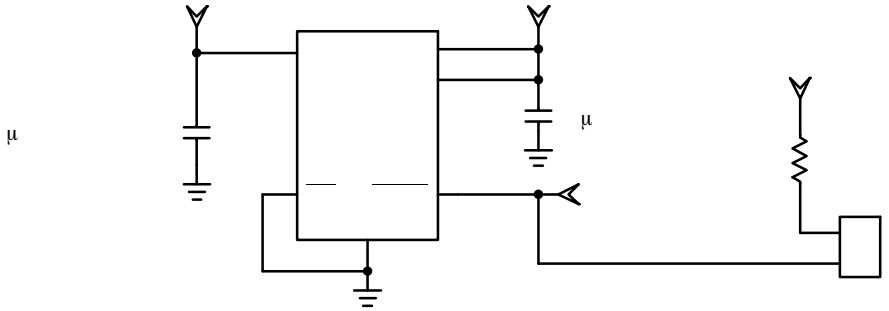

Figure 1. Typical Application Circuit (UDFN Pinout)

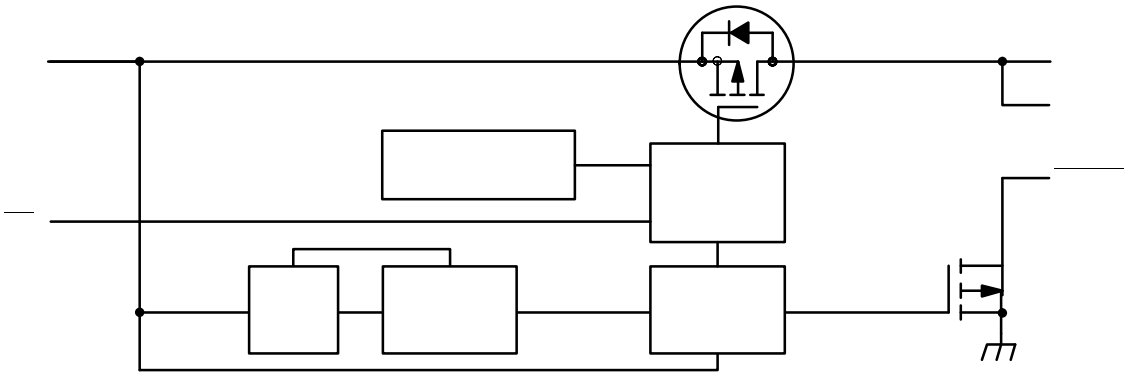

Figure 2. Functional Block Diagram

PIN FUNCTION DESCRIPTION (UDFN Package)

Pin No.	Name	Type	Description

PIN FUNCTION DESCRIPTION (TSOP

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
		–	
		–	
– – –	θ		°
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		–	°
			°

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ELECTRICAL CHARACTERISTICS

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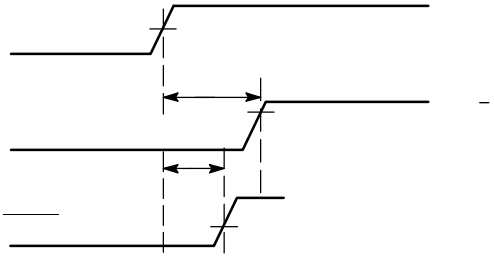


Figure 3. Start Up Sequence

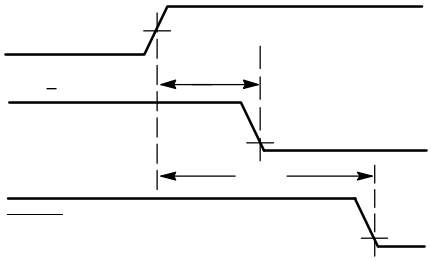


Figure 4. Shutdown on Over Voltage Detection

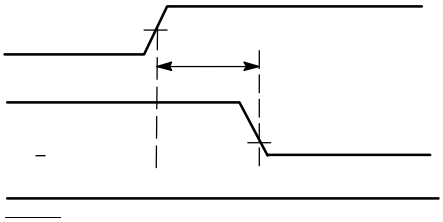


Figure 5. Disable on $\overline{EN}$ = 1

Figure 6. $\overline{FLAG}$ Response with $\overline{EN}$ = 1

Figure 9. Start Up. Vin=Ch1, Vout=Ch2

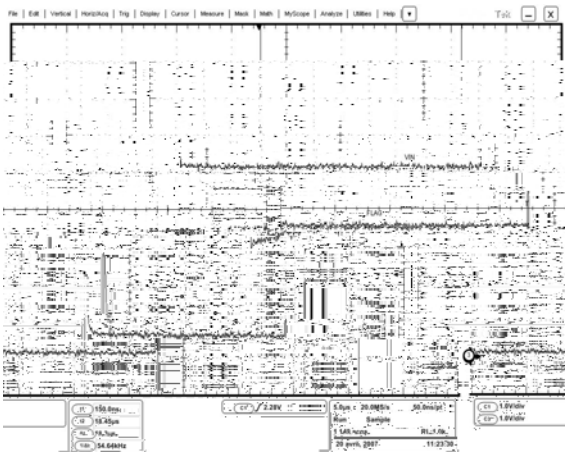


Figure 10. FLAG Going Up Delay. Vin=Ch1, FL:AG=Ch3

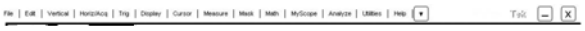


Figure 11. Output Turn Off time. Vin=Ch1, Vout=Ch2

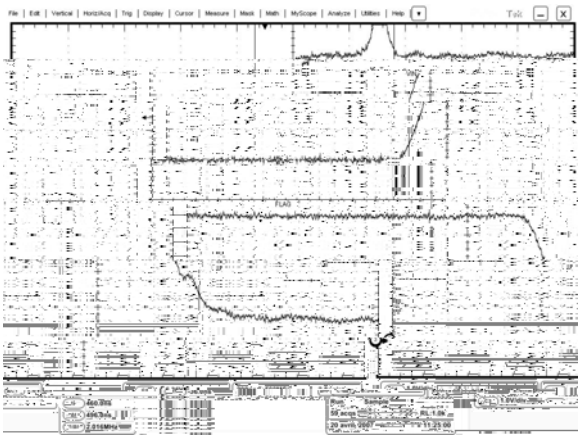


Figure 12. Alert Delay. Vout=Ch1, FLAG=Ch3

Figure 13. Disable Time. EN=Ch4, Vin=Ch1, Vout=Ch2

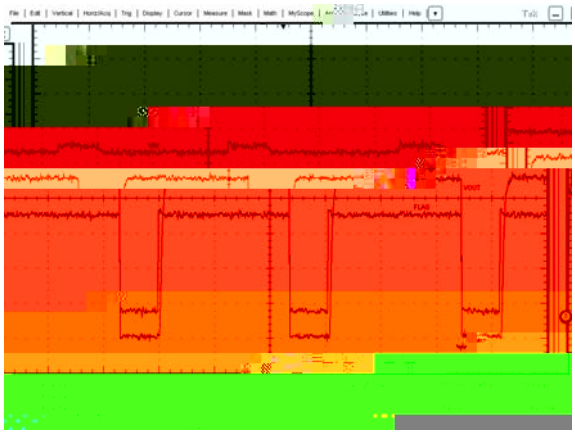


Figure 14. Thermal Shutdown. Vin=Ch1, Vout=Ch2, FLAG=Ch3

Operation

NCP361 provides overvoltage protection for positive voltage, up to 20 V. A PMOS FET protects the systems (i.e.: VBUS) connected on the V_{out} pin, against positive overvoltage. The Output follows the VBUS level until OVLO threshold is overtaken.

Undervoltage Lockout (UVLO)

To ensure proper operation under any conditions, the device has a built−in undervoltage lock out (UVLO) circuit. During V_{in} positive going slope, the output remains disconnected from input until V_{in} voltage is above 3.0 V nominal. The $\overline{FLAGV}$ output is pulled to low as long as V_{in} does not reach UVLO threshold. This circuit has a 70 mV hysteresis to provide noise immunity to transient condition.

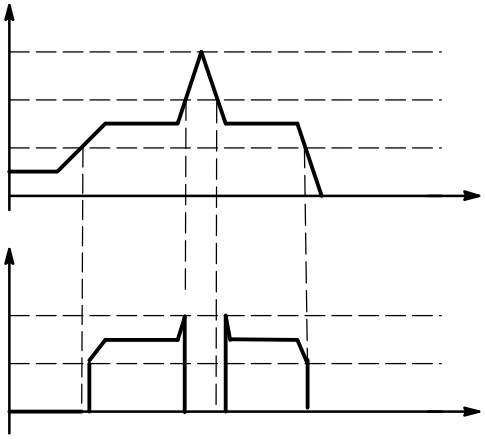


Figure 20. Output Characteristic vs. V_{in}

Overvoltage Lockout (OVLO)

To protect connected systems on V_{out} pin from overvoltage, the device has a built−in overvoltage lock out (OVLO) circuit. During overvoltage condition (OVLO exceeds), the output remains disabled and $\overline{FLAG}$ is tied low, as long as the input voltage is higher than OVLO − hysteresis. This circuit has a 100 mV hysteresis to provide noise immunity to transient conditions.

Overcurrent Protection (OCP)

The NCP361 integrates overcurrent protection to prevent system/battery overload or defect. The current limit threshold is internally set at 750 mA. This value can be changed from 150 mA to 750 mA by a metal tweak, please contact your ON Semiconductor representative for availability. During current fault, the internal PMOS FET is automatically turned off (5 μs) if the charge current exceeds I_{lim}. NCP361 goes into turn on and turn off mode as long as defect is present. The internal ton delay (4 ms typical) allows limiting thermal dissipation. The Flag pin goes to low level when an overcurrent fault appears. That allows the microcontroller to count defect events and turns off the PMOS with EN pin.

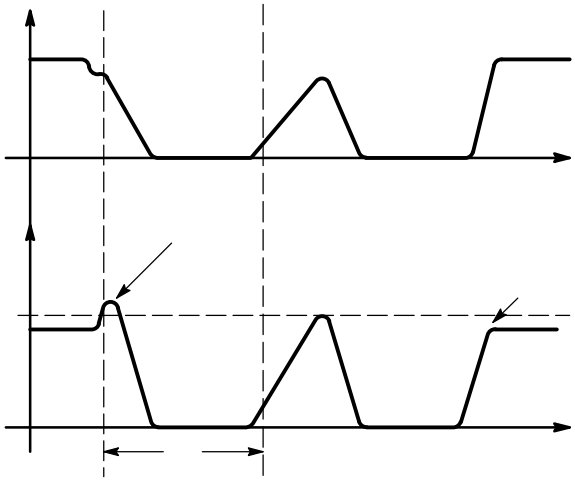


Figure 21. Overcurrent Event Example

$\overline{FLAG}$ Output

NCP361 provides a $\overline{FLAG}$ output, which alerts external systems that a fault has occurred.

This pin is tied to low as soon as: 1.2 V < V_{in} < UVLO, V_{in} > OVLO, I_{charge} > I_{limit}, T_J > 150°C. When NCP361 recovers normal condition, $\overline{FLAG}$ is held high. The pin is an open drain output, thus a pull up resistor (typically 1 MΩ − Minimum 10 kΩ) must be provided to V_{CC}. $\overline{FLAG}$ pin is an open drain output.

$\overline{EN}$ Input

To enable normal operation, the $\overline{EN}$ pin shall be forced to low or connected to ground. A high level on the pin disconnects OUT pin from IN pin. $\overline{EN}$ does not overdrive an OVLO or UVLO fault.

Internal PMOS FET

The NCP361 includes an internal PMOS FET to protect the systems, connected on OUT pin, from positive overvoltage. Regarding electrical characteristics, the $R_{DS(on)}$, during normal operation, will create low losses on V_{out} pin, characterized by V_{in} versus V_{out} dropout.

ESD Tests

The NCP361 fully supports the IEC61000−4−2, level 4 (Input pin, 1 μF mounted on board). That means, in Air condition, V_{in} has a ±15 kV ESD protected input. In Contact condition, V_{in} has ±8 kV ESD protected input. Please refer to Figure 22 to see the IEC61000−4−2 electrostatic discharge waveform.

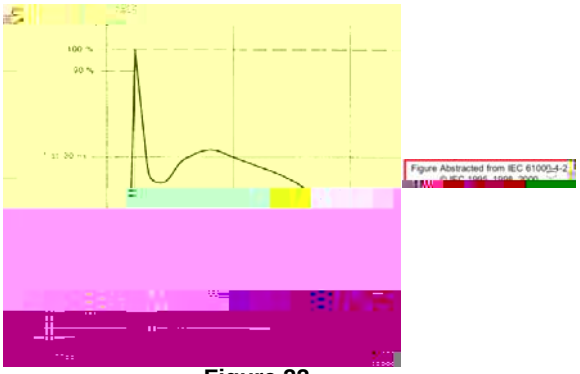


Figure 22.

PCB Recommendations

The NCP361 integrates a 500 mA rated PMOS FET, and the PCB rules must be respected to properly evacuate the heat out of the silicon. The UDFN PAD1 must be connected to ground plane to increase the heat transfer if necessary from an application standpoint. Of course, in any case, this pad shall be not connected to any other potential.

By increasing PCB area, the $R_{\theta JA}$ of the package can be decreased, allowing higher charge current to fill the battery.

Taking into account that internal bondings (wires between package and silicon) can handle up to 1 A (higher than thermal capability), the following calculation shows two different example of current capability, depending on PCB area:

- With 305°C/W (without PCB area), allowing DC current is 500 mA
- With 260°C/W (200 mm^2), the charge DC current allows with a 85°C ambient temperature is:
  $I = \sqrt{(T_J - T_A)/(R_{\theta JA} \times R_{DSON})}$
  I = 625 mA

In every case, we recommend to make thermal measurement on final application board to make sure of the final Thermal Resistance.

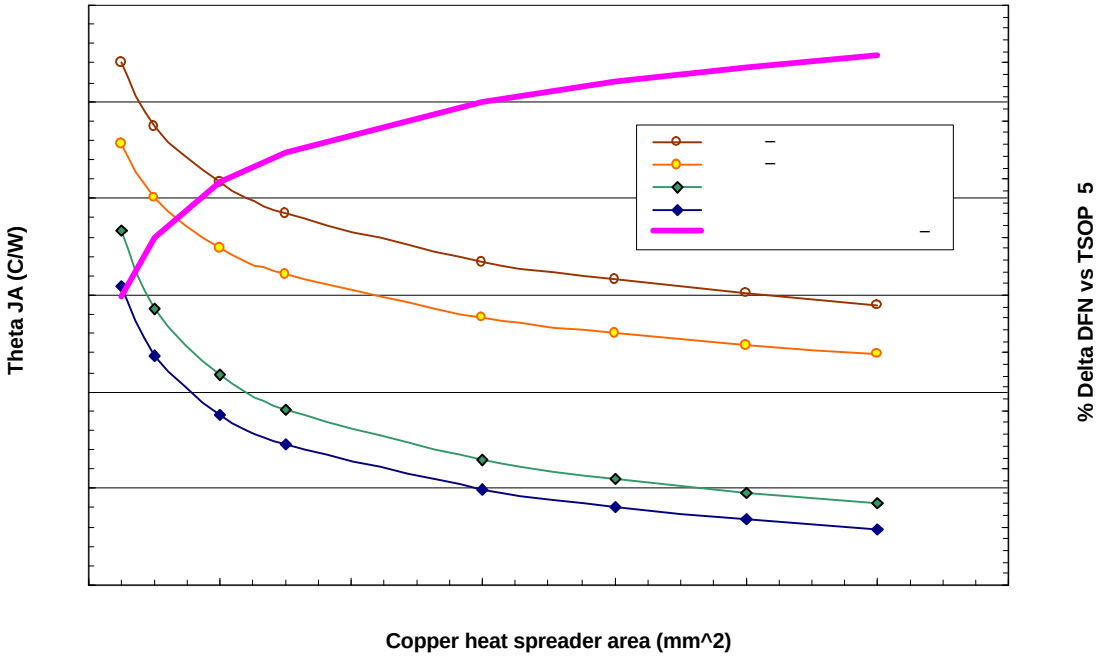
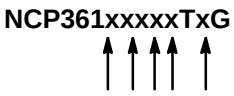


Figure 23. Thermal Resistance of UDFN 2x2 and TSOP Packages as a Function of PCB Area and Thickness

ORDERING INFORMATION

Device	Marking	Package	Shipping
		–	
		– –	
		– –	

SELECTION GUIDE



Code	Contents
	–
	–
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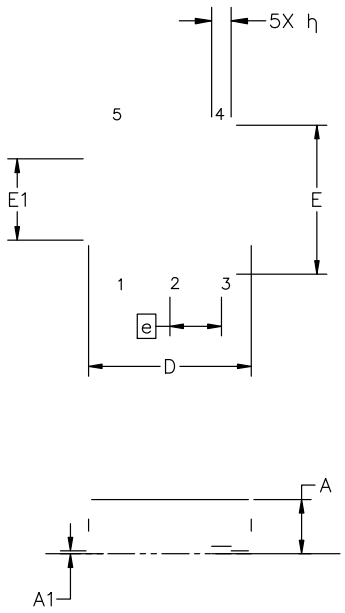
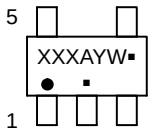
TSOP−5 3.00x1.50x0.95, 0.95P
CASE 483
ISSUE P

DATE 01 APR 2024



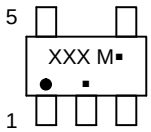
GENERIC
MARKING DIAGRAM*



Analog

XXX = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)



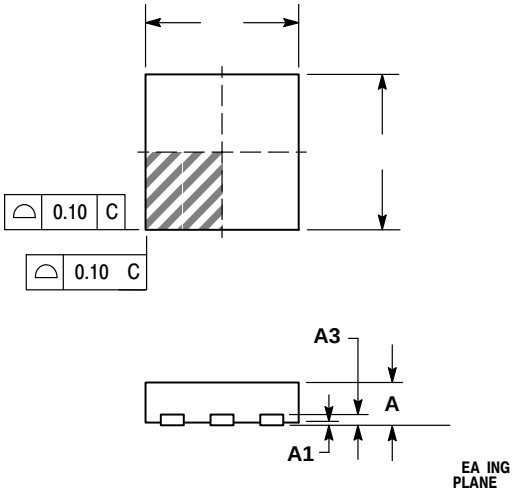
Discrete/Logic

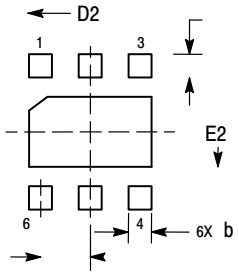
XXX = Specific Device Code
M = Date Code
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

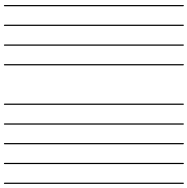
OUR Pb−FREE
STRATEGY AND SOLDERING DETAILS, PLAN

FORMATION ON





NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.25MM FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
5. TIE BARS MAY BE VISIBLE IN THIS VIEW AND ARE CONNECTED TO THE THERMAL PAD.



GENERIC
MARING DIAGRAM

XX = Specific Device Code
M = Date Code
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.