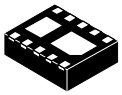
NC 347

i i O a g
i C W i
l a L W RON NMO FE
a a FLAG

Ω

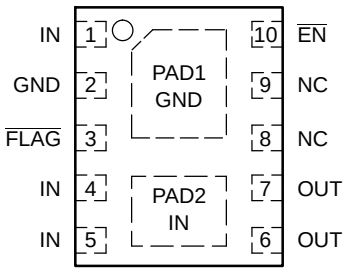
μ

- –
- Ω
- – –



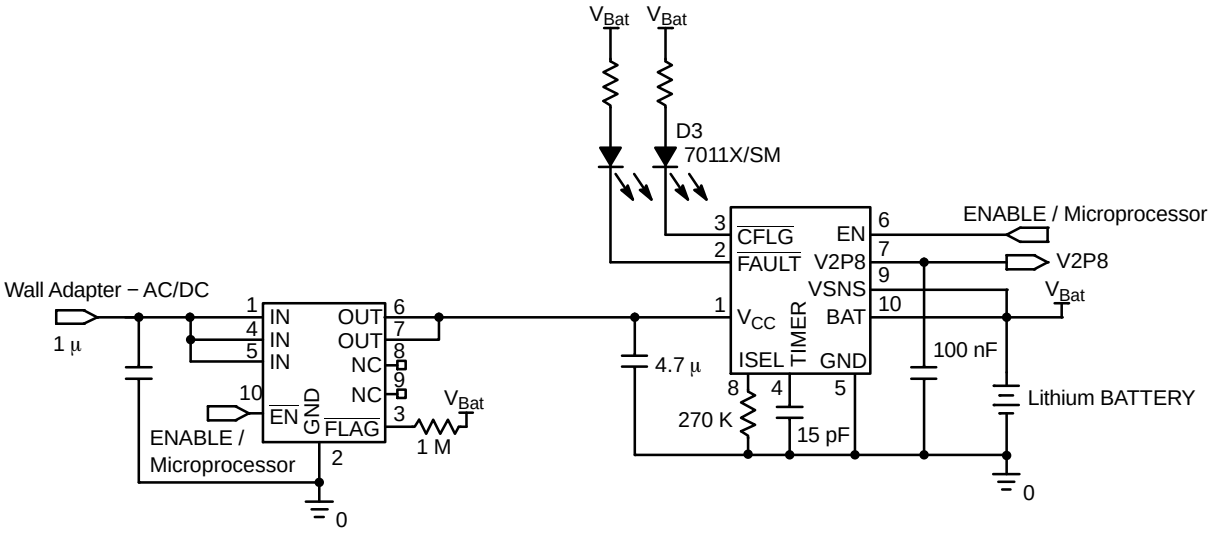
XXX M
▪

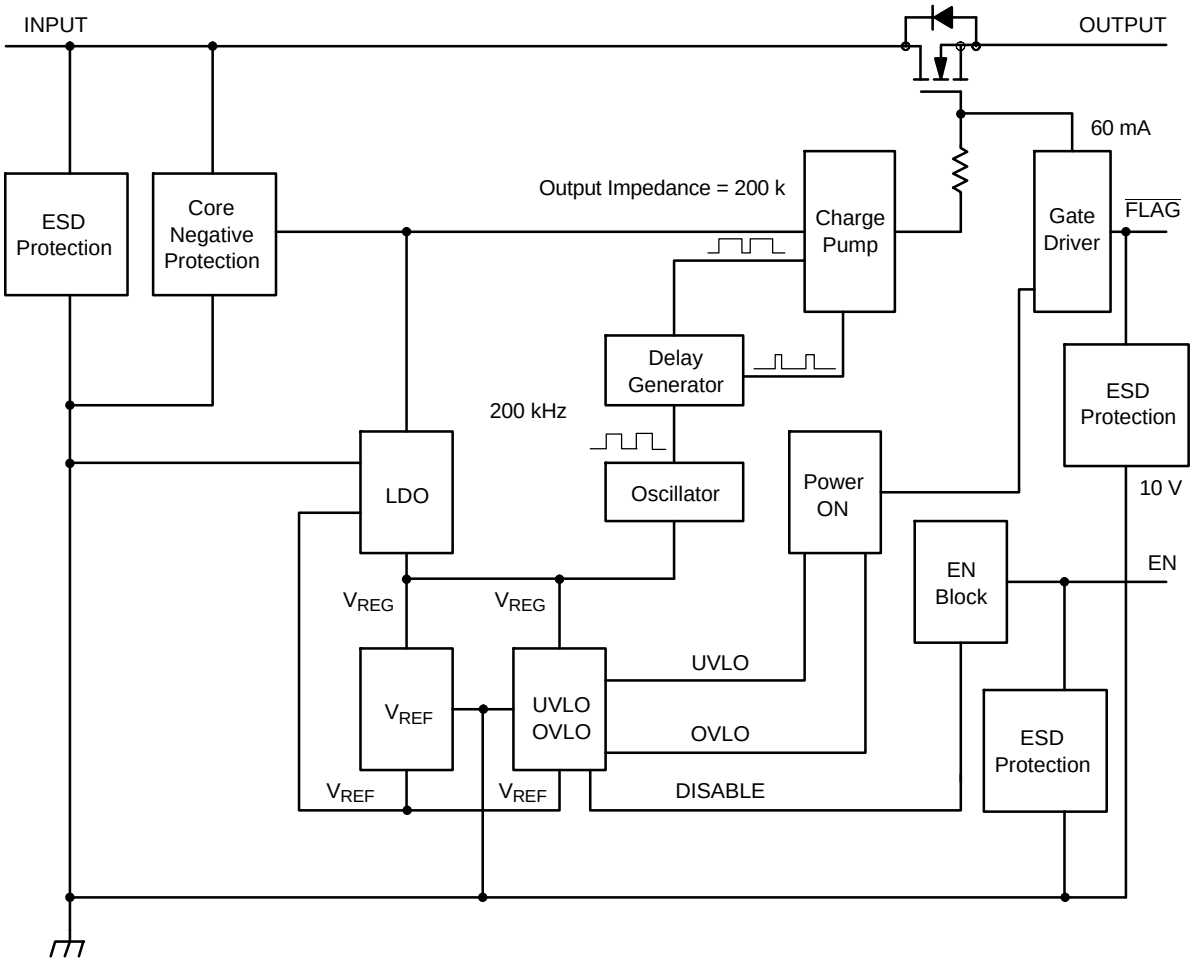
XXX = Specific Device Code
M = Date Code
▪ = Pb−Free Package



(Top View)

Publication Order Number:

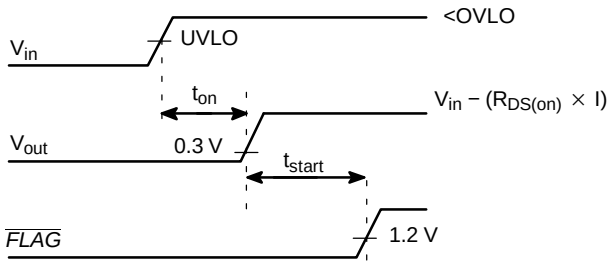

V_Bat
V_Bat
D3
7011X/SM
ENABLE / Microprocessor
V2P8
V_Bat
Wall Adapter − AC/DC
1 µ
IN
IN
IN
OUT
OUT
NC
NC
EN
GND
FLAG
ENABLE /
Microprocessor
V_Bat
1 M
CFLG
FAULT
EN
V2P8
VSNS
BAT
V_CC
ISEL
TIMER
GND
4.7 µ
270 K
15 pF
100 nF
Lithium BATTERY
0
0

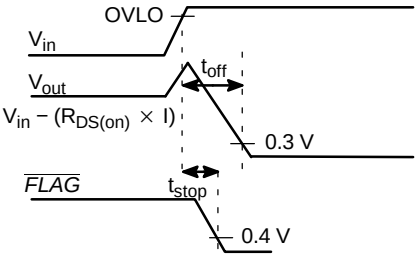

INPUT
OUTPUT
60 mA
ESD
Protection
Core
Negative
Protection
Output Impedance = 200 k
Charge
Pump
Gate
Driver
FLAG
Delay
Generator
ESD
Protection
200 kHz
LDO
Oscillator
Power
ON
10 V
EN
Block
EN
V_REG
V_REG
UVLO
V_REF
UVLO
OVLO
OVLO
ESD
Protection
V_REF
V_REF
DISABLE

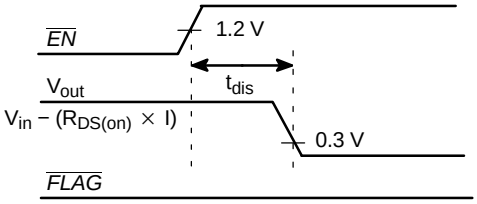
1 4 5	IN	POWER	Input Voltage Pin. This pin is connected to the power supply. The device system core is supplied by this input. A 1 μF low ESR ceramic capacitor, or larger, must be connected between this pin and GND. The three IN pins must be hardwired to common supply.
2	GND	POWER	Ground
3	$\overline{\text{FLAG}}$	OUTPUT	Fault Indication Pin. This pin allows an external system to detect a fault on IN pin. The $\overline{\text{FLAG}}$ pin goes low when input voltage exceeds OVLO threshold or drop below UVLO threshold. Since the $\overline{\text{FLAG}}$ pin is open drain functionality, an external pull up resistor to V_{CC} must be added.
6 7	OUT	OUTPUT	Output Voltage Pin. This pin follows IN pin when “no fault” is detected. The output is disconnected from the V_{in} power supply when the input voltage is under the UVLO threshold or above OVLO threshold. The two OUT pins must be hardwired to common supply.
8	NC	OPEN	No Connect
9	NC	OPEN	No Connect
10	$\overline{\text{EN}}$	INPUT	Enable Pin. The device enters in shutdown mode when this pin is tied to a high level. In this case the output is disconnected from the input. To allow normal functionality, the $\overline{\text{EN}}$ pin shall be connected to GND to a pull down or to a I/O pin. This pin does not have an impact on the fault detection.
PAD1			PAD1, under the device. See PCB recommendations page 10. Can be shorted to GND.
PAD2			The PAD2 is electrically connected to the internal NMOS drain and connected to Pins 4 and 5. See PCB recommendations page 10.

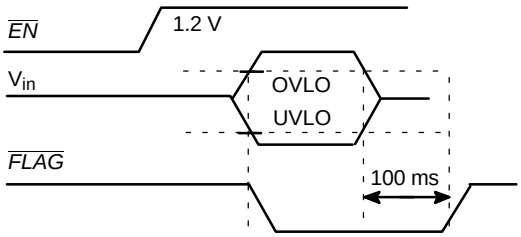
Minimum Voltage (IN to GND)	$Vmin_{in}$	−0.3	V
Minimum Voltage (All others to GND)	Vmin	−0.3	V
Maximum Voltage (IN to GND)	$Vmax_{in}$	30	V
Maximum Voltage (All others to GND)			

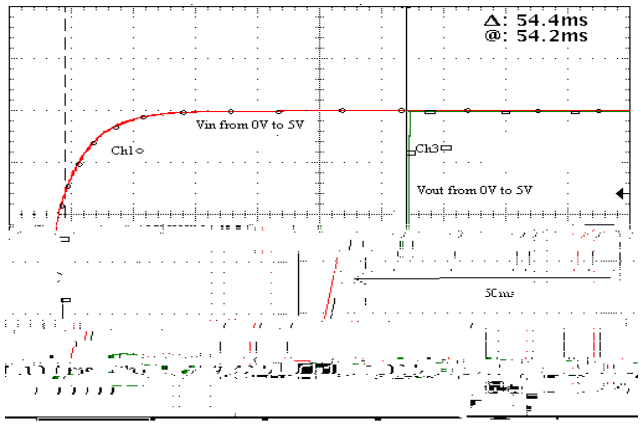
(Min/Max limits values (−40°C < T_A < +85°C) and V_{in} = +5.0 V. Typical values are T_A = +25°C,

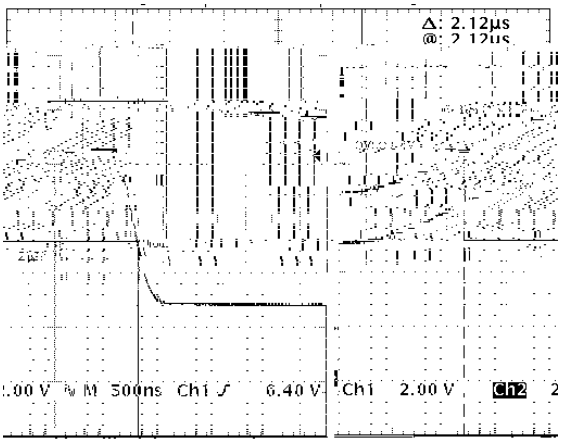

V_{in}
UVLO
<OVLO
t_{on}
$V_{in} - (R_{DS(on)} \times I)$
V_{out}
0.3 V
t_{start}
$\overline{FLAG}$
1.2 V

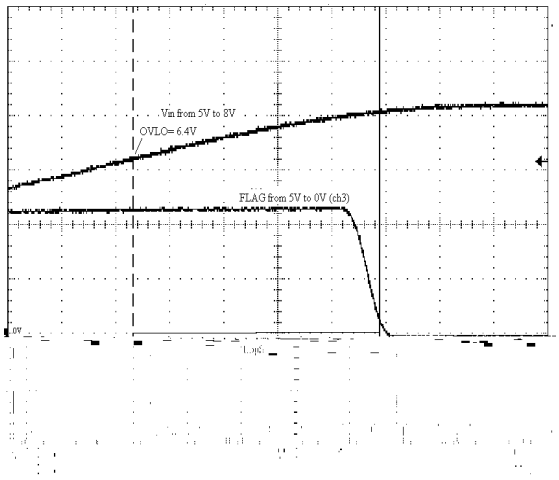

OVLO
V_{in}
t_{off}
V_{out}
$V_{in} - (R_{DS(on)} \times I)$
0.3 V
$\overline{FLAG}$
t_{stop}
0.4 V

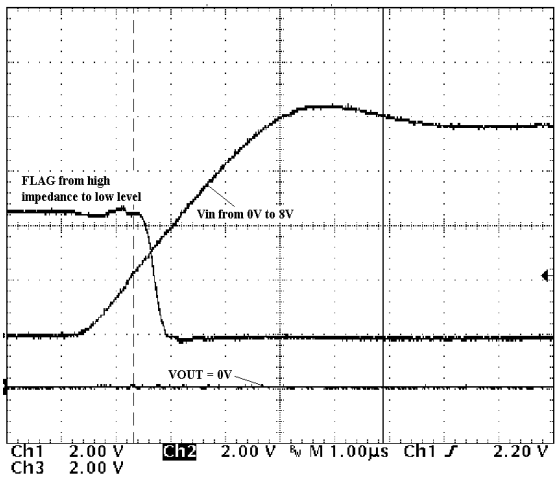

$\overline{EN}$
1.2 V
V_{out}
t_{dis}
$V_{in} - (R_{DS(on)} \times I)$
0.3 V
$\overline{FLAG}$

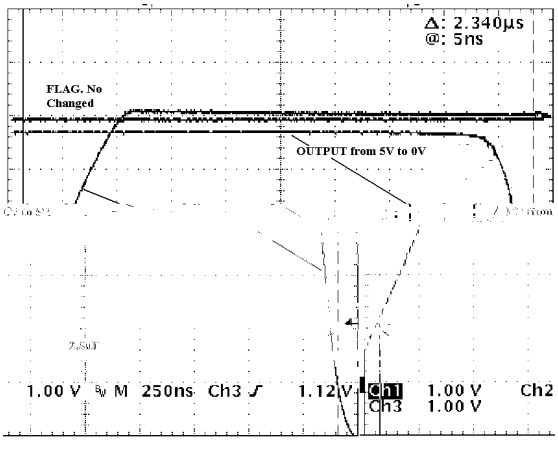

$\overline{EN}$
1.2 V
V_{in}
OVLO
UVLO
$\overline{FLAG}$
100 ms

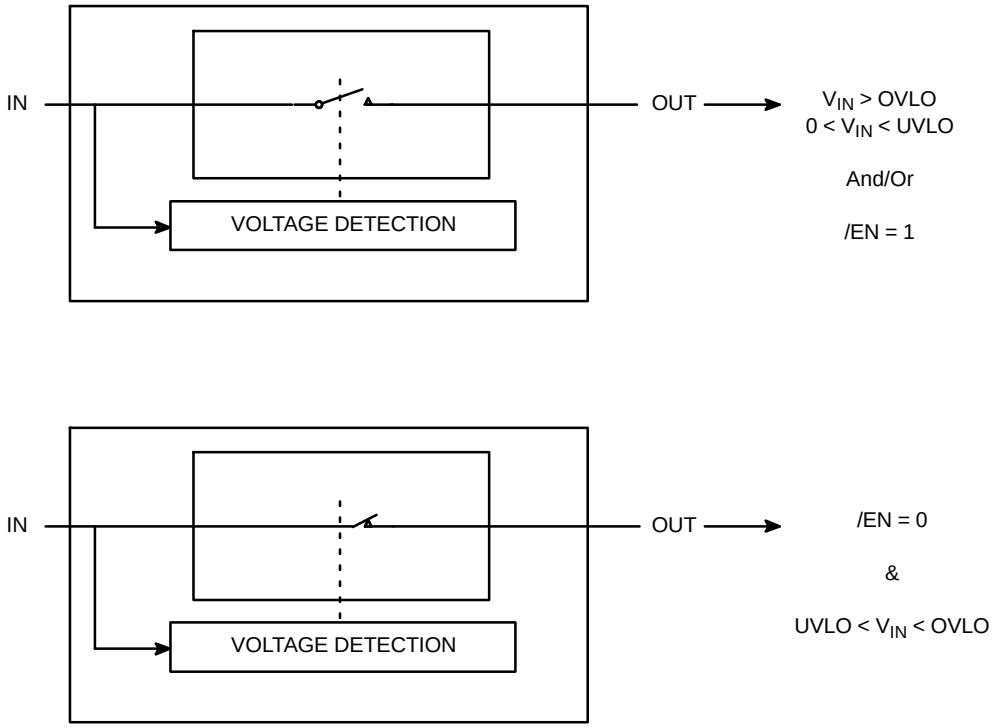

Δ: 54.4ms
@: 54.2ms
Vin from 0V to 5V
Ch1
Ch3
Vout from 0V to 5V
50ms

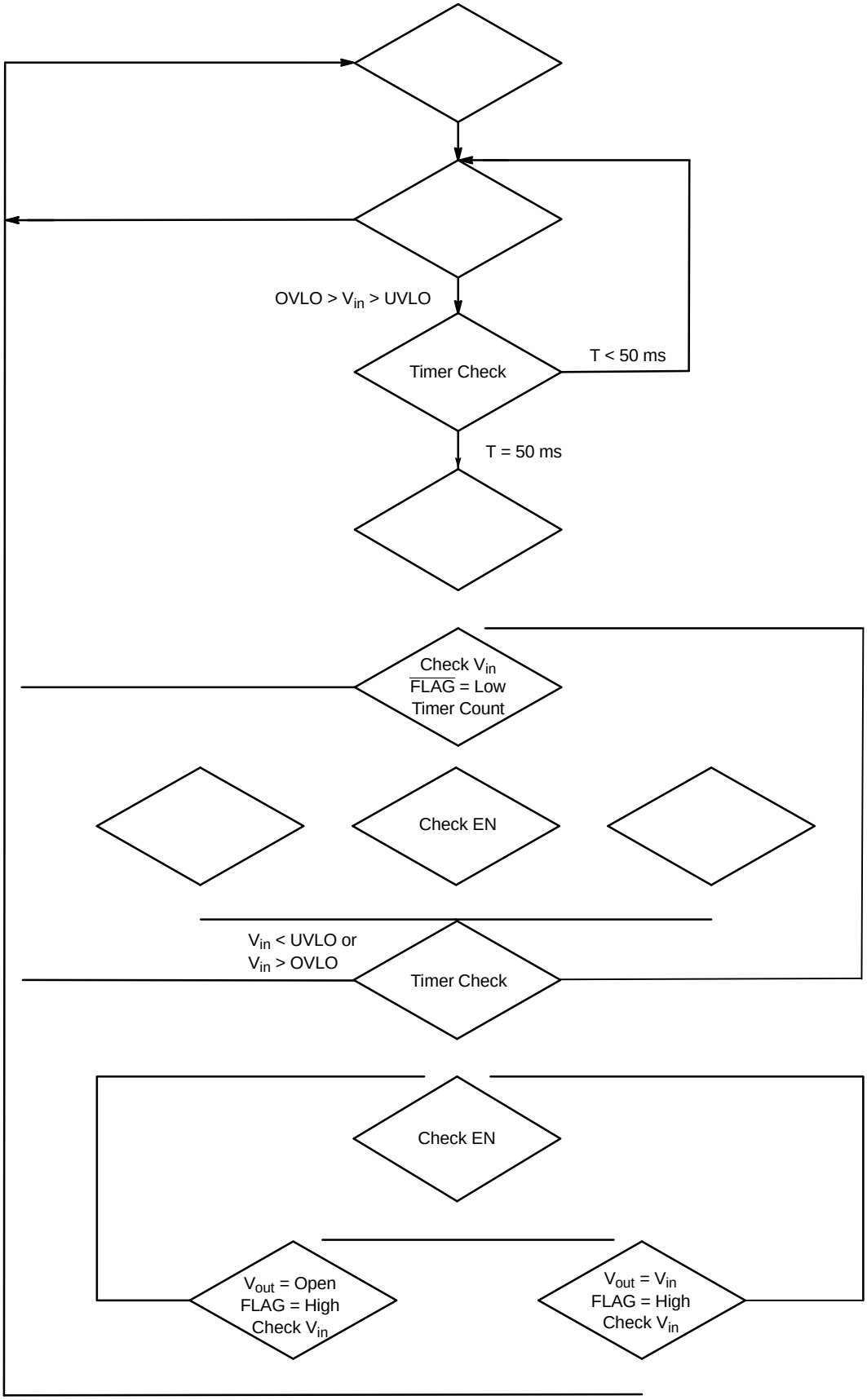

Δ: 2.12µs
@: 2.12µs
.00 V M 500ns Ch1 ƒ 6.40 V Ch1 2.00 V Ch2


Vin from 5V to 8V
OVLO= 6.4V
FLAG from 5V to 0V (ch3)


FLAG from high impedance to low level
Vin from 0V to 8V
VOUT = 0V
Ch1 2.00 V Ch2 2.00 V M 1.00µs Ch1 ƒ 2.20 V
Ch3 2.00 V


Δ: 2.340µs
@: 5ns
FLAG. No Changed
OUTPUT from 5V to 0V
1.00 V M 250ns Ch3 ƒ 1.12 V Ch1 1.00 V Ch2
Ch3 1.00 V


IN
OUT
VOLTAGE DETECTION
V_{IN} > OVLO
0 < V_{IN} < UVLO
And/Or
/EN = 1
IN
OUT
VOLTAGE DETECTION
/EN = 0
&
UVLO < V_{IN} < OVLO


OVLO > V_{in} > UVLO
Timer Check
T < 50 ms
T = 50 ms
Check V_{in}
$\overline{FLAG}$ = Low
Timer Count
Check EN
V_{in} < UVLO or
V_{in} > OVLO
Timer Check
Check EN
V_{out} = Open
FLAG = High
Check V_{in}
V_{out} = V_{in}
FLAG = High
Check V_{in}

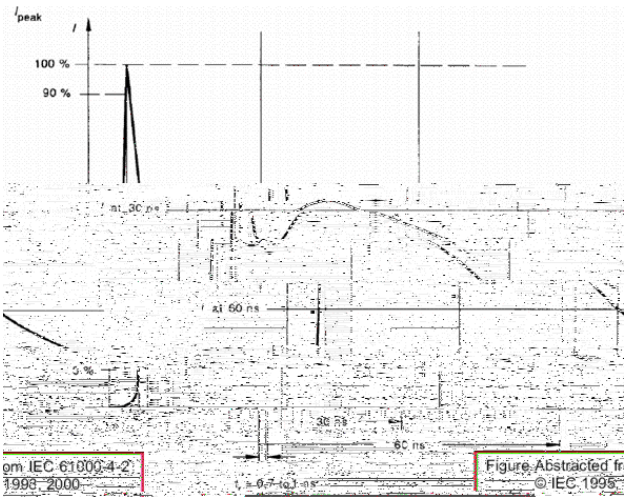
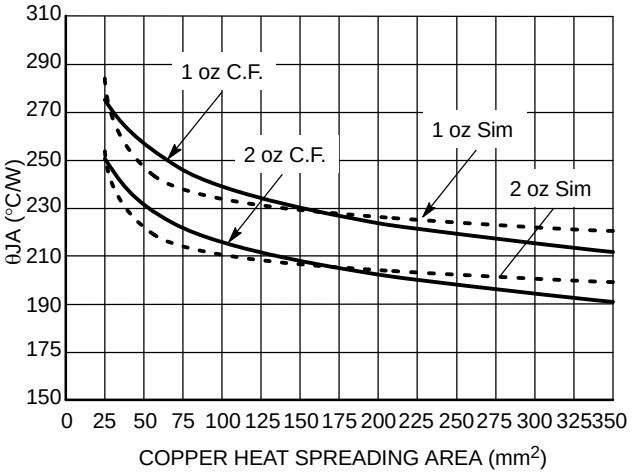
Ω
Ω,
–
– –
μ
±
±
– –
–


Figure Abstracted fr
FLAG
Ω Ω
EN


310
290
270
250
230
210
190
175
150
θJA (°C/W)
1 oz C.F.
2 oz C.F.
1 oz Sim
2 oz Sim
0 25 50 75 100 125 150 175 200 225 250 275 300 325 350
COPPER HEAT SPREADING AREA (mm2)

			†
NCP347MTAETBG	BAL	WDFN−10 (Pb−Free)	3000 / Tape & Reel
NCP347MTAFTBG	BAM		
NCP347MTAHTBG	BAK		
NCP347MTAITBG	ACJ		

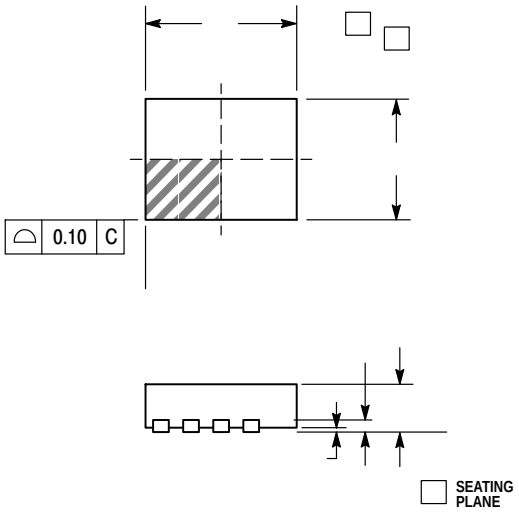
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

The NCP347 can be available in several undervoltage and overvoltage thresholds versions. Part number is designated as follows:

a	UVLO Typical Threshold a: A = 2.95 V
b	OVLO Typical Threshold b: E = 5.63 V b: F = 5.90 V b: H = 7.20 V b: I = 5.85 V
c	Tape & Reel Type c: B = 3000

CASE 516AA−01
ISSUE C

DATE 06 FEB 2007



NO ES:
1. DIMENSIONING AND TOLERANCING PER ASME 14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION APPLIES TO PLATED TERMINAL AND MEASURED BETWEEN 0.15 AND 0.30 mm FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.