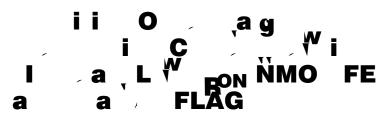
# NC 347



The NCP347 is able to disconnect the systems from its output pin in case wrong input operating conditions are detected. The system is positive overvoltage protected up to +28 V.

Due to this device using internal NMOS, no external device is necessary, reducing the system cost and the PCB area of the application board.

The NCP347 is able to instantaneously disconnect the output from the input, due to integrated Low R<sub>ON</sub> Power NMOS (65 m $\Omega$ ), if the input voltage exceeds the overvoltage threshold (OVLO) or undervoltage threshold (UVLO).

At powerup ( $\overline{EN}$  pin = low level), the  $V_{out}$  turns on 50 ms after the  $V_{in}$  exceeds the undervoltage threshold.

The NCP347 provides a negative going flag (FLAG) output, which alerts the system that a fault has occurred.

In addition, the device has ESD-protected input (15 kV Air) when bypassed with a 1.0  $\mu F$  or larger capacitor.

#### **Features**

- Overvoltage Protection up to 28 V
- On–Chip Low R<sub>DS(on)</sub> NMOS Transistor: 65 mΩ
- Internal Charge Pump
- Overvoltage Lockout (OVLO)
- Undervoltage Lockout (UVLO)
- Internal 50 ms Startup Delay
- Alert FLAG Output
- Shutdown EN Input
- Compliance to IEC61000-4-2 (Level 4)
   8.0 kV (Contact)
   15 kV (Air)
- ESD Ratings: Machine Model = B
   Human Body Model = 3
- 10 Lead WDFN 2.5x2 mm Package
- This is a Pb-Free Device

### **Applications**

- Cell Phones
- Camera Phones
- Digital Still Cameras
- Personal Digital Applications
- MP3 Players







WDFN10 MT SUFFIX CASE 516AA



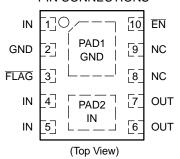


XXX = Specific Device Code

M = Date Code

= Pb-Free Package

#### PIN CONNECTIONS



ORDERING INFORMATION

1

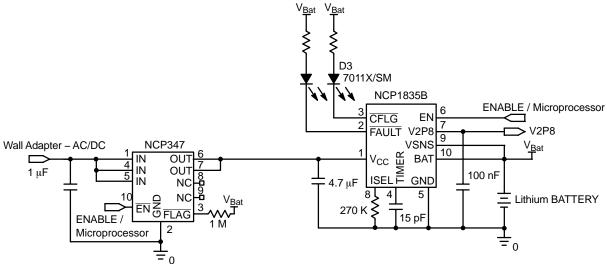


Figure 1. Typical Application Circuit

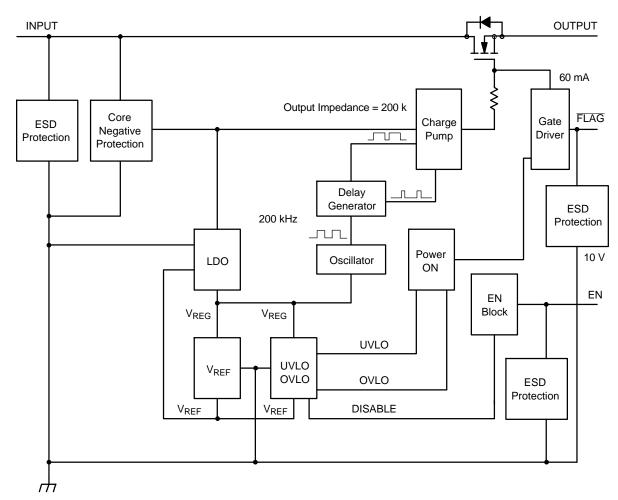


Figure 2. Functional Block Diagram

# PIN FUNCTION DESCRIPTION

Pin No.	Symbol	Function	Description
1 4 5	IN	POWER	Input Voltage Pin. This pin is connected to the power supply. The device system core is supplied by this input. A 1 µF low ESR ceramic capacitor, or larger, must be connected between this pin and GND. The three IN pins must be hardwired to common supply.
2	GND	POWER	Ground
3	FLAG	OUTPUT	Fault Indication Pin. This pin allows an external system to detect a fault on IN pin. The FLAG pin goes low when input voltage exceeds OVLO threshold or drop below UVLO threshold. Since the FLAG pin is open drain functionality, an external pull up resistor to V <sub>CC</sub> must be added.
6 7	OUT	OUTPUT	Output Voltage Pin. This pin follows IN pin when "no fault" is detected. The output is disconnected from the V <sub>in</sub> power supply when the input voltage is under the UVLO threshold or above OVLO threshold. The two OUT pins must be hardwired to common supply.
8	NC	OPEN	No Connect
9	NC	OPEN	No Connect
10	ĒN	INPUT	Enable Pin.  The device enters in shutdown mode when this pin is tied to a high level. In this case the output is disconnected from the input.  To allow normal functionality, the EN pin shall be connected to GND to a pull down or to a I/O pin.  This pin does not have an impact on the fault detection.
PAD1			PAD1, under the device. See PCB recommendations page 10. Can be shorted to GND.
PAD2			The PAD2 is electrically connected to the internal NMOS drain and connected to Pins 4 and 5. See PCB recommendations page 10.

### MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Minimum Voltage (IN to GND)	Vmin <sub>in</sub>	-0.3	V
Minimum Voltage (All others to GND)	Vmin	-0.3	V
Maximum Voltage (IN to GND)		30	V
Maximum Voltage (All others to GND)	_		•

Maximum Voltage (All others to GND)

ELECTRICAL CHARACTERISTICS (Min/Max limits values ( $-40^{\circ}$ C < $T_A$ < +85°C) and $V_{in}$ = +5.0 V. Typical values are $T_A$ = +25°C,

### **TIMING DIAGRAMS**

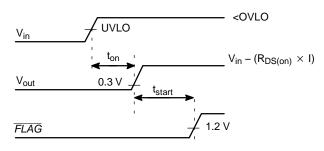


Figure 3. Startup

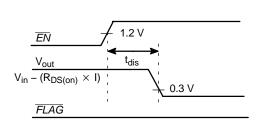


Figure 5. Disable on  $\overline{EN} = 1$ 

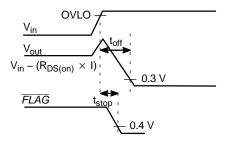


Figure 4. Shutdown on Overvoltage Detection

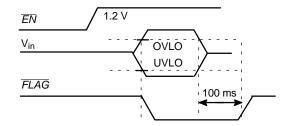


Figure 6.  $\overline{FLAG}$  Response with  $\overline{EN} = 1$ 

### TYPICAL OPERATING CHARACTERISTICS

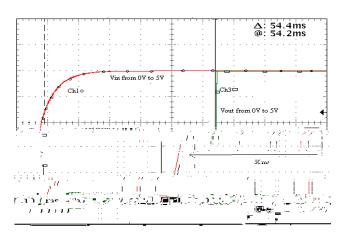


Figure 7. Startup  $V_{in}$  = Ch1,  $V_{out}$  = Ch3

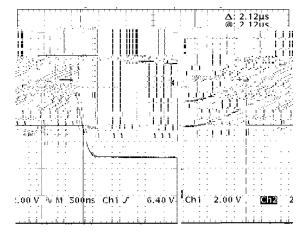


Figure 8. Output Turn Off Time  $V_{in} = Ch1$ ,  $V_{out} = Ch2$ 

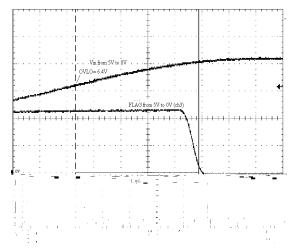


Figure 10. Alert Delay  $V_{out} = Ch1$ , FLAG = Ch3

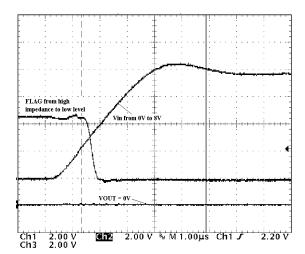


Figure 9. FLAG Going Up Delay

 $V_{out} = Ch3$ , FLAG = Ch2

Figure 11. Initial Overvoltage Delay  $V_{in} = Ch1$ ,  $V_{out} = Ch2$ , FLAG = Ch3

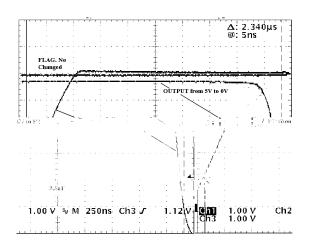


Figure 12. Disable Time EN = Ch1, V<sub>out</sub> = Ch2, FLAG = Ch3

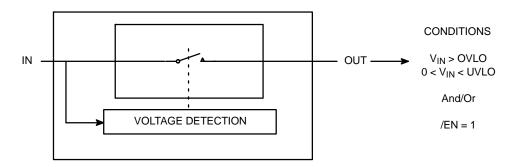


Figure 16. Simplified Diagram

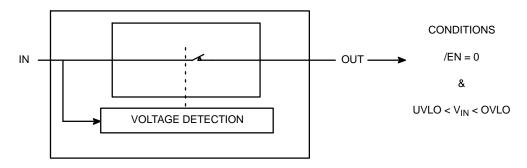


Figure 17. Simplified Diagram

#### Operation

The NCP347 provides overvoltage protection for positive voltage, up to 28 V. A Low  $R_{DS(on)}$  NMOS FET protects the systems (i.e.: charger) connected on the Vout pin, against positive overvoltage. At powerup, with  $\overline{EN}$  pin = low, the output is rising up 50 ms after the input

overtaking undervoltage UVLO (Figure 3). The NCP347 provides a  $\overline{\text{FLAG}}$  output, which alerts the system that a fault has occurred. A 50 ms additional delay, regarding available output (Figure 3) is added between output signal rising up and to  $\overline{\text{FLAG}}$  signal rising up.  $\overline{\text{FLAG}}$  pin is an open drain output.

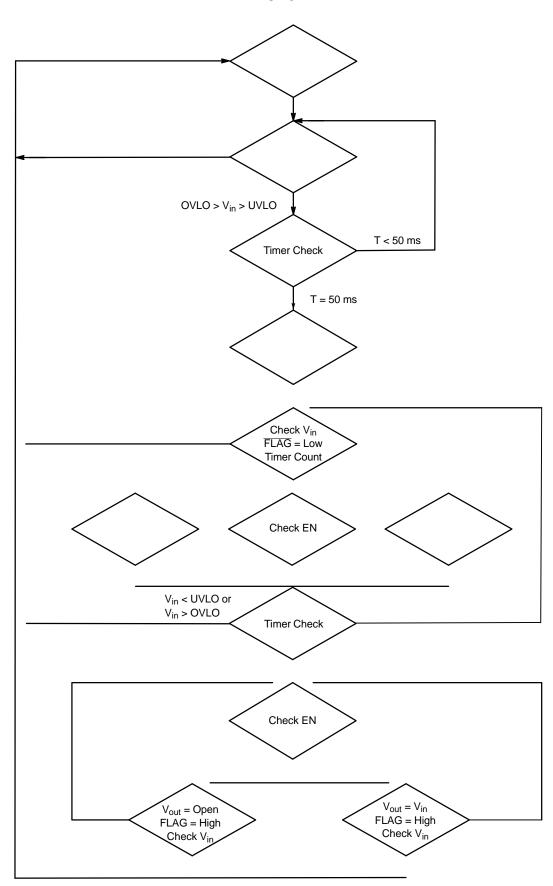


Figure 18. State Machine

#### Undervoltage Lockout (UVLO)

To ensure proper operation under any conditions, the device has a built—in undervoltage lockout (UVLO) circuit. During  $V_{in}$  positive going slope, the output remains disconnected from input until  $V_{in}$  voltage is below 2.92 V, plus hysteresis, nominal. The FLAG output is tied to low as long as  $V_{in}$  does not reach UVLO threshold. This circuit has a 60 mV hysteresis to provide noise immunity to transient condition. Additional UVLO thresholds ranging from UVLO can be manufactured. (See Selection Guide on page 12) Contact your ON Semiconductor representative for availability.

### Overvoltage Lockout (OVLO)

To protect connected systems on V<sub>out</sub> pin from overvoltage, the device has a built–in overvoltage lockout (OVLO) circuit. During overvoltage condition, the output remains disabled as long as the input voltage exceeds 5.675 V typical (NCP347MTAE). Additional OVLO thresholds ranging from OVLO can be manufactured. (See Selection Guide on page 12) Contact your ON Semiconductor representative for availability.

FLAG output is tied to low until V<sub>in</sub> is higher than OVLO. This circuit has a 90 mV hysteresis to provide noise immunity to transient conditions.

#### FLAG Output

The NCP347 provides a FLAG output, which alerts external systems that a fault has occurred.

This pin is tied to low as soon the OVLO threshold is exceeded or when the  $V_{in}$  level is below the UVLO threshold. When  $V_{in}$  level recovers normal condition,  $\overline{FLAG}$  is held high, keeping in mind that an additional 50 ms delay has been added between available output and  $\overline{FLAG}$  = high. The pin is an open drain output, thus a pull up resistor (typically 1 M $\Omega$ , minimum 10 k $\Omega$ ) must be added to  $V_{bat}$ . Minimum  $V_{bat}$  supply must be 2.5 V. The  $\overline{FLAG}$  level will always reflects  $V_{in}$  status, even if the device is turned off ( $\overline{EN}$  = 1).

### **EN** Input

To enable normal operation, the  $\overline{\text{EN}}$  pin shall be forced to low or connected to ground. A high level on the pin, disconnects OUT pin from IN pin.  $\overline{\text{EN}}$  does not overdrive an OVLO or UVLO fault.

#### Internal NMOS FET

The NCP347 includes an internal Low  $R_{DS(on)}$  NMOS FET to protect the systems, connected on OUT pin, from positive overvoltage. Regarding electrical characteristics, the  $R_{DS(on)}$ , during normal operation, will create low losses on  $V_{out}$  pin.

As example:  $R_{load} = 8.0 \Omega$ ,  $V_{in} = 5.0 V$ Typical  $R_{DS(on)} = 65 \text{ m}\Omega$ ,  $I_{out} = 618 \text{ m}A$ 

 $V_{out} = 8 \times 0.618 = 4.95 \text{ V}$ 

NMOS losses =  $R_{DS(on)} \times lout^2 = 0.065 \times 0.618^2 = 25 \text{ mW}$ 

### **ESD Tests**

The NCP347 input pin fully supports the IEC61000–4–2. 1.0  $\mu$ F (minimum) must be connected between V<sub>in</sub> and GND, close to the device.

That means, in Air condition,  $V_{in}$  has a  $\pm$  15 kV ESD protected input. In Contact condition,  $V_{in}$  has  $\pm$  8.0 kV ESD protected input.

Please refer to Figure 19 to see the IEC 61000-4-2 electrostatic discharge waveform.

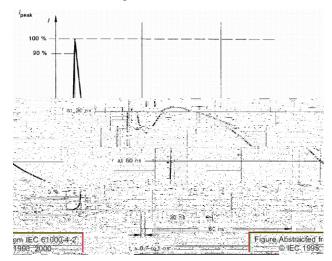


Figure 19. Electrostatic Discharge Waveform

#### PCB Recommendations

The NCP347 integrates a 2 amperes rated NMOS FET.

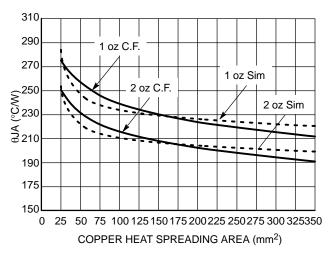


Figure 20.

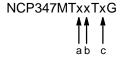
### ORDERING INFORMATION

Device	Marking	Package	Shipping <sup>†</sup>
NCP347MTAETBG	BAL		
NCP347MTAFTBG	BAM	WDFN-10 (Pb-Free)	3000 / Tape & Reel
NCP347MTAHTBG	BAK		
NCP347MTAITBG	ACJ		

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

### **SELECTION GUIDE**

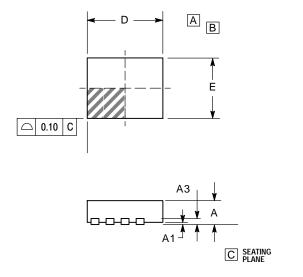
The NCP347 can be available in several undervoltage and overvoltage thresholds versions. Part number is designated as follows:



Code	Contents
а	UVLO Typical Threshold a: A = 2.95 V
b	OVLO Typical Threshold b: E = 5.63 V b: F = 5.90 V b: H = 7.20 V b: I = 5.85 V
С	Tape & Reel Type c: B = 3000

# WDFN10 2.5x2, 0.5P CASE 516AA-01 ISSUE C

# DATE 06 FEB 2007



2. 3.	DIME® IONING AND OLERANCING PER # ME 14.5M, 1994. CON ROLLING DIME® ION: MILLIME EP. DIME® ION APPLIE O PLA ED ERMINAL AND ME® RED BE #EEN 0.15 AND 0.30   FROM ERMINAL
4.	COPLANARI APPLIB O HEE PO ED. PAD A FELLAS, HE ERMINAD.

