# NCP346

## OV– V a –P –c IC

The NCP346 Overvoltage Protection circuit (OVP) protects sensitive electronic circuitry from overvoltage transients and power supply faults when used in conjunction with an external P−channel

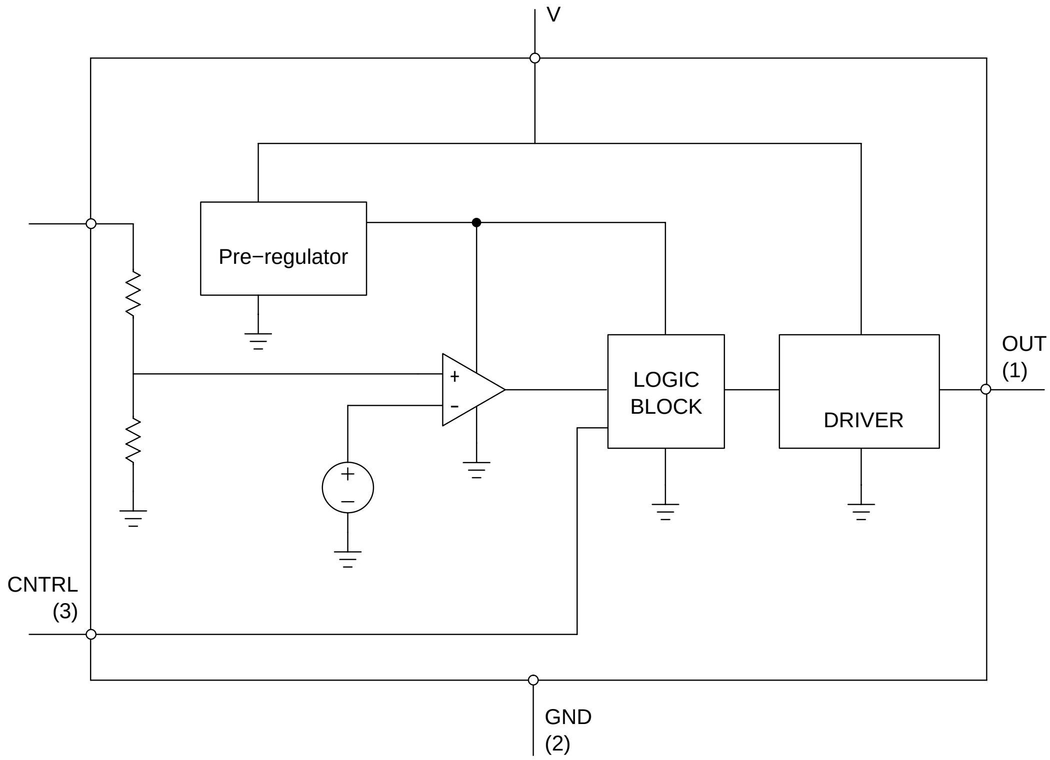



**Figure 2. Detailed Block Diagram**

**MAXIMUM RATINGS** ($T_A$ = 25°C unless otherwise noted.)

| Rating | Pin | Symbol | Min | Max | Unit |
|---|---|---|---|---|---|
| OUT Voltage to GND | 1 | $V_O$ | −0.3 | 30 | V |
| Input and CNTRL Pin Voltage to GND | 4<br>3 | $V_{input}$<br>$V_{CNTRL}$ | −0.3<br>−0.3 | 30<br>13 | V |
| Input Pin Voltage to $V_{CC}$ | 4, 5 | $V(V_{CC,}$ IN) | −0.3 | 15 | V |
| $V_{CC}$ Maximum Range | 5 | $V_{CC(max)}$ | −0.3 | 30 | V |
| Maximum Power Dissipation at $T_A$ = 85°C | − | $P_D$ | − | 0.216 | W |
| Thermal Resistance, Junction−to−Air | − | $R_{\theta JA}$ | − | 300 | °C/W |
| Junction Temperature | − | $T_J$ | − | 150 | °C |
| Operating Ambient Temperature | − | $T_A$ | −40 | 85 | °C |
| $V_{CNTRL}$ Operating Voltage | 3 | − | 0 | 5.0 | V |
| Storage Temperature Range | − | $T_{stg}$ | −65 | 150 | °C |

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

**ATTRIBUTES**

| Characteristic | Value |
|---|---|
| ESD Protection<br>Human Body Model (HBM) per JEDEC Standard JESD22−A114<br>Machine Model (MM) per JEDEC Standard JESD22−A114 | <br>≤ 2.5 kV<br>≤ 250 V |
| Moisture Sensitivity, Indefinite Time Out of Drypack (Note 1) | Level 1 |
| Transistor Count | 89 |
| Latchup Current Maximum Rating per JEDEC Standard EIA/JESD78 | ≤ 150 mA |

1. For additional Moisture Sensitivity information, refer to Application Note AND8003/D.

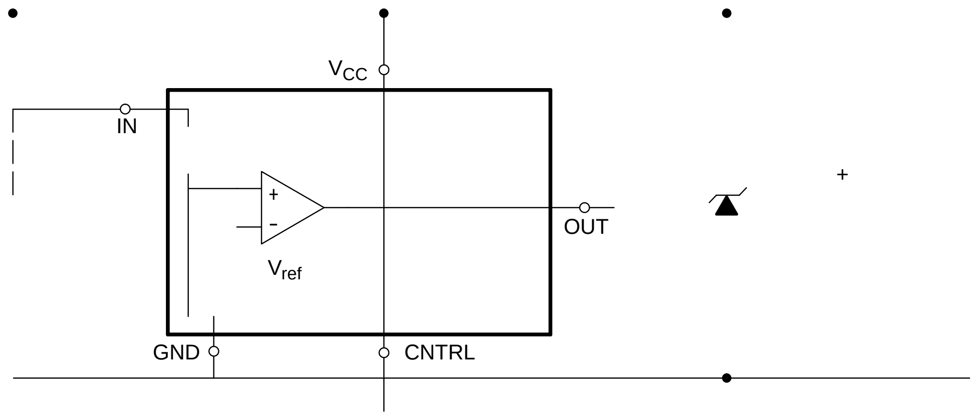
**ELECTRICAL CHARACTERISTICS** (NCP346SN1T1)
(For typical values $T_A$ = 25°C, for min/max values $T_A$ = −40°C to +85°C unless otherwise noted.)

| Characteristic | Pin | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{CC}$ Operating Voltage Range | 5 | | | | | |

**ELECTRICAL CHARACTERISTICS** (NCP346SN2T1)
(For typical values $T_A$ = 25°C, for min/max values $T_A$ = −40°C to +85°C unless otherwise noted.)

| Characteristic | Pin | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{CC}$ Operating Voltage Range | 5 | $V_{CC(opt)}$ | 2.5 | − | 25 | V |
| Total Supply Current (IN Connected to $V_{CC}$; ON Mode, $V_{CC}$ = 5.0 V, CNTRL Pin Floating, Steady State) | 4, 5 | $I_{cc\ on}$ | − | 650 | 1200 | μA |
| Total Supply Current (IN Connected to $V_{CC}$; OFF Mode Driven by CNTRL Pin, $V_{CC}$ = 5.0 V, $V_{CNTRL}$ = 1.5 V, Steady State) | 4, 5 | $I_{cc\ off}$ CNTRL | − | 700 | 1200 | μA |
| Total Supply Current (IN Connected to $V_{CC}$; OFF Mode Driven by Overvoltage, $V_{CC}$ = 6.0 V, CNTRL Pin Floating, Steady State) | 4, 5 | $I_{cc\ off}$ IN | − | 750 | 1200 | μA |
| Input Threshold (IN Connected to $V_{CC}$; $V_{CC}$ Increasing) | 4 | $V_{th}$ (LH) | 5.3 | 5.5 | 5.7 | V |
| Input Threshold (IN Connected to $V_{CC}$; $V_{CC}$ Decreasing) | 4 | $V_{th}$ (HL) | 5.3 | 5.45 | 5.7 | V |
| Input Hysteresis (IN Connected to $V_{CC}$) | 4 | $V_{hyst}$ | − | 50 | − | mV |

# APPLICATION INFORMATION



### Normal Operation

Figure 1 illustrates a typical configuration. The external adapter provides power to the protection system so the circuitry is only active when the adapter is connected. The

**Design Steps for Adjusting the Overvoltage Threshold**

1. Use Typical $R_{in}$, and $V_{th}$ Values from the Electrical Specifications
2. Minimize $R_{in}$ Effect by Selecting $R_1$ << $R_{in}$ since:

$$V_{OV} = V_{th}(1 + R_1/R_2 + R_1/R_{in}). \quad \text{(eq. 6)}$$

3. Let X = $R_{in}$ / $R_1$ = 100.
4. Identify Required Nominal Overvoltage Threshold.
5. Calculate nominal $R_1$ and $R_2$ from Nominal Values:

$$R_1 = R_{in}/X \quad \text{(eq. 7)}$$

$$R_2 = \frac{R_1}{(V_{OV}/V_{th} - R_1/R_{in} - 1)} \quad \text{(eq. 8)}$$

6. Pick Standard Resistor Values as Close as Possible to these Values
7. Use min/max Data and Resistor Tolerances to Determine Overvoltage Detection Tolerance:

$$V_{OVmin} = V_{thmin}(1 + R_{1min}/R_{2max} + R_{1min}/R_{inmax}) \quad \text{(eq. 9)}$$

$$V_{OVtyp} = V_{thtyp}(1 + R_{1typ}/R_{2typ} + R_{1typ}/R_{intyp}) \quad \text{(eq. 10)}$$

$$V_{OVmax} = V_{thmax}(1 + R_{1min} R_{2max} + R_{1max}/R_{inmin}) \quad \text{(eq. 11)}$$

The specification takes into account the hysteresis of the comparator, so the minimum input threshold voltage ($V_{th}$) is the falling voltage detection point and the maximum is the rising voltage detection point. One should design the input supply such that its maximum supply voltage in normal operation is less than the minimum desired overvoltage threshold.

8. Use worst case resistor tolerances to determine the maximum $V(V_{CC}$,IN)

$$V(V_{CC}, IN)\,min = V_{CCmax} * (R1min/(R1min + R2max)) \quad \text{(eq. 12)}$$

$$V(V_{CC}, IN)typ = V_{CCmax} * (R1typ/(R1typ + R2typ)) \quad \text{(eq. 13)}$$

$$V(V_{CC}, IN)\,max = V_{CCmax} * (R1max/(R1max + R2min)) \quad \text{(eq. 14)}$$

This is shown empirically in Tables 2 through 4.

The following tables show an example of obtaining a 6 V detection voltage from the NCP346SN2T2, which has a typical $V_{th}$ of 5.5 V.

**Table 1. Design Steps 1−5**

| Parameter | Typical | Design Steps |
| --- | --- | --- |
| IN Pin Input Impedance ($I_N$) | 54000 | (1) |

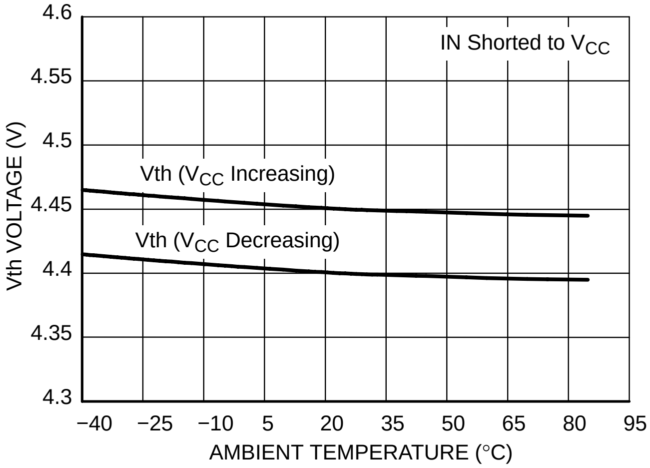
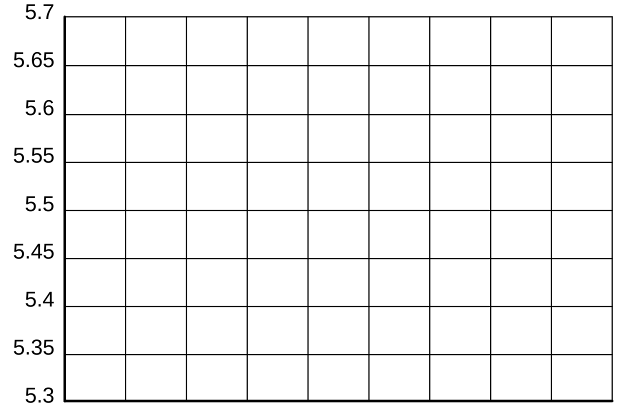



**Figure 5. Typical Vth Variation vs. Temperature (NCP346SN1)**




0 2.5 5 7.5 10 12.5 15 17.5 20 22.5 25 27.530

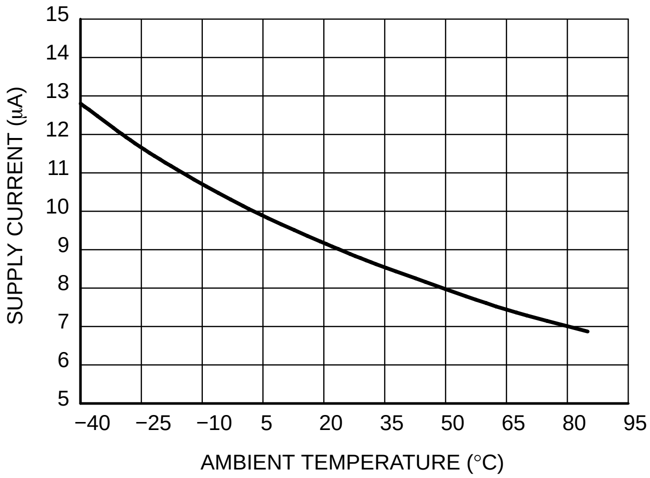



**Figure 11. Typical OUT Sink Current vs. Temperature (NCP346SN1)**

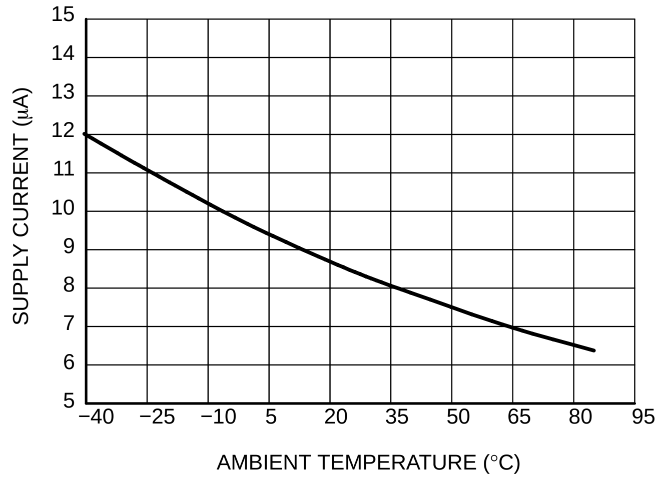



**Figure 12. Typical OUT Sink Current vs. Temperature (NCP346SN2)**

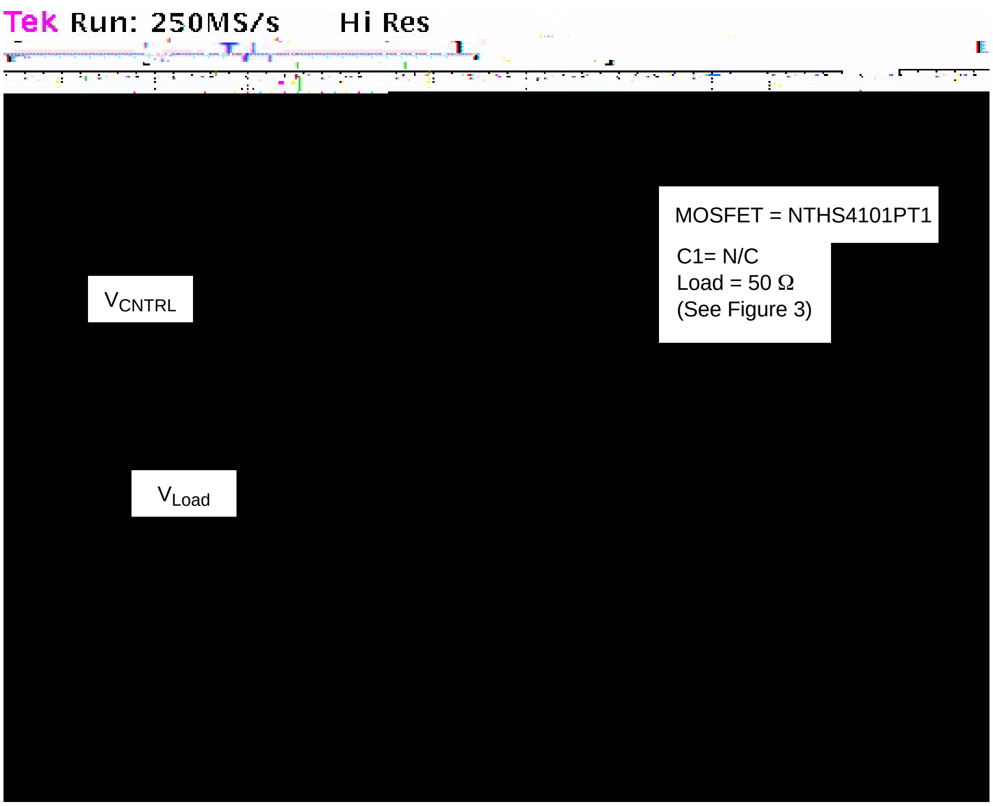



**Figure 13. Typical Turn−off Time CNTRL (NCP346SN1)**

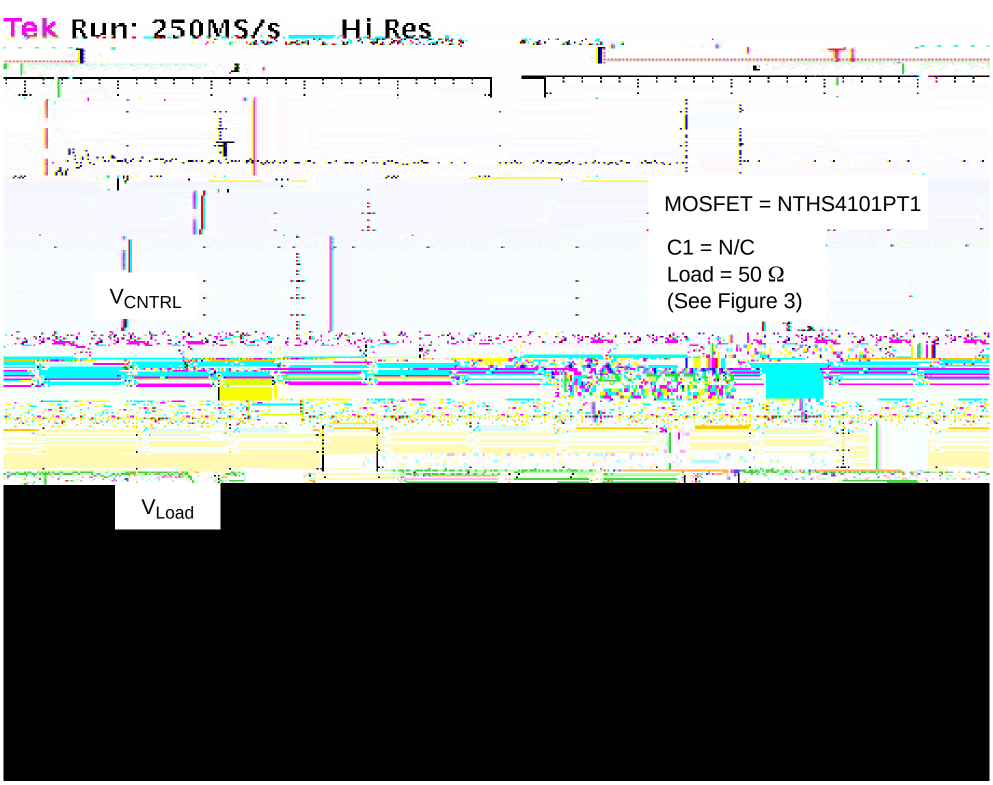



**Figure 14. Typical Turn−off Time CNTRL (NCP346SN2)**

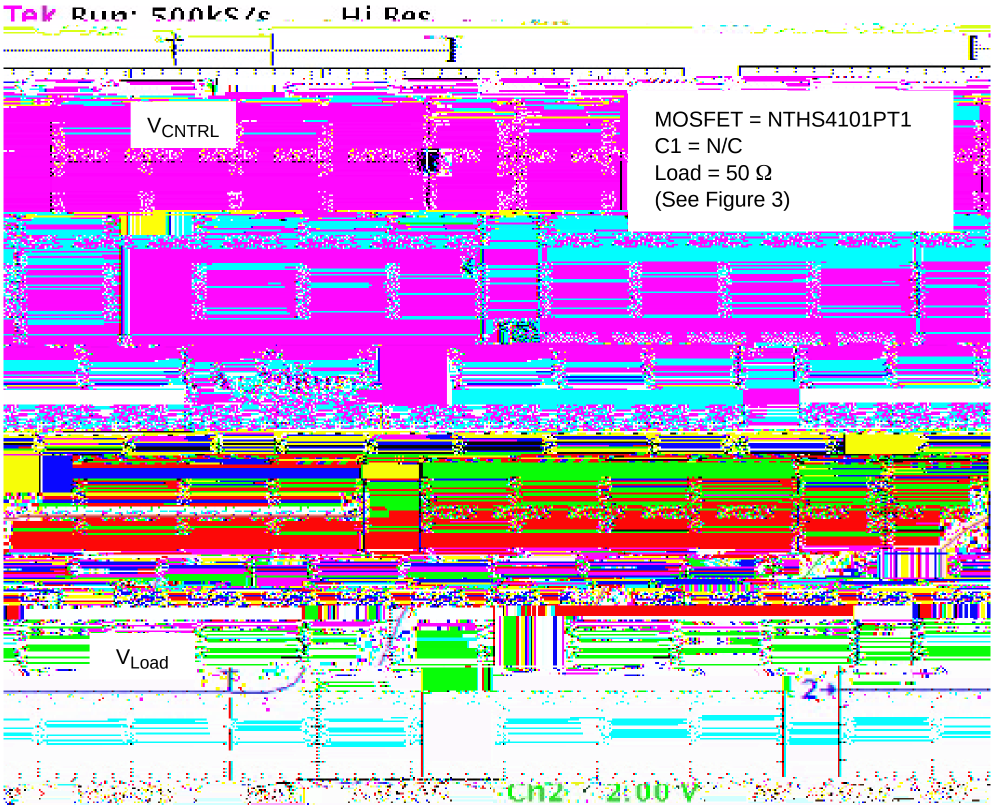



**Figure 15. Typical Turn−on Time CNTRL (NCP346SN1)**

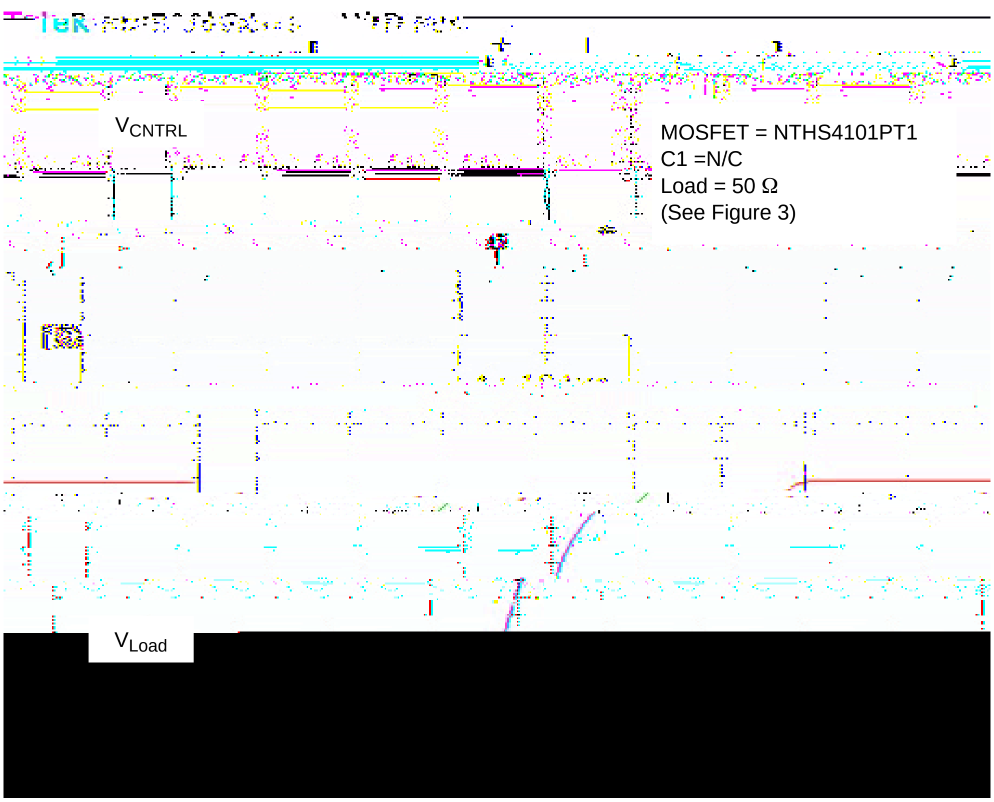



**Figure 16. Typical Turn−on Time CNTRL (NCP346SN2)**

## THIN SOT−23−5 POWER DISSIPATION

The power dissipation of the Thin SOT−23−5 is a function of the pad size. This can vary from the minimum pad size for soldering to a pad size given for maximum power dissipation. Power dissipation for a surface mount device is determined by $T_{J(max)}$, the maximum rated junction temperature of the die, $R_{\theta JA}$, the thermal resistance from the device junction to ambient, and the operating temperature, $T_A$. Using the values provided on the data sheet for the Thin SOT−23−5 package, $P_D$ can be calculated as follows:

$$P_D = \frac{T_{J(max)} - T_A}{R_{\theta JA}}$$

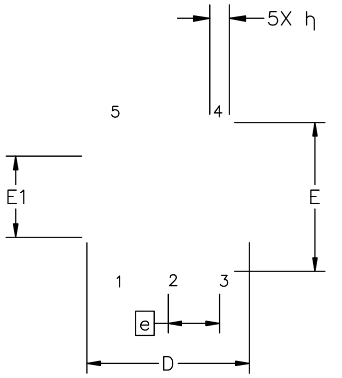
The values for the equation are found in the maximum ratings table on the data sheet. Substituting these values into the equation for an ambient temperature $T_A$ of 25°C, one can calculate the power dissipation of the device which in this case is 400 milliwatts.

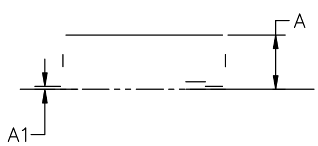
$$P_D = \frac{150°C - 25°C}{300°C/W} = 417 \text{ milliwatts}$$

The 300°C/W for the Thin SOT−23−5 package assumes the use of the recommended footprint on a glass epoxy printed circuit board to achieve a power dissipation of 417mw.

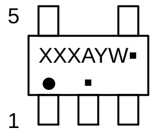
**TSOP−5 3.00x1.50x0.95, 0.95P**
CASE 483
ISSUE P

DATE 01 APR 2024

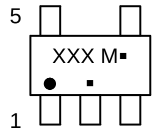



**GENERIC**
**MARKING DIAGRAM***




**Analog**




**Discrete/Logic**

XXX = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
▪ = Pb−Free Package

XXX = Specific Device Code
M = Date Code
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

OUR Pb−FREE
STRATEGY AND SOLDERING DETAILS, PLN

FORMATION ON