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I D
MO FE
NC 302045

Description

The NCP302045 integrates a MOSFET driver, high-side MOSFET and low-side MOSFET into a single package.

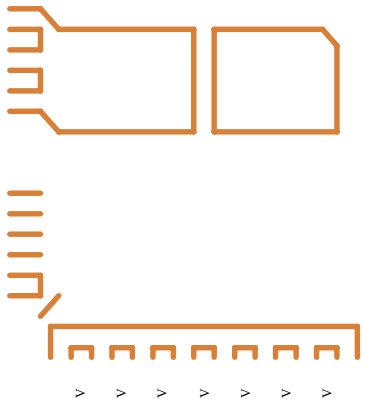
The driver and MOSFETs have been optimized for high-current DC−DC buck power conversion applications. The NCP302045 integrated solution greatly reduces package parasitics and board space compared to a discrete component solution.

Features

- Capable of Average Currents up to 45 A
- Capable of Switching at Frequencies up to 2 MHz
- Capable of Peak Currents up to 75 A
- Compatible with 3.3 V or 5 V PWM Input
- Responds Properly to 3-level PWM Inputs
- Option for Zero Cross Detection with 3-level PWM
- Internal Bootstrap Diode
- Undervoltage Lockout
-

MARKING DIAGRAM

PINOUT DIAGRAM



ORDERING INFORMATION

Device	Package	Shipping†
NCP302045MNTWG	PQFN31 (Pb−Free)	3000 / Tape & Reel

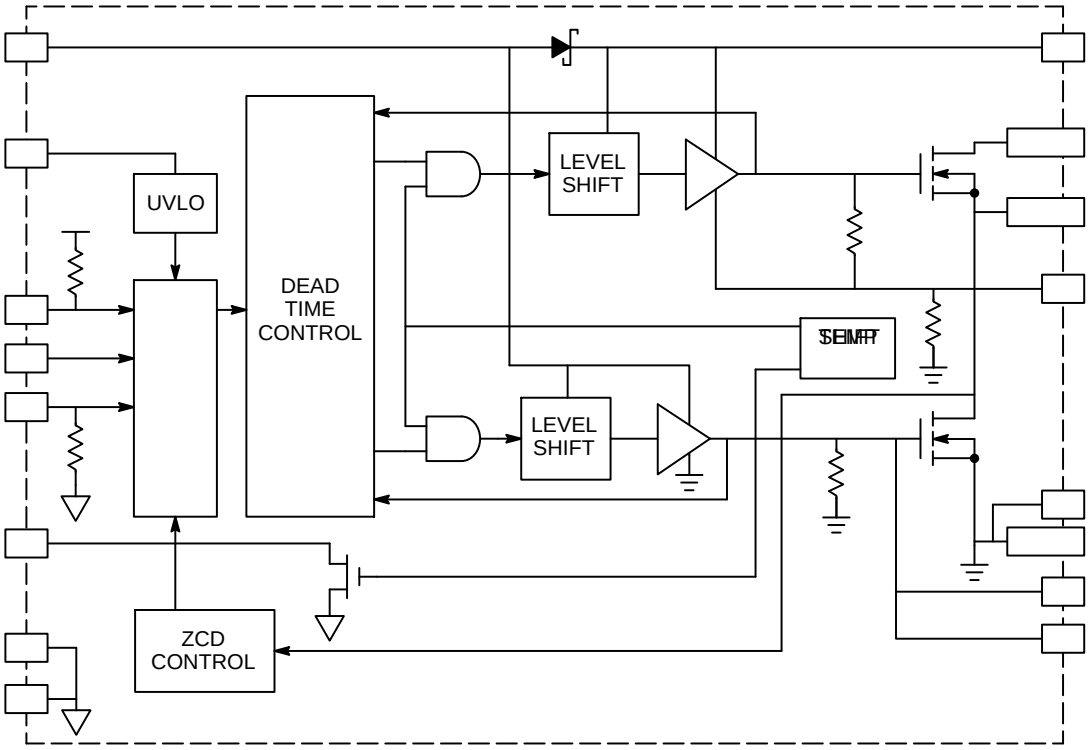


Figure 2. Block Diagram

Table 5. ELECTRICAL CHARACTERISTICS
(V_{VCC} = V_{VCCD} = 5.0 V, V_{VIN} = 12 V, $V_{DISB\#}$ = 2.0 V, C_{VCCD} = C_{VCC} = 0.1 μF unless specified otherwise) Min/Max values are valid for the temperature range −40°C ≤ T_J ≤ 125°C unless noted otherwise, and are guaranteed by test, design or statistical correlation.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
VCC SUPPLY CURRENT						
Operating		DISB# = 5 V, PWM = 400 kHz	−	1	2	mA
No switching		DISB# = 5 V, PWM = 0 V	−	−	2	mA
Disabled		DISB# = 0 V, SMOD# = VCC	−	0.4	1	μA
		DISB# = 0 V, SMOD# = GND	−	6	13	μA
UVLO Start Threshold	V_{UVLO}	VCC Rising	2.9	−	3.3	V
UVLO Hysteresis			150	−	−	mV
VCCD SUPPLY CURRENT						
Enabled, No Switching		DISB# = 5 V, PWM = 0 V, V_{PHASED} = 0 V	−	175	300	μA
Disabled		DISB# = 0 V	−	0.4	1	μA
Operating		DISB# = 5 V, PWM = 400 kHz	−	−	20	

Table 5. ELECTRICAL CHARACTERISTICS (continued)
(V_{VCC} = V_{VCCD} = 5.0 V, V_{VIN} = 12 V, $V_{DISB\#}$ = 2.0 V, C_{VCCD} = C_{VCC} = 0.1 μF unless specified otherwise) Min/Max values are valid for the temperature range −40°C ≤ T_J ≤ 125°C unless noted otherwise, and are guaranteed by test, design or statistical correlation.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
PWM INPUT						
Non-overlap Delay, Leading Edge	T_{NOL_L}	GL Falling = 1 V to GH−VSW Rising = 1 V	−	13	−	ns
Non-overlap Delay, Trailing Edge	T_{NOL_T}	GH−VSW Falling = 1 V to GL Rising = 1 V	−	12	−	ns
PWM Propagation Delay, Rising	T_{PWM,PD_R}	PWM = High to GL = 90%	−	13	35	ns
PWM Propagation Delay, Falling	T_{PWM,PD_F}	PWM = Low to VSW = 90%	−	52	78	ns
Exiting PWM Mid-state Propagation Delay, Mid-to-Low	$T_{PWM\_EXIT\_L}$	PWM = Mid-to-Low to GL = 10%	−	14	25	ns
Exiting PWM Mid-state Propagation Delay, Mid-to-High	$T_{PWM\_EXIT\_H}$	PWM = Mid-to-High to VSW = 10%	−	13	25	ns
ZCD FUNCTION						
Zero Cross Detect Threshold	V_{ZCD}		−	−6	−	mV
ZCD Blanking + Debounce Time	t_{BLNK}		−	330	−	ns
THERMAL WARNING & SHUTDOWN						
Thermal Warning Temperature	T_{THWN}	Temperature at Driver Die	−	150	−	°C
Thermal Warning Hysteresis	T_{THWN_HYS}		−	15	−	°C
Thermal Shutdown Temperature	T_{THDN}	Temperature at Driver Die	−	180	−	°C
Thermal Shutdown Hysteresis	T_{THDN_HYS}		−	25	−	°C
THWN Open Drain Current	I_{THWN}		−	−	5	mA
BOOSTSTRAP DIODE						
Forward Voltage		Forward Bias Current = 2.0 mA	−	380	−	mV
HIGH-SIDE DRIVER						
Output Impedance, Sourcing	R_{SOURCE_GH}	Source Current = 100 mA	−	0.9	−	Ω
Output Sourcing Peak Current	I_{SOURCE_GH}		−	2	−	A
Output Impedance, Sinking	R_{SINK_GH}	Sink Current = 100 mA	−	0.7	−	Ω
Output Sinking Peak Current	I_{SINK_GH}		−	2.5	−	A
LOW-SIDE DRIVER						
Output Impedance, Sourcing	R_{SOURCE_GL}	Source Current = 100 mA	−	0.9	−	Ω
Output Sourcing Peak Current	I_{SOURCE_GL}	GL = 2.5 V	−	2	−	A
Output Impedance, Sinking	R_{SINK_GL}	Sink Current = 100 mA	−	0.4	−	Ω
Output Sinking Peak Current	I_{SINK_GL}	GL = 2.5 V	−	4.5	−	A
GL Rise Time	T_{R_GL}	GL = 10% to 90%, C_{LOAD} = 3.0 nF				

APPLICATIONS INFORMATION

Theory of Operation

The NCP302045 is an integrated driver and MOSFET module designed for use in a synchronous buck converter topology. The NCP302045 supports numerous application control definitions including ZCD (Zero Current Detect) and alternately PWM Tristate control. A PWM input signal is required to control the drive signals to the high-side and low-side integrated MOSFETs.

Low-Side Driver

The low-side driver drives an internal, ground-referenced low-R_{DS}(on) N-Channel MOSFET. The voltage supply for the low-side driver is internally connected to the VCCD and PGND pins.

High-Side Driver

The high-side driver drives an internal, floating low-R_{DS}(on) N-channel MOSFET. The gate voltage for the high side driver is developed by a bootstrap circuit referenced to Switch Node (VSW and PHASE) pins.

The bootstrap circuit is comprised of the integrated diode and an external bootstrap capacitor and resistor. When the NCP302045 is starting up, the VSW pin is at ground, allowing the bootstrap capacitor to charge up to VCCD through the bootstrap diode (see Figure 1). When the PWM input is driven high, the high-side driver turns on the high-side MOSFET using the stored charge of the bootstrap capacitor. As the high-side MOSFET turns on, the voltage at the VSW and PHASE pins rises. When the high-side MOSFET is fully turned on, the switch node settles to VIN and the BST pin settles to VIN + VCCD (excluding parasitic ringing).

Bootstrap Circuit

The bootstrap circuit relies on an external charge storage capacitor (C_{BST}) and an integrated diode to provide current to the HS Driver. A multi-layer ceramic capacitor (MLCC) with a value greater than 100 nF should be used as the

bootstrap capacitor. An optional 1 to 4 Ω resistor in series with the bootstrap capacitor decreases the VSW overshoot.

Power Supply Decoupling

The NCP302045 sources relatively large currents into the MOSFET gates. In order to maintain a constant and stable supply voltage (VCCD) a low-ESR capacitor should be placed near the power and ground pins. A multi-layer ceramic capacitor (MLCC) between 1 μF and 4.7 μF is typically used.

A separate supply pin (VCC) is used to power the analog and digital circuits within the driver. A 1 μF ceramic capacitor should be placed on this pin in close proximity to the NCP302045. It is good practice to separate the VCC and VCCD decoupling capacitors with a resistor (10 Ω typical) to avoid coupling driver noise to the analog and digital circuits that control the driver function (see Figure 1).

Safety Timer and Overlap Protection Circuit

It is important to avoid cross-conduction of the two MOSFETS which could result in a decrease in the power conversion efficiency or damage to the device.

The NCP302045 prevents cross-conduction by monitoring the status of the MOSFETs and applying the appropriate amount of non-overlap (NOL) time (the time between the turn-off of one MOSFET and the turn-on of the other MOSFET). When the PWM input pin is driven high, the gate of the low-side MOSFET (LSGATE) goes low after a propagation delay (tpdlGL). The time it takes for the low-side MOSFET to turn off is dependent on the total charge on the low-side MOSFET gate.

The NCP302045 monitors the gate voltage of both MOSFETs and the switch node voltage to determine the conduction status of the MOSFETs. Once the low-side MOSFET is turned off an internal timer delays (tpdhGH) the turn-on of the high-side MOSFET. When the PWM input pin goes low, the gate of the high-side MOSFET (HSGATE) goes low after the propagation delay (tpdlGH). The time to turn off the high-side MOSFET (tfGH) is dependent on the total gate charge of the high-side MOSFET. A timer is triggered once the high-side MOSFET stops conducting, to delay (tpdhGL) the turn-on of the low-side MOSFET.

Zero Current Detect

The Zero Current Detect PWM (ZCD_PWM) mode is enabled when SMOD# is high (see Tables 6 and 8).

With PWM set to > VPWM_HI, GL goes low and GH goes high after the non-overlap delay. When PWM is driven to < VPWM_HI and to > VPWM_LO, GL goes high after the non-overlap delay, and stays high for the duration of the ZCD blanking timer (T_{ZCD_BLANK}) and an 80 ns de-bounce timer. Once this timer expires, VSW is monitored for zero current detection, and GL is pulled low once zero current is detected. The threshold on VSW to determine zero current undergoes an auto-calibration cycle every time DISB# is brought from low to high. This auto-calibration cycle typically takes 25 μs to complete.

PWM Input

The PWM Input pin is a tri-state input used to control the HS MOSFET ON/OFF state. It also determines the state of the LS MOSFET. See Table 6 for logic operation. The PWM in some cases must operate with frequency programming resistances to ground. These resistances can range from 10 kΩ to 300 kΩ depending on the application. When SMOD# is set to > VSMOD#_HI or to < VSMOD#_LO, the input impedance to the PWM input is very high in order to avoid interferences with controllers that must use programming resistances on the PWM pin.

If SMOD# is set to < VSMOD#_HI and > VSMOD#_LO (Mid-State), the PWM pin undriven default voltage is set to Mid-State with internal divider resistances.

Disable Input (DISB#)

The DISB# pin is used to disable the GH to the High-Side FET to prevent power transfer. The pin has a pull-down resistance to force a disabled state when it is left unconnected. DISB# can be driven from the output of a logic device or set high with a pull-up resistance to VCC.

VCC Undervoltage Lockout

The VCC pin is monitored by an Undervoltage Lockout Circuit (UVLO). VCC voltage above the rising threshold enables the NCP302045.

Table 7. UVLO/DISB# LOGIC TABLE

UVLO	DISB#	Driver State
L	X	Disabled (GH = GL = 0)
H	L	Disabled (GH = GL = 0)
H	H	Enabled (See Table 6)
H	Open	Disabled (GH = GL = 0)

Thermal Warning/Thermal Shutdown Output

The THWN pin is an open drain output. When the temperature of the driver exceeds T_{THWN}, the THWN pin is pulled low indicating a thermal warning. At this point, the part continues to function normally. When the temperature drops T_{THWN_HYS} below T_{THWN}, the THWN pin goes high. If the driver temperature exceeds T_{THDN}, the part enters thermal shutdown and turns off both MOSFETs. Once the temperature falls T_{THDN_HYS} below T_{THDN}, the part resumes normal operation.

Skip Mode Input (SMOD#)

The SMOD# tri-state input pin has an internal pull-up resistance to VCC. When driven low, the SMOD# pin enables the low side synchronous MOSFET to operate independently of the internal ZCD function. When the SMOD# pin is set low while PWM is in the mid-state, the low side MOSFET is disabled to allow discontinuous u d to allow d7 1

For Use with Controllers with 3-State PWM and No Zero Current Detection Capability:

For Use with Controllers with 3-state PWM and Zero Current Detection Capability:

Table 9. LOGIC TABLE 3-STATE PWM CONTROLLERS WITH ZCD

PWM	SMOD#	GH (Not a Pin)	GL
H	L	ON	OFF
M	L	OFF	OFF
L	L	OFF	ON

This section describes operation with controllers that are capable of 3 PWM output levels and have zero current detection during discontinuous conduction mode (DCM).

The SMOD# pin needs to be pulled low (below $V_{SMOD\#\_LO}$).

To operate the buck converter in continuous conduction mode (CCM), PWM needs to switch between the logic high and low states. During DCM, the controller is responsible for detecting when zero current has occurred, and then notifying the NCP302045 to turn off the LS FET. When the controller detects zero current, it needs to set PWM to mid-state, which causes the NCP302045 to pull both GH and GL to their off states without delay.

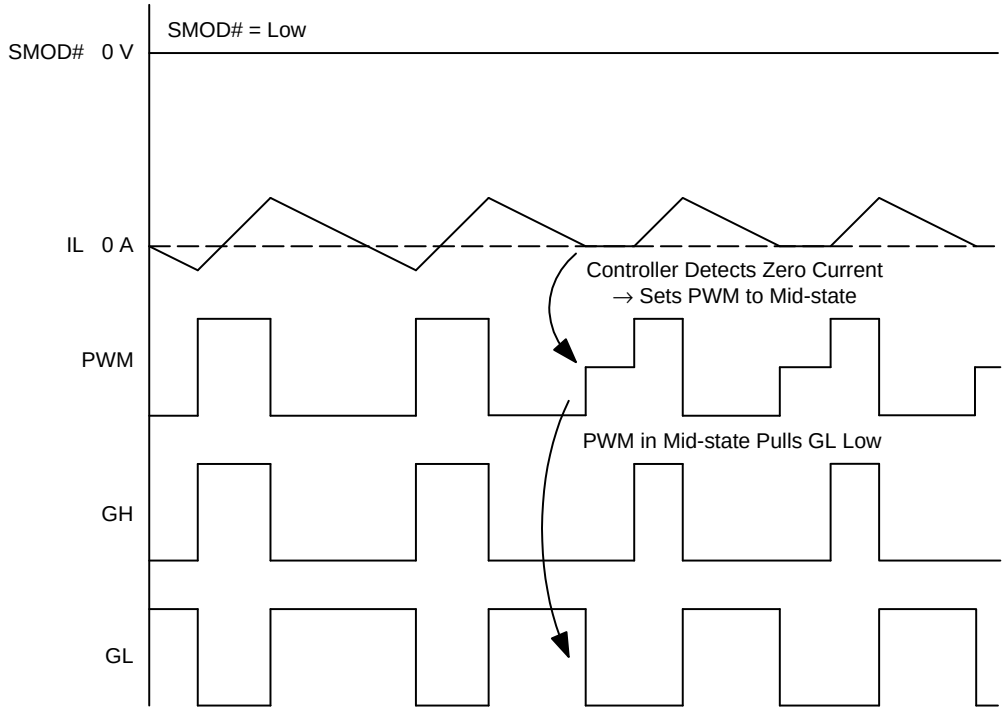


Figure 17. Timing Diagram 3-State PWM Controller, with ZCD

RECOMMENDED PCB LAYOUT

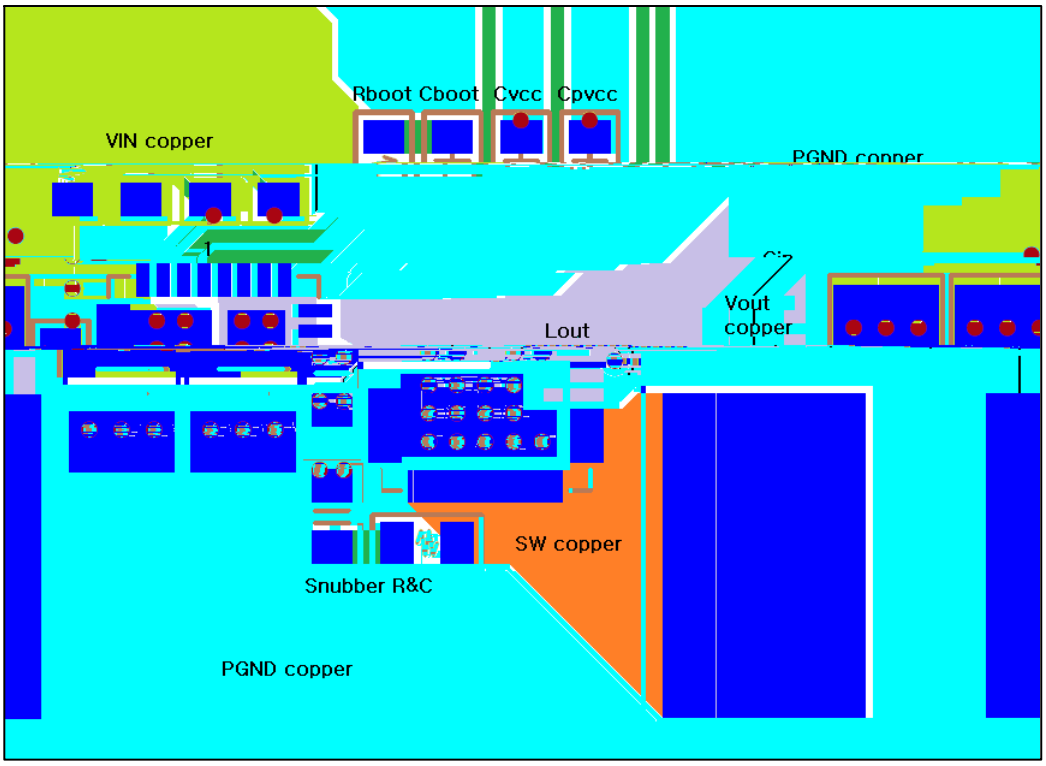


Figure 18. Top Copper Layer (Viewed from Top)

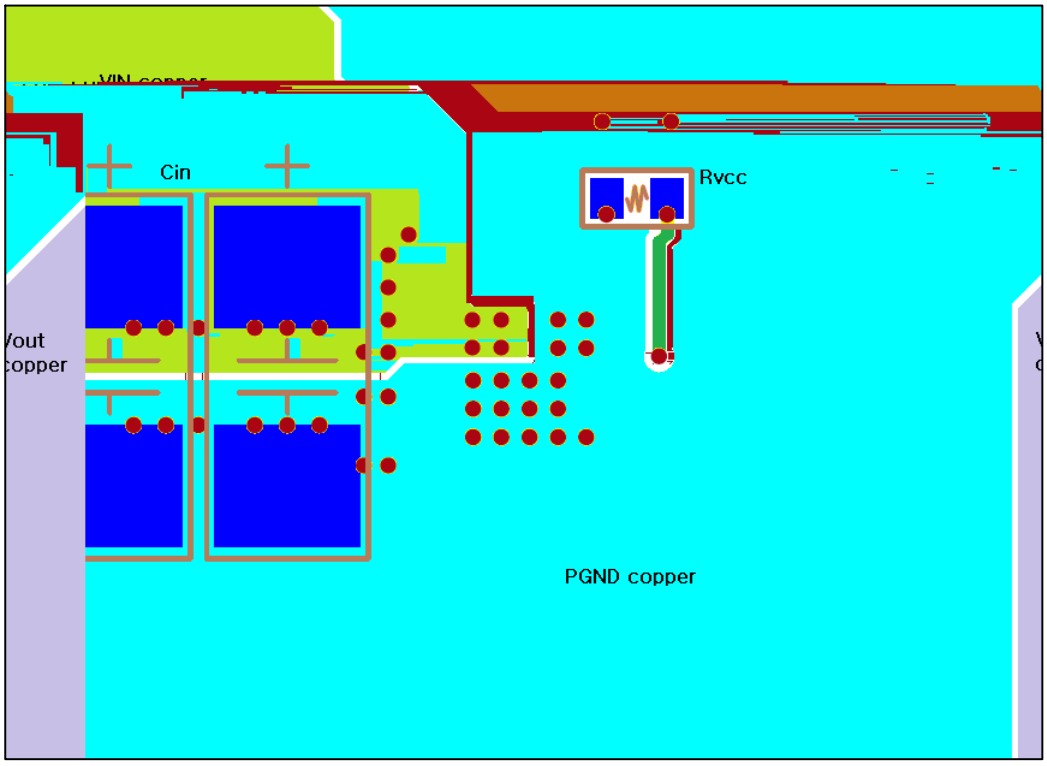
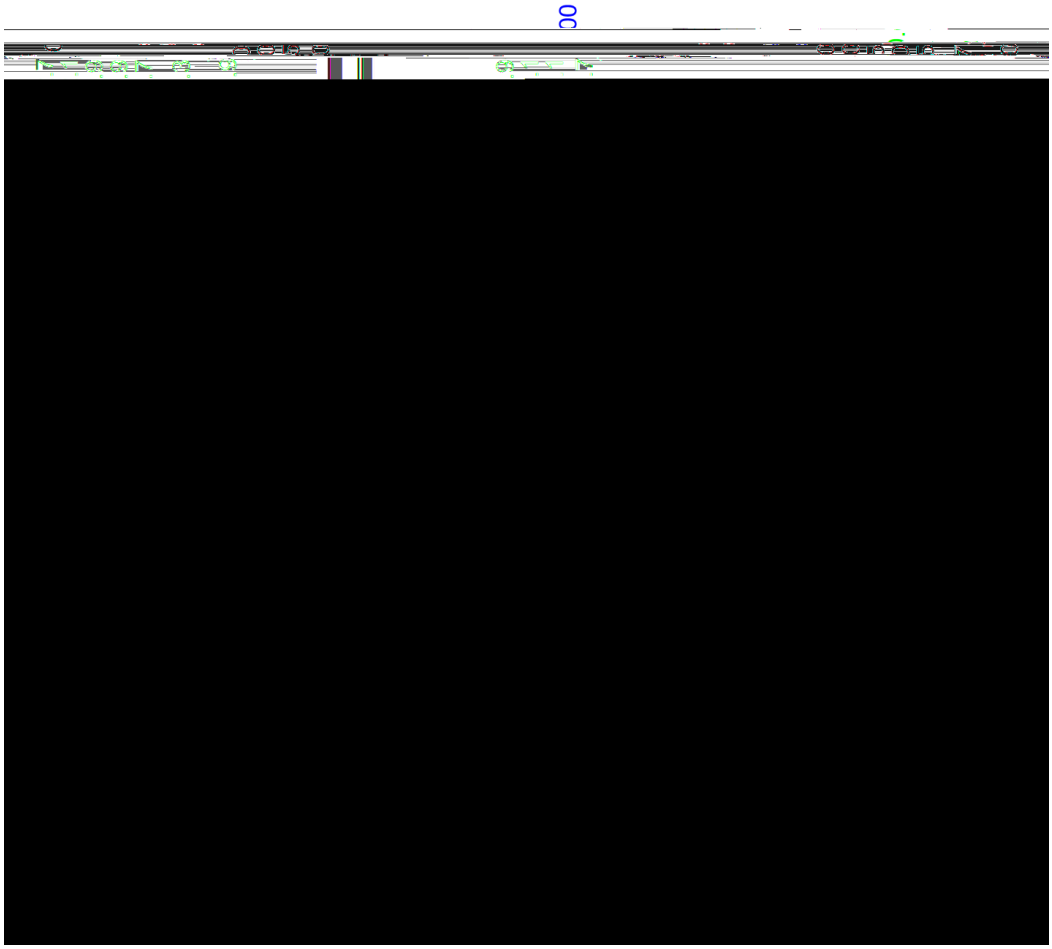


Figure 19. Bottom Copper Layer (Viewed from Top)

RECOMMENDED PCB FOOTPRINT (OPTION 1)

RECOMMENDED PCB FOOTPRINT (OPTION 2)

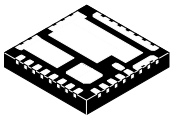


LAND PATTERN RECOMMENDATION

RECOMMENDED MOUNTING FOOTPRINT

For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

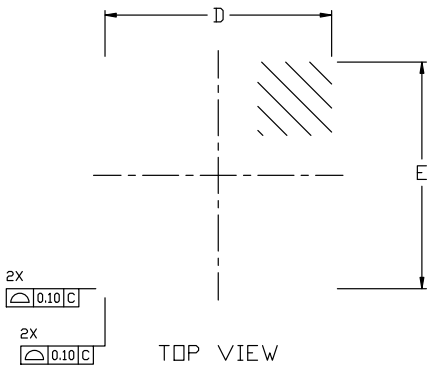
Figure 21. Recommended PCB Footprint (Option 2)



SCALE 2.5:1

PQFN31 5X5, 0.5P
CASE 483BR
ISSUE D

DATE 13 FEB 2023

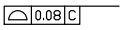


TOP VIEW

NOTES:

1. DOES NOT FULLY CONFORM TO JEDEC REGISTRATION MO-220.

SIDE VIEW



NOTE 4

SEATING PLANE

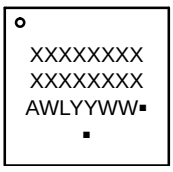
DETAIL 'A'
(SCALE 2:1)

PQFN31 5X5, 0.5P
CASE 483BR
ISSUE D

DATE 13 FEB 2023

RECOMMENDED MOUNTING FOOTPRINT*
(2X SCALE

GENERIC MARKING DIAGRAM*



XXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.