NCP302035

I D
MOSFET

Description

The NCP302035 integrates a MOSFET driver, high-side MOSFET and low-side MOSFET into a single package.

The driver and MOSFETs have been optimized for high-current DC−DC buck power conversion applications. The NCP302035 integrated solution greatly reduces package parasitics and board space compared to a discrete component solution.

Features

- Capable of Average Currents up to 35 A
- Capable of Switching at Frequencies up to 2 MHz
- Capable of Peak Currents up to 70 A
- Compatible with 3.3 V or 5 V PWM Input
- Responds Properly to 3-level PWM Inputs
- Option for Zero Cross Detection with 3-level PWM
- Internal Bootstrap Diode
- Undervoltage Lockout
- Supports Intel® Power State 4
- Thermal Warning output
- Thermal Shutdown

Applications

- Desktop & Notebook Microprocessors

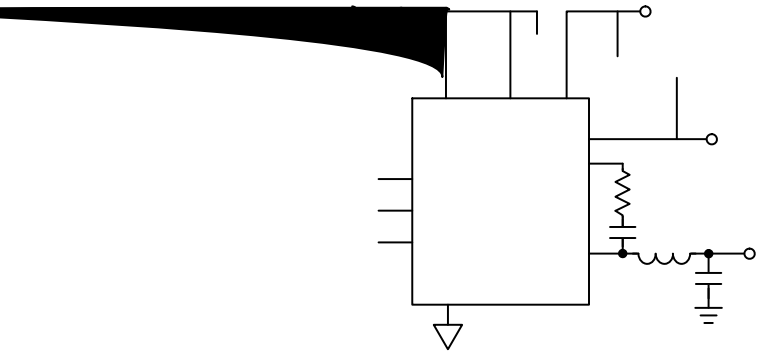

Figure 1. Application Schematic

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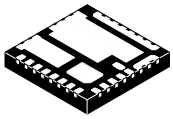

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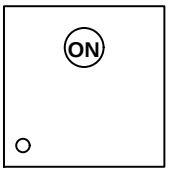
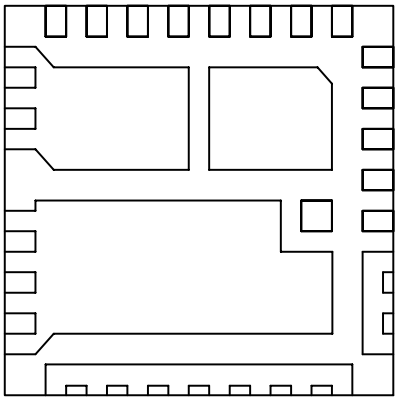
Case 483BR

MARKING DIAGRAM



PINOUT DIAGRAM



ORDERING INFORMATION

Device	Package	Shipping
	–	

Table 2. ABSOLUTE MAXIMUM RATINGS –

Pin Name/Parameter	Min	Max	Unit
	–		
	–		
	–		
	–		
	–		
	–		
	–		
	–		

Table 3. THERMAL INFORMATION

Rating	Symbol	Value	Unit
	θ		°
	θ –		°
		–	°
		–	°
		–	°

–
–

Table 4. RECOMMENDED OPERATING CONDITIONS

Parameter	Pin Name	Conditions	Min	Typ	Max	Unit
		°	–	–		
		°	–	–		
		°	–	–		
			–	–		°

Table 5. ELECTRICAL CHARACTERISTICS

Table 6. LOGIC TABLE

INPUT TRUTH TABLE				
DISB#	**PWM**	**SMOD#**	**GH (Not a Pin)**	**GL**

TYPICAL PERFORMANCE CHARACTERISTICS

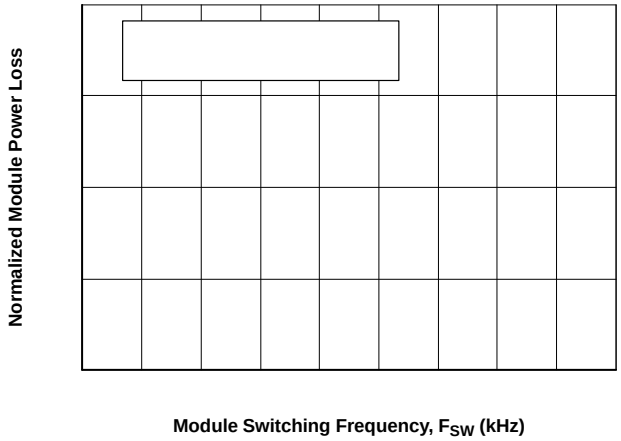


Figure 9. Power Loss vs. Switching Frequency

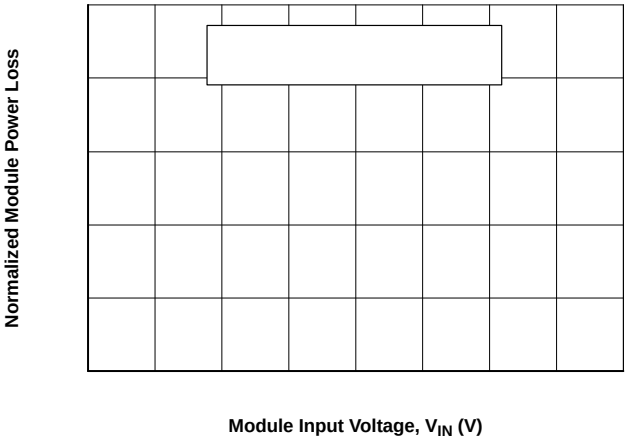


Figure 10. Power Loss vs. Input Voltage

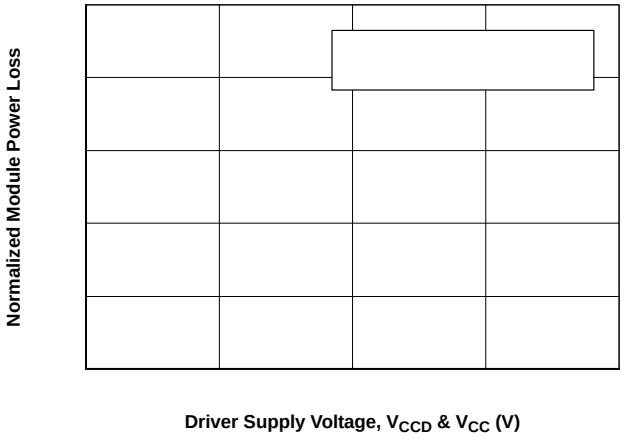


Figure 11. Power Loss vs. Driver Supply Voltage

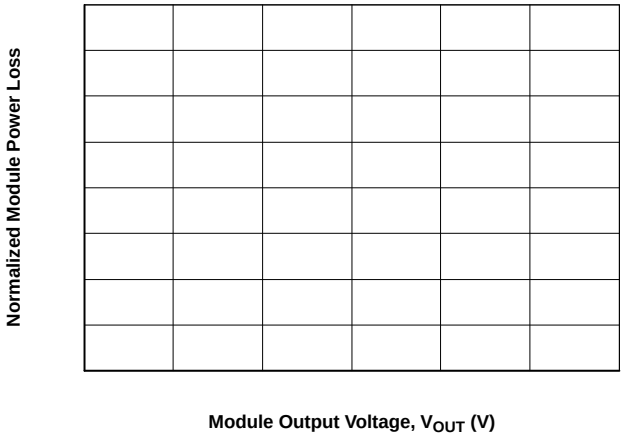


Figure 12. Power Loss vs. Output Voltage

Figure 13. Driver Supply Current vs. Switching Frequency

Figure 14. Driver Supply Current vs. Driver Supply Voltage

APPLICATIONS INFORMATION

Theory of Operation

The NCP302035 is an integrated driver and MOSFET module designed for use in a synchronous buck converter topology. The NCP302035 supports numerous application control definitions including ZCD (Zero Current Detect) and alternately PWM Tristate control. A PWM input signal is required to control the drive signals to the high-side and low-side integrated MOSFETs.

Low-Side Driver

The low-side driver drives an internal, ground-referenced low-R_{DS}(on) N-Channel MOSFET. The voltage supply for

Disable Input (DISB#)

The DISB# pin is used to disable the GH to the High-Side FET to prevent power transfer. The pin has a pull-down resistance to force a disabled state when it is left unconnected. DISB# can be driven from the output of a logic device or set high with a pull-up resistance to VCC.

VCC Undervoltage Lockout

The VCC pin is monitored by an Undervoltage Lockout Circuit (UVLO). VCC voltage above the rising threshold enables the NCP302035.

Table 7. UVLO/DISB# LOGIC TABLE

UVLO	DISB#	Driver State

For Use with Controllers with 3-State PWM and No Zero Current Detection Capability:

Table 8. LOGIC TABLE 3-STATE PWM CONTROLLERS WITH NO ZCD

PWM	SMOD#	GH (Not a Pin)	GL

This section describes operation with controllers that are capable of 3 states in their PWM output and relies on the NCP302035 to conduct zero current detection during discontinuous conduction mode (DCM).

The SMOD# pin needs to either be set to 5 V or left disconnected. The NCP302035 has an internal pull-up resistor that connects to VCC that sets SMOD# to the logic high state if this pin is disconnected.

To operate the buck converter in continuous conduction mode (CCM), PWM needs to switch between the logic high and low states. To enter into DCM, PWM needs to be switched to the mid-state.

Whenever PWM transitions to mid-state, GH turns off and GL turns on. GL stays on for the duration of the de-bounce timer and ZCD blanking timers. Once these timers expire, the NCP302035 monitors the VSW voltage and turns GL off when VSW exceeds the ZCD threshold voltage. By turning off the LS FET, the body diode of the LS FET allows any positive current to go to zero but prevents negative current from conducting.

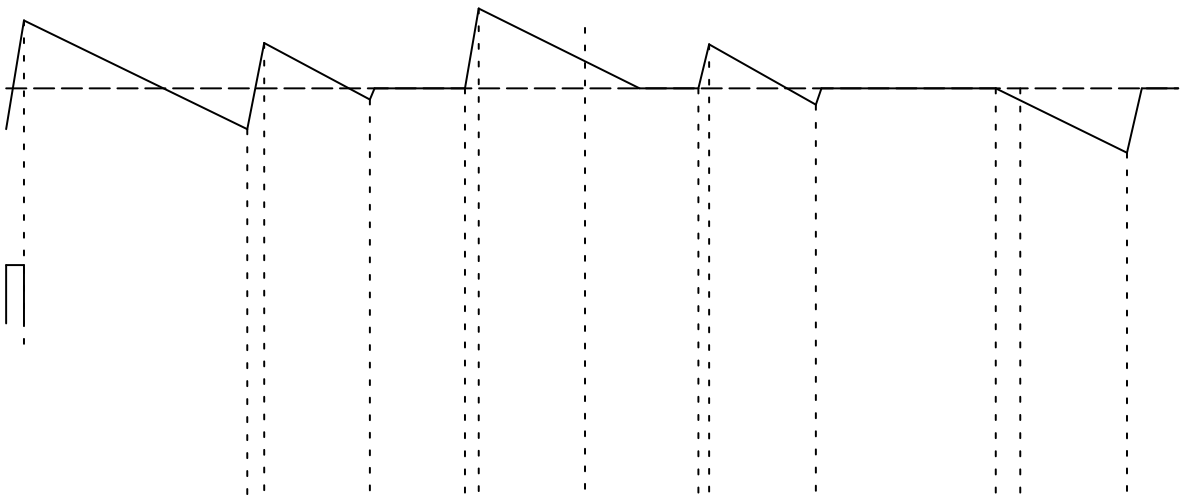


Figure 16. Timing Diagram 3-State PWM Controller, No ZCD

RECOMMENDED PCB LAYOUT

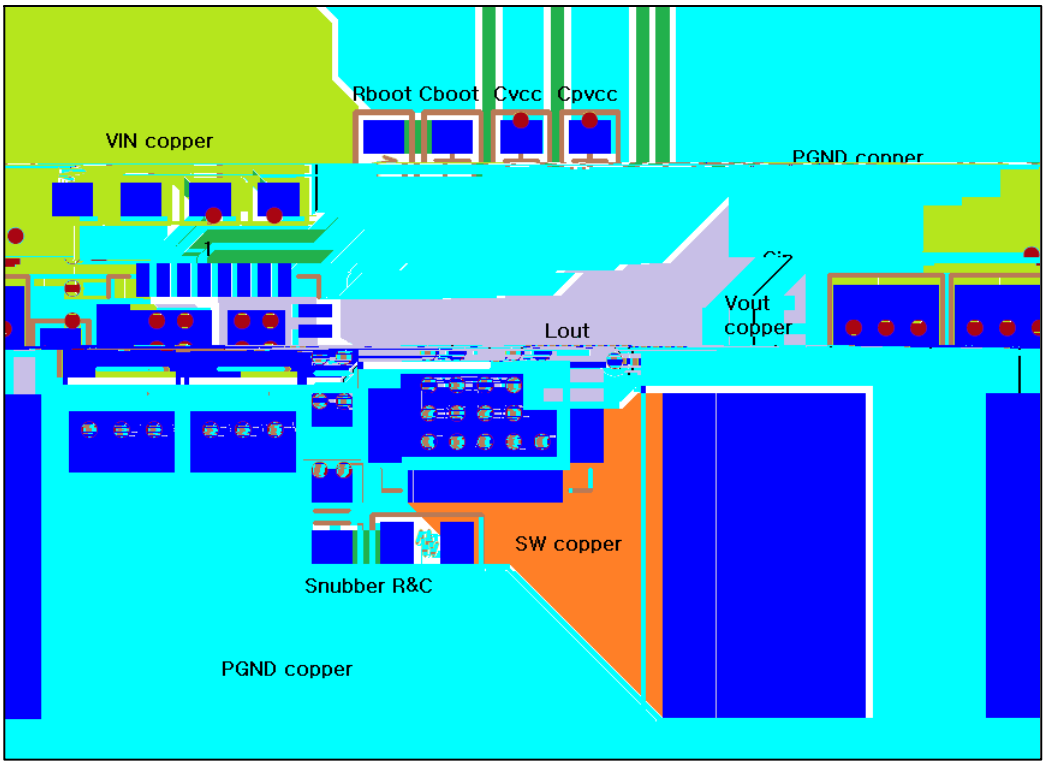


Figure 18. Top Copper Layer (Viewed from Top)

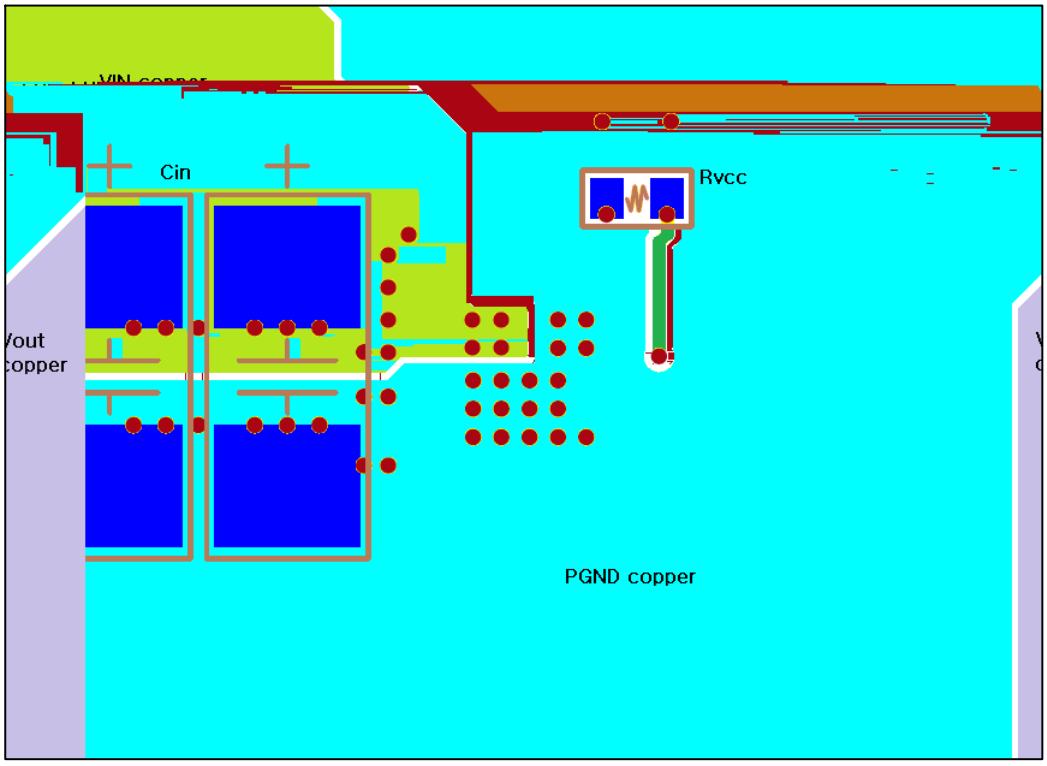


Figure 19. Bottom Copper Layer (Viewed from Top)

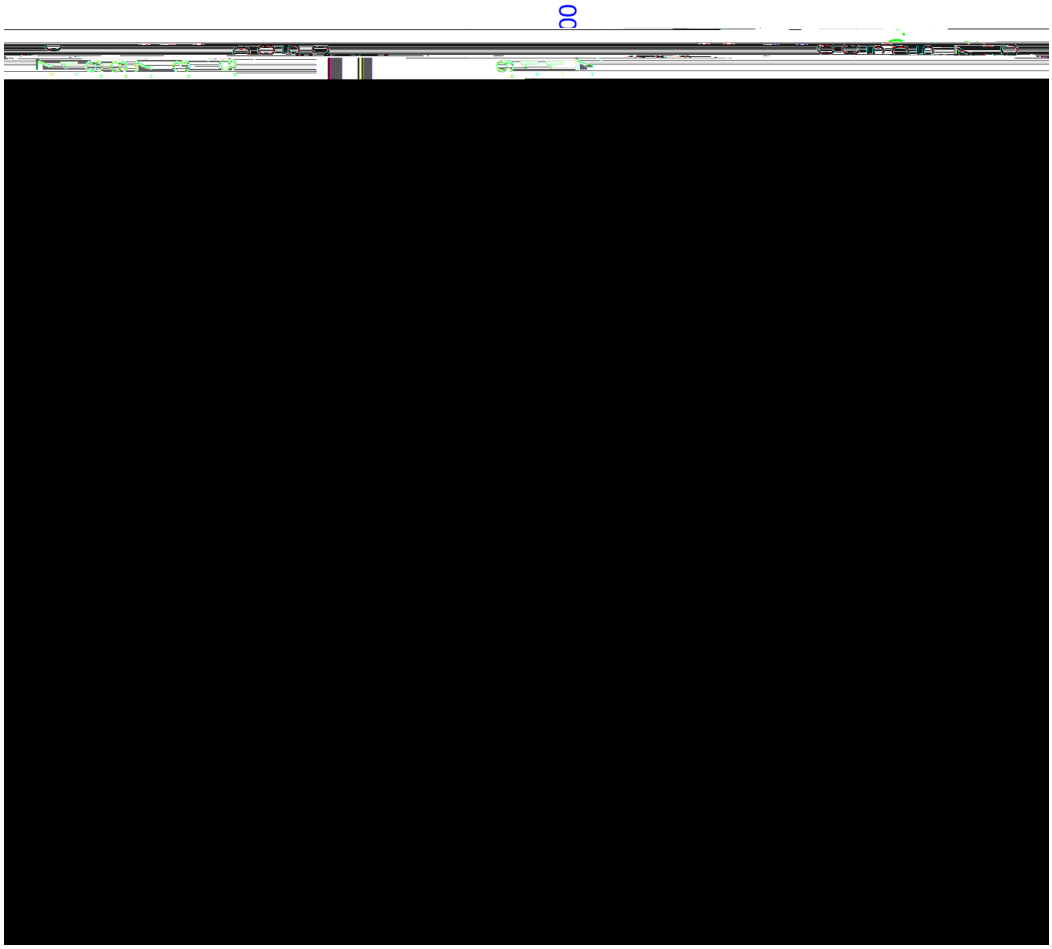
RECOMMENDED PCB FOOTPRINT (OPTION 1)

LAND PATTERN RECOMMENDATION

RECOMMENDED MOUNTING FOOTPRINT

Figure 20. Recommended PCB Footprint (Option 1)

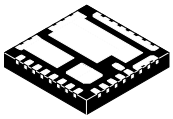
RECOMMENDED PCB FOOTPRINT (OPTION 2)



LAND PATTERN RECOMMENDATION

RECOMMENDED MOUNTING FOOTPRINT

Figure 21. Recommended PCB Footprint (Option 2)



SCALE 2.5:1

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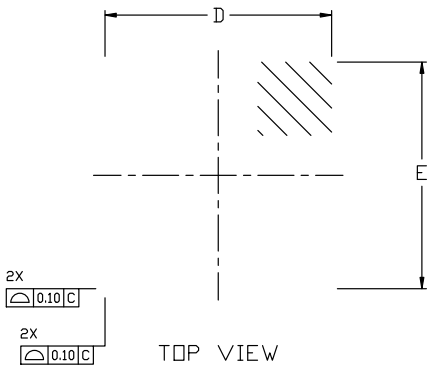
ISSUE D

DATE 13 FEB 2023

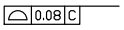


TOP VIEW

NOTES:

1. DOES NOT FULLY CONFORM TO JEDEC REGISTRATION MO-220.

SIDE VIEW



NOTE 4

SEATING PLANE

DETAIL 'A'
(SCALE 2:1)

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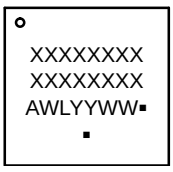
CASE 483BR
ISSUE D

DATE 13 FEB 2023

RECOMMENDED MOUNTING FOOTPRINT*
(2X SCALE

GENERIC MARKING DIAGRAM*



XXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.