I D MOSFET

Description

The NCP302035 integrates a MOSFET driver, high-side MOSFET and low-side MOSFET into a single package.

The driver and MOSFETs have been optimized for high-current DC–DC buck power conversion applications. The NCP302035 integrated solution greatly reduces package parasitics and board space compared to a discrete component solution.

Features

- Capable of Average Currents up to 35 A
- Capable of Switching at Frequencies up to 2 MHz
- Capable of Peak Currents up to 70 A
- Compatible with 3.3 V or 5 V PWM Input
- Responds Properly to 3-level PWM Inputs
- Option for Zero Cross Detection with 3-level PWM
- Internal Bootstrap Diode
- Undervoltage Lockout
- Supports Intel[®] Power State 4
- Thermal Warning output
- Thermal Shutdown

Applications

• Desktop & Notebook Microprocessors

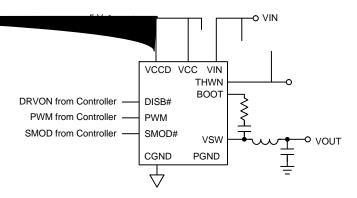


Figure 1. Application Schematic



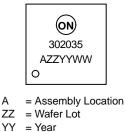
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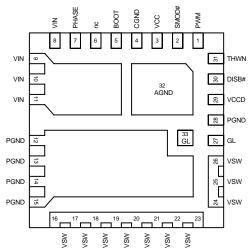
PQFN31 5x5, 0.5P Case 483BR

MARKING DIAGRAM



WW = Work Week





ORDERING INFORMATION

Device	Package	Shipping [†]
NCP302035MNTWG	PQFN31 (Pb–Free)	3000 / Tape & Reel

+For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

Pin Name/Parameter	Min	Мах	Unit
VCC, VCCD	-0.3	6.5	V
VIN	-0.3	30	V
BOOT (DC)	-0.3	35	V
BOOT (< 20 ns)	-0.3	40	V
BOOT to PHASE (DC)	-0.3	6.5	V
VSW, PHASE (DC)	-0.3	30	V
VSW, PHASE (< 5 ns)	-5	37	V
All Other Pins	-0.3	V _{VCC} + 0.3	V

Table 2. ABSOLUTE MAXIMUM RATINGS (Electrical Information – all signals referenced to PGND unless noted otherwise)

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

Table 3. THERMAL INFORMATION

Rating	Symbol	Value	Unit
Thermal Resistance (under ON Semiconductor SPS Thermal Board)	θ_{JA}	12.4	°C/W
	θ_{J-PCB}	1.8	°C/W
Operating Junction Temperature Range (Note 1)	TJ	-40 to +150	°C
Operating Ambient Temperature Range	T _A	-40 to +125	°C
Maximum Storage Temperature Range	T _{STG}	-55 to +150	°C
Maximum Power Dissipation		8.5	W
Moisture Sensitivity Level	MSL	1	

The maximum package power dissipation must be observed.
JESD 51–5 (1S2P Direct-Attach Method) with 0 LFM

3. JESD 51-7 (1S2P Direct-Attach Method) with 0 LFM

Table 4. RECOMMENDED OPERATING CONDITIONS

Parameter	Pin Name	Conditions	Min	Тур	Max	Unit
Supply Voltage Range	VCC, VCCD		4.5	5.0	5.5	V
Conversion Voltage	VIN		4.5	12	20	V
Continuous Output Current		F_{SW} = 1 MHz, V_{IN} = 12 V, V_{OUT} = 1.0 V, T_A = 25°C	-	-	30	А
		$F_{SW} = 300 \text{ kHz}, V_{IN} = 12 \text{ V}, V_{OUT} = 1.0 \text{ V}, T_A = 25^{\circ}\text{C}$	-	-	35	А
Peak Output Current		F_{SW} = 500 kHz, V_{IN} = 12 V, V_{OUT} = 1.0 V, Duration = 10 ms, Period = 1 s, T_A = 25°C	_	_	70	A
Junction Temperature			-40	-	125	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

Table 5. ELECTRICAL CHARACTERISTICS (continued)

 $(V_{VCC} = V_{VCCD} = 5.0 \text{ V}, V_{VIN} = 12 \text{ V}, V_{DISB\#} = 2.0 \text{ V}, \text{ C}$

Table 6. LOGIC TABLE

INPUT TRUTH TABLE				
DISB#	PWM	SMOD# (Note 4)	GH (Not a Pin)	GL
L	Х	Х	L	L
Н	Н	Х	Н	L
Н	L	Х	L	Н
Н	MID	H or MID	L	ZCD (Note 5)
Н	MID	L	L	L (Note 6)

PWM input is driven to mid-state with internal divider resistors when SMOD# is driven to mid-state and PWM input is undriven externally.
GL goes low following 80 ns de-bounce time, 250 ns blanking time and then SW exceeding ZCD threshold.
There is no delay before GL goes low.

TYPICAL PERFORMANCE CHARACTERISTICS

(Test Conditions: $V_{IN} = 12 \text{ V}$, $V_{CC} = PV_{CC} = 5 \text{ V}$, $V_{OUT} = 1 \text{ V}$, $L_{OUT} = 250 \text{ nH}$, $T_A = 25^{\circ}C$ and natural convection cooling, unless otherwise noted.)

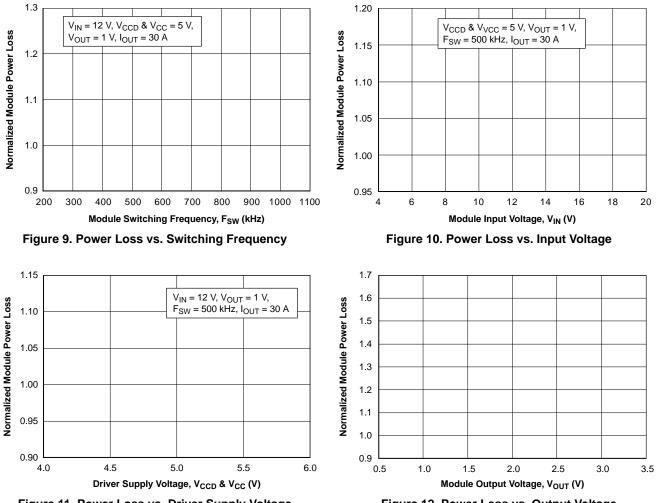


Figure 11. Power Loss vs. Driver Supply Voltage

Figure 12. Power Loss vs. Output Voltage

Figure 13. Driver Supply Current vs. Switching Frequency Figure 14. Driver Supply Current vs. Driver Supply Voltage

APPLICATIONS INFORMATION

Theory of Operation

The NCP302035 is an integrated driver and MOSFET module designed for use in a synchronous buck converter topology. The NCP302035 supports numerous application control definitions including ZCD (Zero Current Detect) and alternately PWM Tristate control. A PWM input signal is required to control the drive signals to the high-side and low-side integrated MOSFETs.

Low-Side Driver

The low-side driver drives an internal, ground-referenced low- $R_{DS}(on)$ N-Channel MOSFET. The voltage supply for

Disable Input (DISB#)

The DISB# pin is used to disable the GH to the High-Side FET to prevent power transfer. The pin has a pull-down resistance to force a disabled state when it is left unconnected. DISB# can be driven from the output of a logic device or set high with a pull-up resistance to VCC.

VCC Undervoltage Lockout

The VCC pin is monitored by an Undervoltage Lockout Circuit (UVLO). VCC voltage above the rising threshold enables the NCP302035.

Table 7. UVLO/DISB# LOGIC TABLE

UVLO	DISB#	Driver State
L	X Disabled (GH = GL = 0	
Н	L	Disabled (GH = GL = 0)
Н	Н	Enabled (See Table 6)
Н	Open	Disabled (GH = GL = 0)

For Use with Controllers with 3-State PWM and No Zero Current Detection Capability:

PWM	SMOD#	GH (Not a Pin)	GL
Н	Н	ON	OFF
М	Н	OFF	ZCD
L	Н	OFF	ON

Table 8. LOGIC TABLE 3-STATE PWM CONTROLLERS WITH NO ZCD

This section describes operation with controllers that are capable of 3 states in their PWM output and relies on the NCP302035 to conduct zero current detection during discontinuous conduction mode (DCM).

The SMOD# pin needs to either be set to 5 V or left disconnected. The NCP302035 has an internal pull-up resistor that connects to VCC that sets SMOD# to the logic high state if this pin is disconnected.

To operate the buck converter in continuous conduction mode (CCM), PWM needs to switch between the logic high

and low states. To enter into DCM, PWM needs to be switched to the mid-state.

Whenever PWM transitions to mid-state, GH turns off and GL turns on. GL stays on for the duration of the de-bounce timer and ZCD blanking timers. Once these timers expire, the NCP302035 monitors the VSW voltage and turns GL off when VSW exceeds the ZCD threshold voltage. By turning off the LS FET, the body diode of the LS FET allows any positive current to go to zero but prevents negative current from conducting.

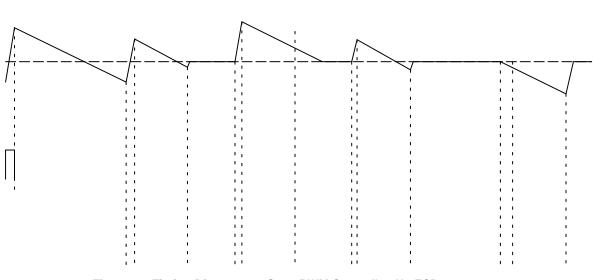


Figure 16. Timing Diagram 3-State PWM Controller, No ZCD

RECOMMENDED PCB LAYOUT

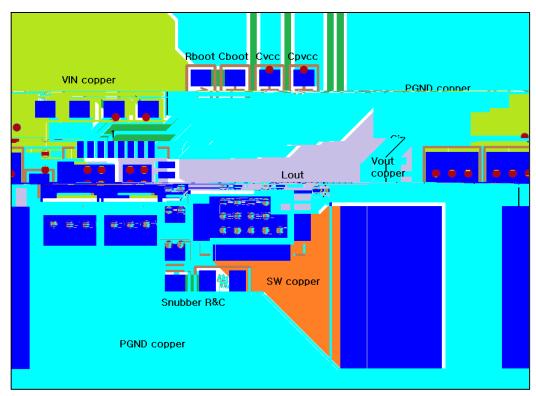


Figure 18. Top Copper Layer (Viewed from Top)

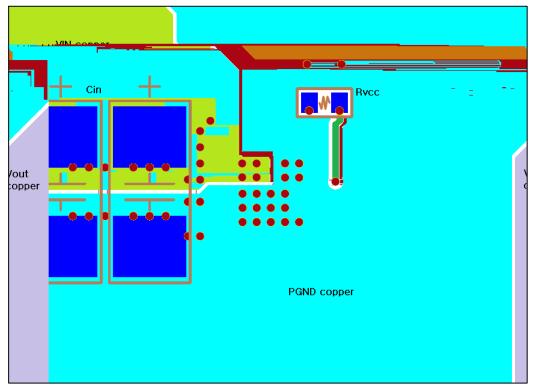


Figure 19. Bottom Copper Layer (Viewed from Top)

RECOMMENDED PCB FOOTPRINT (OPTION 1)

LAND PATTERN RECOMMENDATION

RECOMMENDED MOUNTING FOOTPRINT

For additional information on our Pb-Free strategy and soldering

Figure 20. Recommended PCB Footprint (Option 1)

RECOMMENDED PCB FOOTPRINT (OPTION 2)



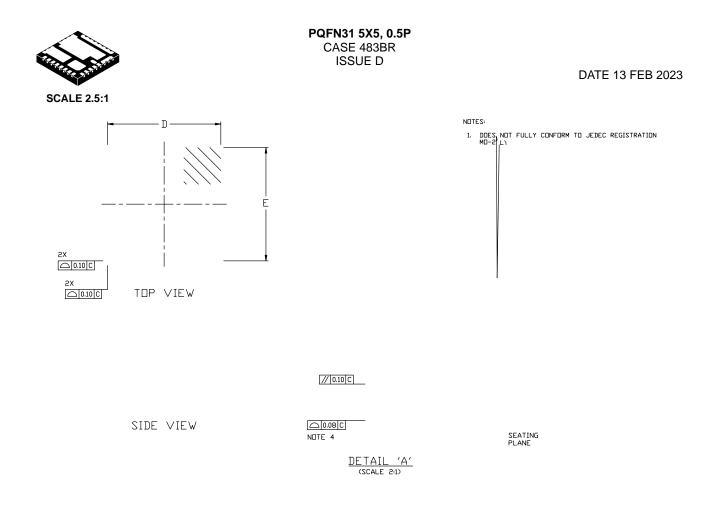
LAND PATTERN RECOMMENDATION

RECOMMENDED MOUNTING FOOTPRINT

For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

Figure 21. Recommended PCB Footprint (Option 2)

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PQFN31 5X5, 0.5P CASE 483BR ISSUE D

DATE 13 FEB 2023

RECOMMENDED MOUNTING FOOTPRINT* (2X SCALE

GENERIC MARKING DIAGRAM*

o XXXXXXXX XXXXXXXX AWLYYWW• XXXX = Specific Device Code A = Assembly Location

WL = Wafer Lot

YY = Year

WW = Work Week

= Pb–Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb–Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.

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