NCP2823 Series

The NCP2823A/B are cost effective mono audio power amplifiers designed for portable electronic devices. NCP2823A is optimized for 8 operation and NCP2823B can operate with speaker impedance down to 4.0 . For Instance, NCP2823B is capable of delivering 3 W of continuous average power to a 4.0 from a 5.0 V supply in a Bridge Tied Load (BTL) configuration. Under the same conditions, NCP2823A can provide 1.5 W to an 8.0 BTL load with less than 10% THD+N. For cellular handsets or PDAs it offers space and cost savings because no output filter is required when using inductive transducers. With more than 90% efficiency and very low shutdown current, it increases the lifetime of your battery and drastically lowers the junction temperature.

NCP2823 processes analog inputs with a pulse width modulation technique that lowers output noise and THD. The device allows independent gain while summing signals from various audio sources. Thus, in cellular handsets, the earpiece, the loudspeaker and even melody ringer can be driven with a single NCP2823. Due to its low 26 V noise floor, A−weighted, clean listening is guaranteed no matter the load sensitivity.

Features

- Optimized PWM Output Stage: Filterless Capability
- Externally gain setting
- Low consumption: 1.8 mA for NCP2823A
- High efficiency: up to 92%

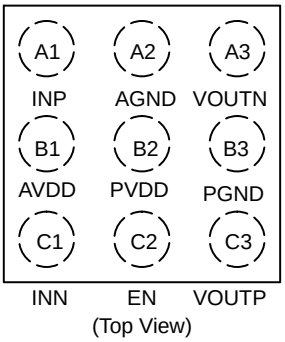


Figure 1. Pin Description

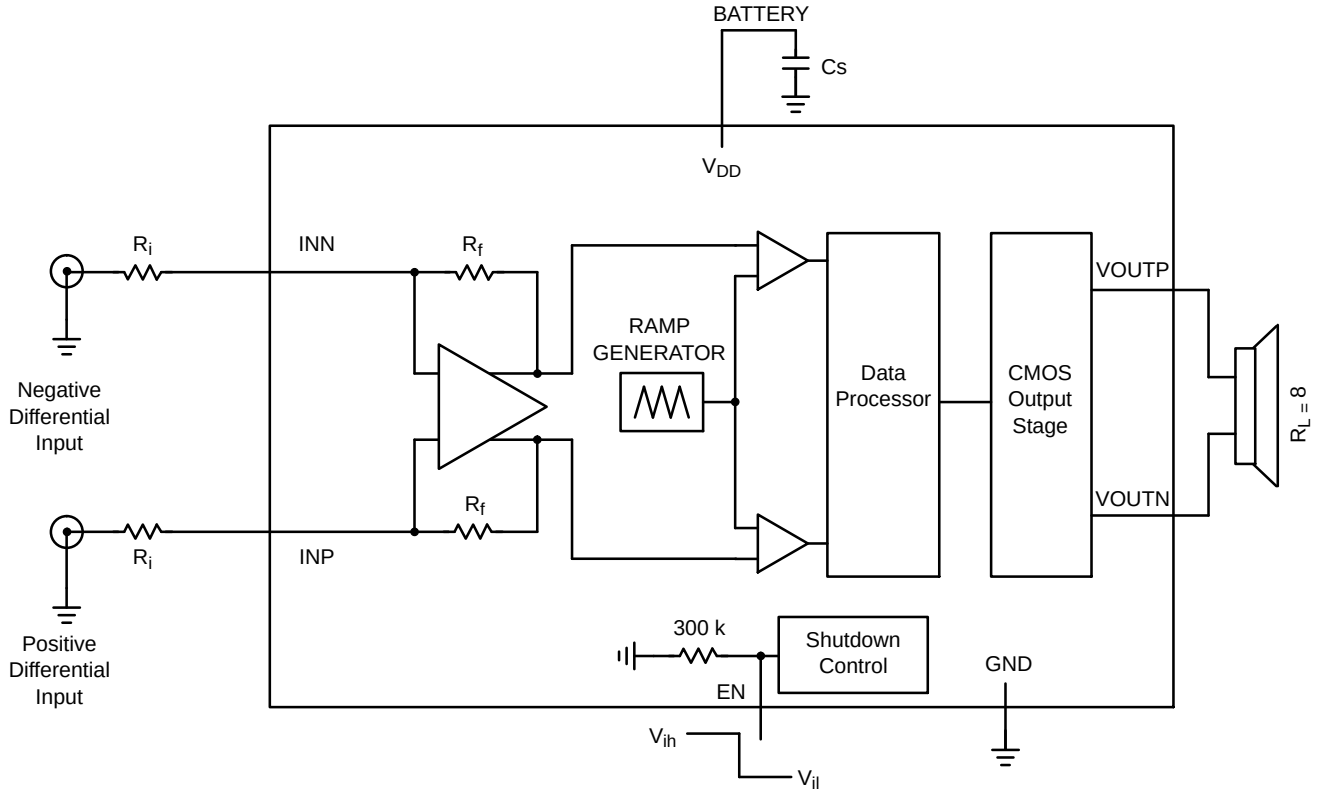


Figure 2. Simplified Block Diagram

PIN FUNCTION DESCRIPTION

Pin	Pin Name	Type	Description
A1			

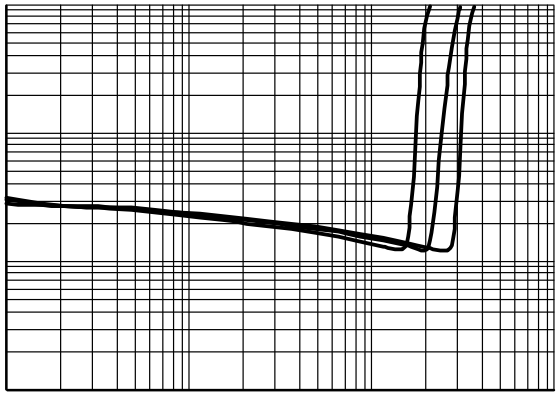
n and Max Limits apply for T_A between −40°C to +85°C and for V_{DD} between 2.5 V to 5.5 V referenced to T_A = + 25 °C and V_{DD} = 3.6 V. (see Note 8)

Conditions		Min	Typ	Max	Unit
		2.5		5.5	V
		250	300	350	kHz
NCP2823A V_P = 3.6 V, No Load NCP2823B V_P = 3.6 V, No Load			1.8 2.6	2.4 4.6	mA
V_{ENL} = V_{ENR} = 0 V			0.01	1	A
EN rising edge			7.4		ms
EN falling edge			4		ms
V_{ENL} = 0 V			20		k
			300		m
NCP2823A, V_P = 3.6 V, Po = 600 mW, RL = 8 , F = 1 kHz			92		%
NCP2823B, V_P = 3.6 V, Po = 1 W, RL = 4 , F = 1 kHz			90		
		285 k Ri	300 k Ri	315 k Ri	V/V
			30		kHz
			150		°C
			10		°C
		1.2	−	V_{DD}	V
			−	0.4	V
			250		k
			0.3		mV
F = 217 Hz, Input ac grounded			−77		dB
F = 1 kHz, Input ac grounded			−63		
V_P = 5 V, Pout = 600 mW (A. Weighted)			97		dB
Input shorted together V_{IC} = 1 V_{pp}, f = 217 Hz			−80		dB
Input ac grounded, Av = 0 dB	No weighting		35		V
	A. Weighted		26		

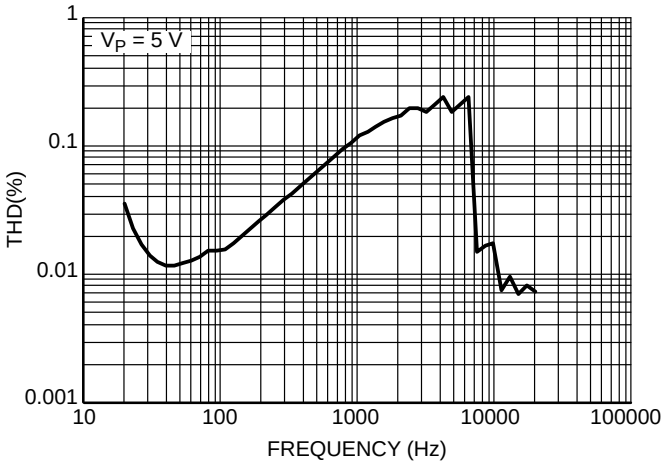
ELECTRICAL CHARACTERISTICS Min and Max Limits apply for T_A between −40°C to +85°C and for V_{DD} between 2.5 V to 5.5 V (Unless otherwise noted). Typical values are referenced to T_A = + 25 °C and V_{DD} = 3.6 V. (see Note 8)

Symbol	Parameter	Conditions			Min	Typ	Max	Unit
AUDIO PERFORMANCES								
Po	Output Power	NCP2823A RL = 8 F = 1 kHz	THD+N < 1%	V_P = 5 V		1.5		W
				V_P = 3.6 V		0.7		
				V_P = 2.5 V		0.22		
			THD+N < 10%	V_P = 5 V		1.8		
				V_P = 3.6 V		0.87		
				V_P = 2.5 V		0.4		
		NCP2823B RL = 4 F = 1 kHz	THD+N < 1%	V_P = 5 V		1.72		
				V_P = 3.6 V		1.2		
				V_P = 2.5 V		0.58		
			THD+N < 10%	V_P = 5 V				

TYPICAL OPERATING CHARACTERISTICS



TYPICAL OPERATING CHARACTERISTICS



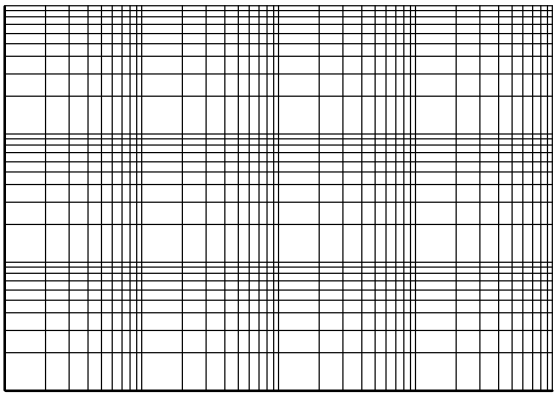


Figure 9. THD+N vs Frequency P_{out} = 1 W, R_L = 8 Ω

DETAIL OPERATING DESCRIPTION

General Description

The basic structure of the NCP2823A/B is composed of one analog pre−amplifier, a pulse width modulator and an H−bridge CMOS power stage. The first stage is externally configurable with gain−setting resistor Ri and the internal fixed feedback resistor Rf (the closed−loop gain is fixed by the ratios of these resistors). The load is driven differentially through two output stages. The differential PWM output signal is a digital image of the analog audio input signal. The human ear is a band pass filter regarding acoustic waveforms, which the typical cut off values are 20 Hz and 20 kHz. Thus, the user will hear only the amplified audio input signal within the frequency range. The switching frequency and its harmonics are fully filtered. The inductive parasitic element of the loudspeaker helps to guarantee a superior distortion value.

Power Amplifier

The output PMOS and NMOS transistors of the amplifier have been designed to deliver a maximum output power before clipping. The channel resistance (Ron) of the NMOS and PMOS transistors is typically 0.3 .

Gain Selection

The preamplifier stage amplifies the input signal. The gain is fully configurable by external resistors.

The gain setting is given by the following equation:

$$Av = \frac{300\ k}{Ri} \qquad \text{(eq. 1)}$$

Turn On and Turn Off Transitions

In order to reduce “pop and click” noises during transition, the output power in the load must not be established or cutoff suddenly. When logic high is applied to the Enable pin, the internal biasing voltage rises quickly and, 4 ms later, once the output DC level is around the common mode voltage, the gain is established slowly (5.0 ms). Thus, the total turn on time to get full power to the load is 7.4 ms (typical). The device has the same behavior when it is turned−off by a logic low on the Enable pin. No power is delivered to the load 4 ms after a falling edge on the shutdown pin. Due to the fast turn on and off times, the shutdown signal can be used as a mute signal as well.

Shutdown Function

The device enters shutdown mode when the Enable signal is low. During the shutdown mode, the DC Shutdown current of the circuit does not exceed 1 A.

The NCP2823A/B has an internal resistor (R_{PLD} = 250 k) connected between GND and Enable. The purpose of this resistor is to eliminate any unwanted state changes when the Enable pin is floating.

30 kHz Built−in Low Pass Filter

This filter allows connecting directly a DAC or a CODEC to the NCP2823 input without increasing the output noise by mixing frequency with the DAC/CODEC output frequency. Consequently, optimized operation with DACs or CODECs is guaranteed without additional external components.

Power Supply Bypassing

The NCP2823 requires a correct decoupling of the power supply in order to guarantee the best operation in terms of audio performances. To achieve these performances, it is necessary to place a 4.7 F low ESR ceramic capacitor as close as possible to the PVDD pin in order to reduce high frequency transient spikes due to parasitic inductance (see Layout considerations).

Input Capacitors C_{in}

Thanks to its fully differential architecture the NCP2823 does not require input capacitors. However, it is possible to use input capacitors when the differential source is not biased or in single ended configuration. In this case it is necessary to taktypicTm.00rforTe a17us9requency ran TmMOS and N3e

The EMI Level is strongly dependent upon the application. However, ferrite beads placed close to the NCP2823 will reduce EMI radiation when it is needed.

Ferrite value is strongly dependent upon the application.

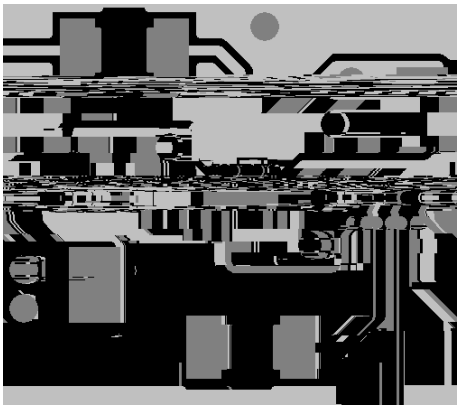


Figure 18. PCB Layout example

ORDERING INFORMATION

Device	Package	Shipping†
NCP2823AFCT2G	WLCSP9 (Pb−Free)	3000 / Tape & Reel
NCP2823AFCCT2G	WLCSP9 (Backside Laminate Coating) (Pb−Free)	

9 PIN FLIP CHIP 1.45x1.45x0.596

b-Free
strategy and soldering details, please do▮nloa
the