NCP2820 Series

2.65 W Filterless Class-D Audio Power Amplifier

The NCP2820 is a cost effective mono Class D audio power amplifier capable of delivering 2.65 W of continuous average power to 4.0 from a 5.0 V supply in a Bridge Tied Load (BTL) configuration. Under the same conditions, the output power stage can provide 1.4 W to a 8.0 BTL load with less than 1% THD+N. For cellular handsets or PDAs it offers space and cost savings because no output filter is required when using inductive tranducers. With more than 90% efficiency and very low shutdown current, it increases the lifetime of your battery and drastically lowers the junction temperature.

The NCP2820 processes analog inputs with a pulse width modulation technique that lowers output noise and THD when compared to a conventional sigma delta modulator. The device allows independent gain while summing signals from various audio sources. Thus, in cellular handsets, the earpiece, the loudspeaker and even the melody ringer can be driven with a single NCP2820. Due to its low 42 V noise floor, A weighted, a clean listening is guaranteed no matter the load sensitivity. With zero pop and click noise performance NCP2820A turns on within 1 ms versus 9 ms for NCP2820 version.

Features

- Optimized PWM Output Stage: Filterless Capability
- Efficiency up to 90%
  Low 2.5 mA Typical Quiescent Current
- Large Output Power Capability: 1.4 W with 8.0 Load (CSP) and THD + N < 1%
- Ultra Fast Start up Time: 1 ms for NCP2820A Version
- High Performance, THD+N of 0.03% @ V_p = 5.0 V,
  R_L = 8.0 , P_{out} = 100 mW
- Excellent PSRR (65 dB): No Need for Voltage Regulation
- Surface Mounted Package 9 Pin Flip Chip CSPand UDFN8
- Fully Differential Design. Eliminates Two Input Coupling Capacitors
- Very Fast Turn On/Off Times with Advanced Rising and Falling Gain Technique
- External Gain Configuration Capability
- Internally Generated 250 kHz Switching Frequency
- “Pop and Click” Noise Protection Circuitry
- NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC Q100 Qualified and PPAP Capable
- These are Pb Free Devices

Applications

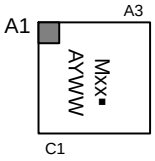
- Cellular Phone
- Portable Electronic Devices
- PDAs and Smart Phones
- Portable Computer

http://onsemi.com

MARKING DIAGRAMS

1

9 PIN FLIP CHIP CSP
FC SUFFIX
CASE 499AL



8

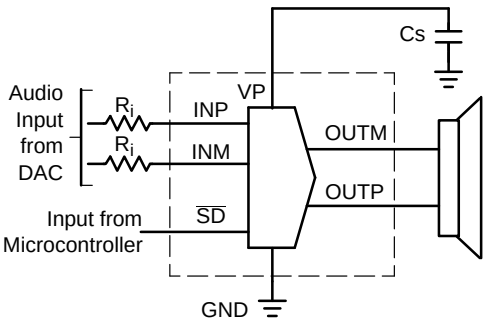
1

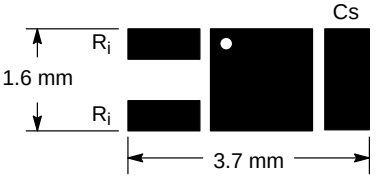
8 PIN UDFN 2x2.2
MU SUFFIX
CASE 506AV

xx = ZB for NCP2820
= AT for NCV2820
M = Date Code
▪ = Pb−Free Package

ORDERING INFORMATION

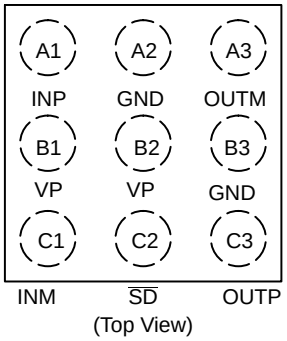
See detailed ordering and shipping information on page 19 of this data sheet.





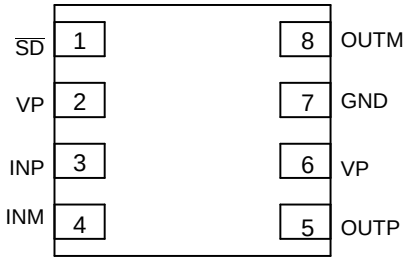
PIN CONNECTIONS

9 Pin Flip Chip CSP



(Top View)

UDFN8



(Top View)

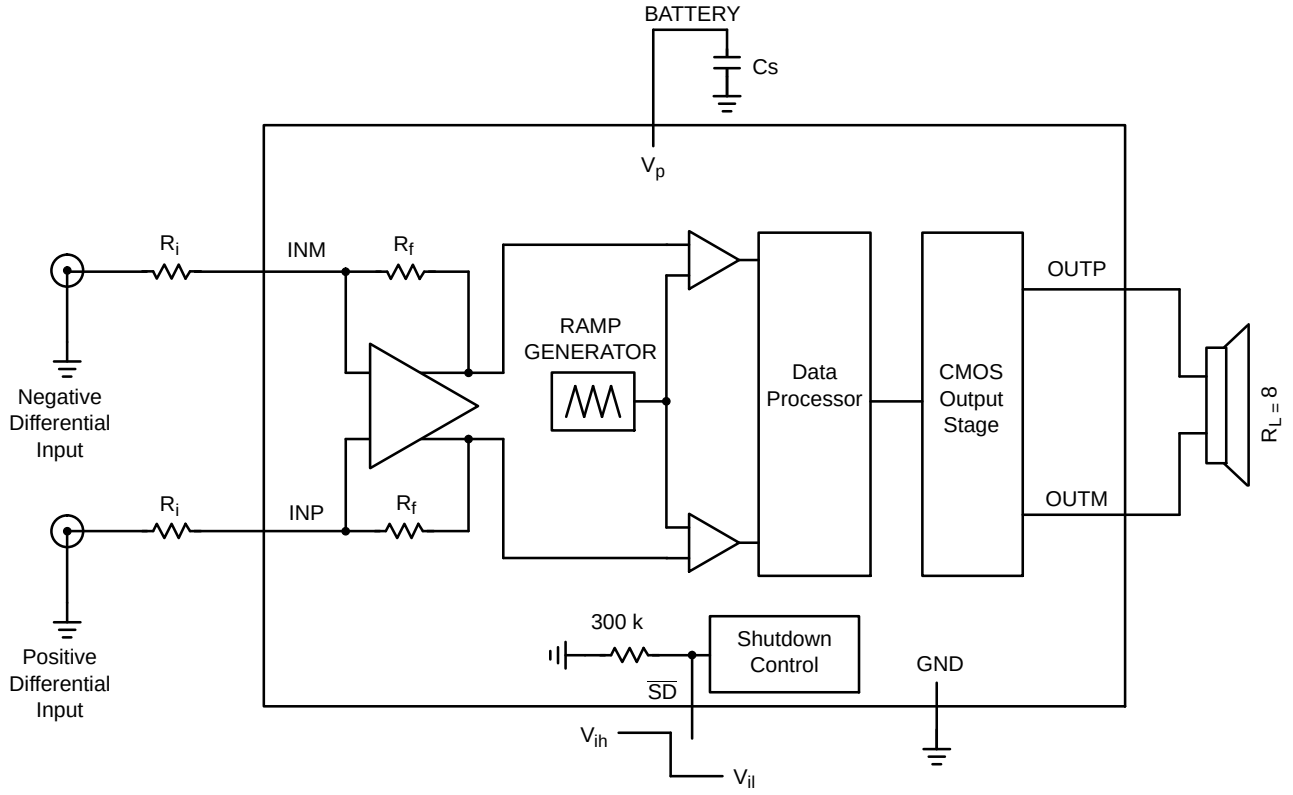


Figure 1. Typical Application

PIN DESCRIPTION

Pin No.		Symbol	Type	Description
CSP	UDFN8			
A1	3	INP	I	Positive Differential Input.
A2	7	GND	I	Analog Ground.
A3	8	OUTM	O	Negative BTL Output.
B1	2	V_p	I	Analog Positive Supply. Range: 2.5 V – 5.5 V.
B2	6	V_p	I	Power Analog Positive Supply. Range: 2.5 V – 5.5 V.
B3	7	GND	I	Analog Ground.
C1	4	INM	I	Negative Differential Input.
C2	1	$\overline{SD}$	I	The device enters in Shutdown Mode when a low level is applied on this pin. An internal 300 k resistor will force the device in shutdown mode if no signal is applied to this pin. It also helps to save space and cost.
C3	5	OUTP	O	Positive BTL Output.

MAXIMUM RATINGS

Symbol	Rating		Max	Unit
V_p	Supply Voltage	Active Mode Shutdown Mode	6.0 7.0	V
V_{in}	Input Voltage		−0.3 to V_{CC} +0.3	V
I_{out}	Max Output Current (Note 1)		1.5	A
P_d	Power Dissipation (Note 2)		Internally Limited	−
T_A	Operating Ambient Temperature		−40 to +85	°C
T_J	Max Junction Temperature		150	°C
T_{stg}	Storage Temperature Range		−65 to +150	°C
R_{JA}	Thermal Resistance Junction−to−Air	9−Pin Flip−Chip UDFN8	90 (Note 3) 50	°C/W
− −	ESD Protection Human Body Model (HBM) (Note 4) Machine Model (MM) (Note 5)		> 2000 > 200	V
−	Latchup Current @ T_A = 85°C (Note 6)	9−Pin Flip−Chip UDFN8	±70 ±100	mA
MSL	Moisture Sensitivity (Note 7)		Level 1	

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. The device is protected by a current breaker structure. See “Current Breaker Circuit” in the Description Information section for more information.
2. The thermal shutdown is set to 160°C (typical) avoiding irreversible damage to the device due to power dissipation.
3. For the 9−Pin Flip−Chip CSP package, the R_{JA} is highly dependent of the PCB Heatsink area. For example, R_{JA} can equal 195°C/W with 50 mm^2 total area and also 135°C/W with 500 mm^2. When using ground and power planes, the value is around 90°C/W, as specified in table.
4. Human Body Model: 100 pF discharged through a 1.5 k resistor following specification JESD22/A114. On 9−Pin Flip−Chip, B2 Pin (V_P) is qualified at 1500 V.
5. Machine Model: 200 pF discharged through all pins following specification JESD22/A115.
6. Latchup Testing per JEDEC Standard JESD78.
7. Moisture Sensitivity Level (MSL): 1 per IPC/JEDEC standard: J−STD−020A.

ELECTRICAL CHARACTERISTICS (Limits apply for T_A = +25°C unless otherwise noted) (NCP2820FCT1G & NCP2820FCT2G)

Characteristic	Symbol	Conditions	Min	Typ	Max	Unit
Operating Supply Voltage	V_p	T_A = −40°C to +85°C	2.5	−	5.5	V
Supply Quiescent Current	I_{dd}	V_p = 3.6 V, R_L = 8.0 V_p = 5.5 V, No Load V_p from 2.5 V to 5.5 V, No Load T_A = −40°C to +85°C	− −			

ELECTRICAL CHARACTERISTICS (Limits apply for T

ELECTRICAL CHARACTERISTICS (Limits apply for T_A = +25°C unless otherwise noted) (NCP2820MUTBG & NCV2820MUTBG)

Characteristic	Symbol	Conditions	Min	Typ	Max	Unit
RMS Output Power	Po	R_L = 8.0 , f = 1.0 kHz, THD+N < 1%				W
		V_p = 2.5 V	−	0.22	−	
		V_p = 3.0 V	−	0.33	−	
		V_p = 3.6 V	−	0.45	−	
		V_p = 4.2 V	−	0.67	−	
		V_p = 5.0 V	−	0.92	−	
		R_L = 8.0 , f = 1.0 kHz, THD+N < 10%				W
		V_p = 2.5 V	−	0.36	−	
		V_p = 3.0 V	−	0.53	−	
		V_p = 3.6 V	−	0.76	−	
		V_p = 4.2 V	−	1.07	−	
		V_p = 5.0 V	−	1.49	−	
		R_L = 4.0 , f = 1.0 kHz, THD+N < 1%				W
		V_p = 2.5 V	−	0.24	−	
		V_p = 3.0 V	−	0.38	−	
		V_p = 3.6 V	−	0.57	−	
		V_p = 4.2 V	−	0.83	−	
		V_p = 5.0 V	−	1.2	−	
		R_L = 4.0 , f = 1.0 kHz, THD+N < 10%				W
		V_p = 2.5 V	−	0.52	−	
		V_p = 3.0 V	−	0.8	−	
		V_p = 3.6 V	−	1.125	−	
		V_p = 4.2 V	−	1.58	−	
		V_p = 5.0 V	−	2.19	−	
Efficiency	−	R_L = 8.0 , f = 1.0 kHz				%
		V_p = 5.0 V, P_{out} = 1.2 W	−	87	−	
		V_p = 3.6 V, P_{out} = 0.6 W	−	87	−	
		R_L = 4.0 , f = 1.0 kHz				
		V_p = 5.0 V, P_{out} = 2.0 W	−	79	−	
		V_p = 3.6 V, P_{out} = 1.0 W	−	78	−	
Total Harmonic Distortion + Noise	THD+N	V_p = 5.0 V, R_L = 8.0 ,				%
		f = 1.0 kHz, P_{out} = 0.25 W	−	0.05	−	
		V_p = 3.6 V, R_L = 8.0 ,				
		f = 1.0 kHz, P_{out} = 0.25 W	−	0.06	−	
Common Mode Rejection Ratio	CMRR	V_p from 2.5 V to 5.5 V				dB
		V_{ic} = 0.5 V to V_p − 0.8 V	−	−62	−	
		V_p = 3.6 V, V_{ic} = 1.0 V_{pp}				
		f = 217 Hz	−	−56	−	
		f = 1.0 kHz	−	−57	−	
Power Supply Rejection Ratio	PSRR	$V_{p\_ripple\_pk-pk}$ = 200 mV, R_L = 8.0 , Inputs AC Grounded				dB
		V_p = 3.6 V				
		f = 217 kHz	−	−62	−	
		f = 1.0 kHz	−	−65	−	

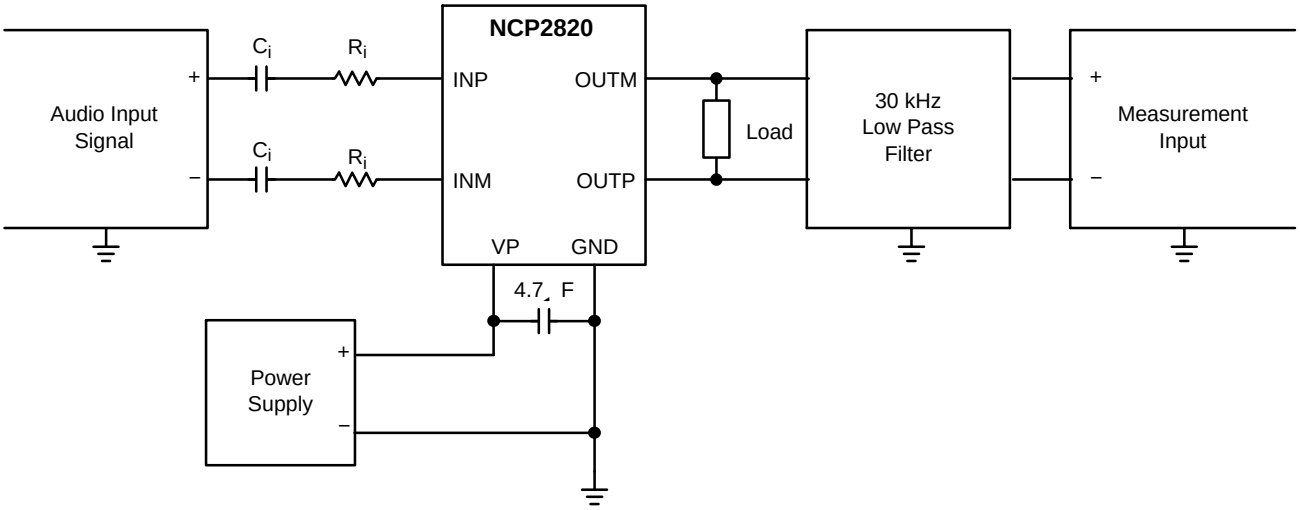
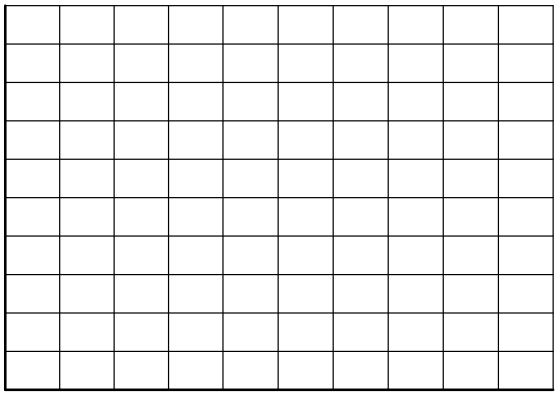


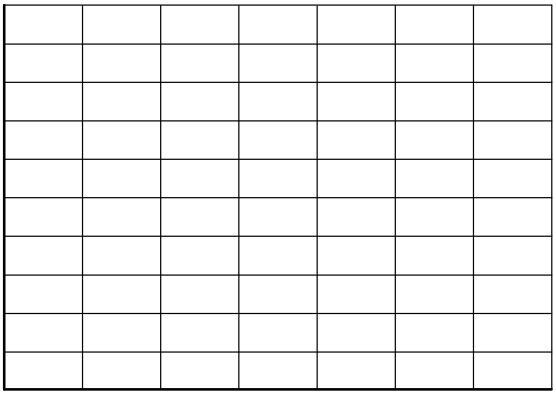
Figure 2. Test Setup for Graphs

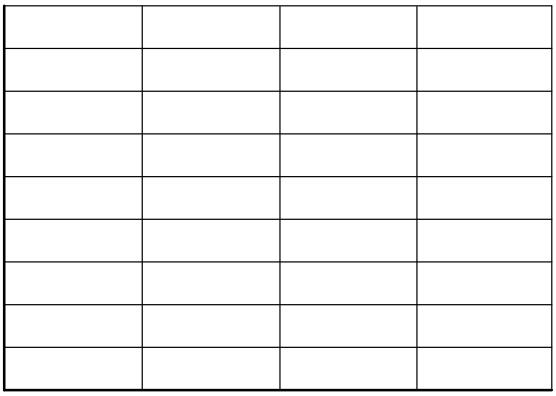
NOTES:

1. Unless otherwise noted, C_i = 100 nF and R_i= 150 k

TYPICAL CHARACTERISTICS







EFFICIENCY %

P_{out} (W)

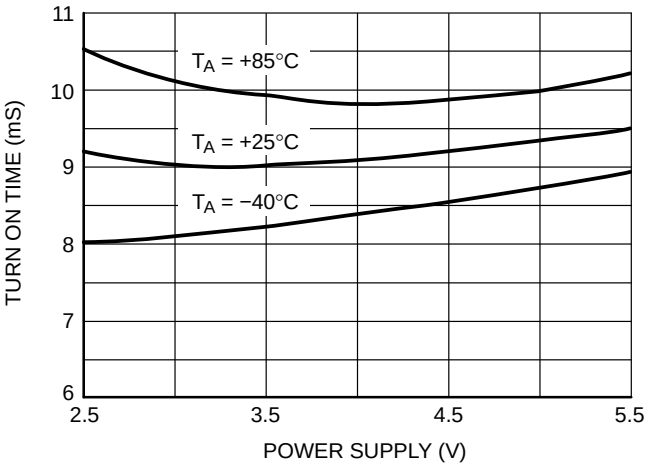


Figure 33. Turn on Time

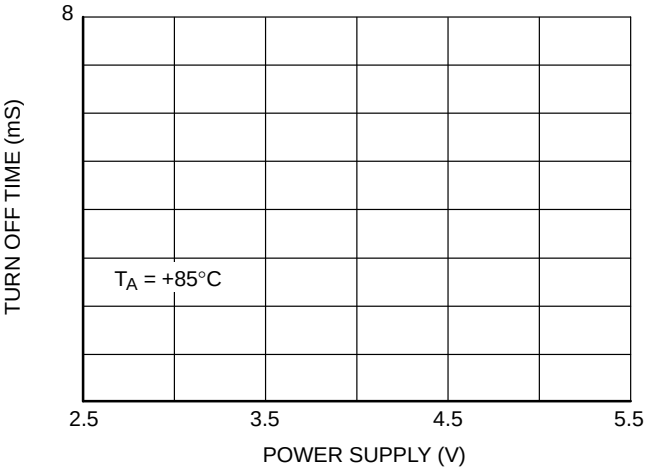


Figure 34. Turn off Time

APPLICATION INFORMATION

NCP2820 PWM Modulation Scheme

The NCP2820 uses a PWM modulation scheme with each output switching from 0 to the supply voltage. If V_{in} = 0 V outputs OUTM and OUTP are in phase and no current is flowing through the differential load. When a positive signal is applied, OUTP duty cycle is greater than 50% and OUTM is less than 50%. With this configuration, the current through the load is 0 A most of the switching period and thus power losses in the load are lowered.

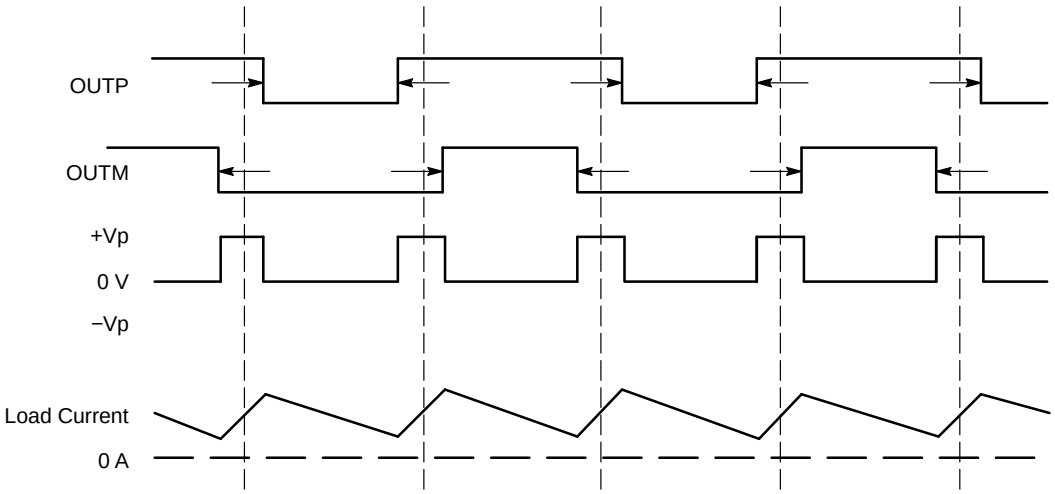


Figure 35. Output Voltage and Current Waveforms into an Inductive Loudspeaker DC Output Positive Voltage Configuration

Voltage Gain

The first stage is an analog amplifier. The second stage is

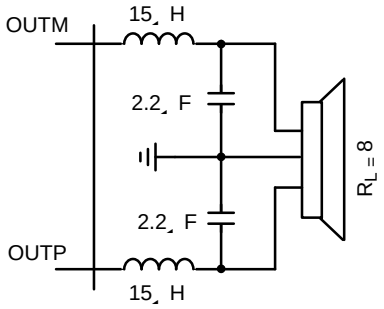


Figure 36. Advanced Optional Audio Output Filter

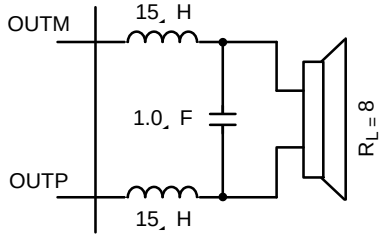


Figure 37. Optional Audio Output Filter

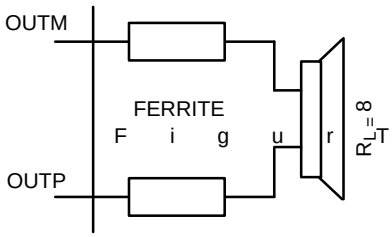


Figure 38. Optional EMI Ferrite Bead Filter

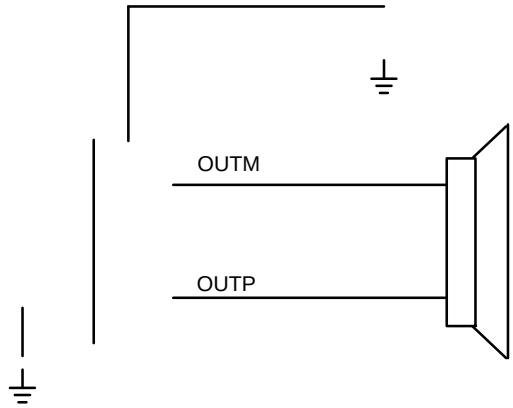


Figure 41. NCP2820 Application Schematic with Differential Input Configuration and High Pass Filtering Function

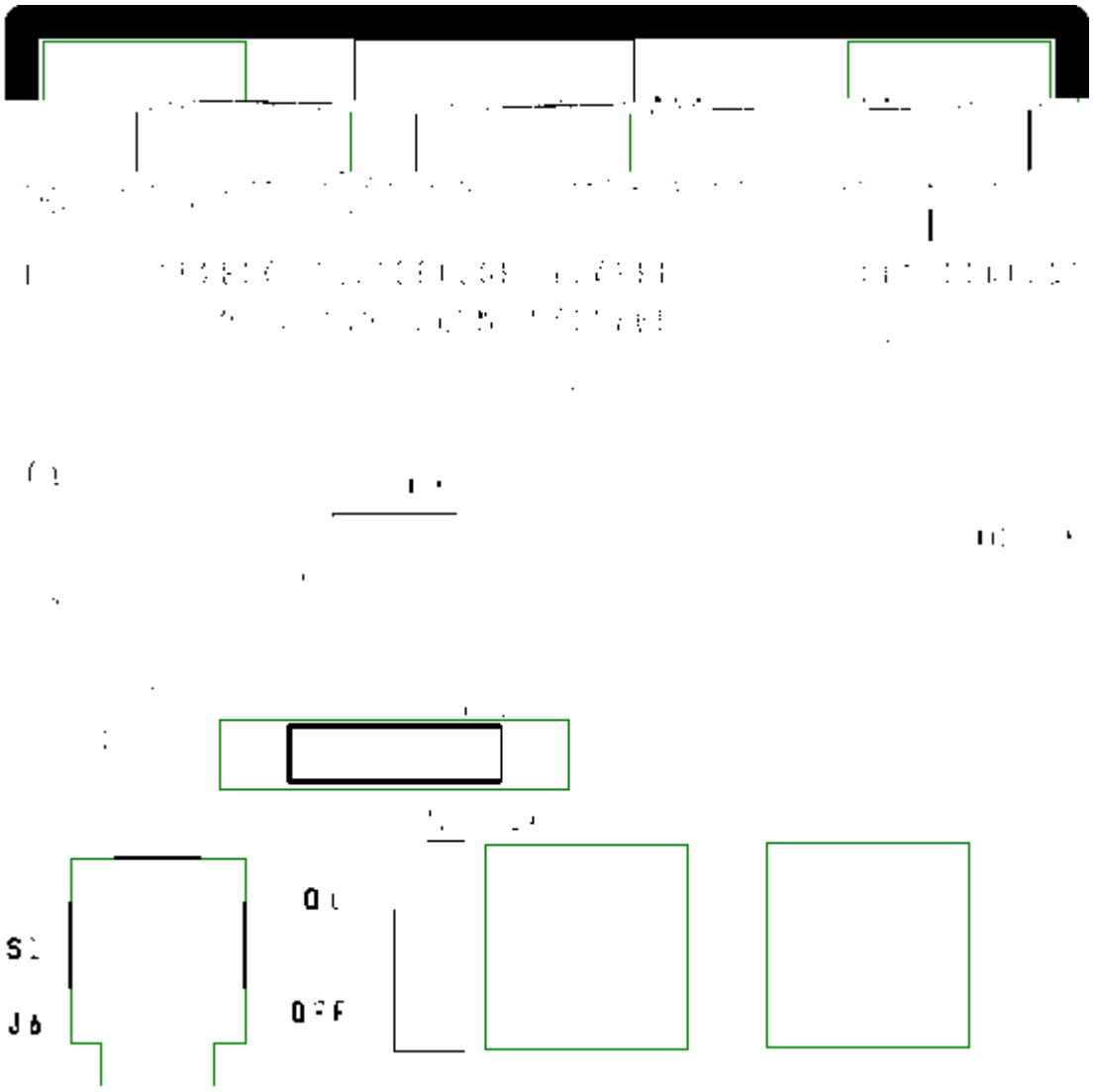


Figure 45. Silkscreen Layer of the UDFN8 Evaluation Board

PCB Layout Information

NCP2820 is suitable for low cost solution. In a very small package it gives all the advantages of a Class D audio amplifier. The required application board is focused on low cost solution too. Due to its fully differential capability, the audio signal can only be provided by an input resistor. If a low pass filtering function is required, then an input coupling capacitor is needed. The values of these components determine the voltage gain and the bandwidth frequency. The battery positive supply voltage requires a good decoupling capacitor versus the expected distortion.

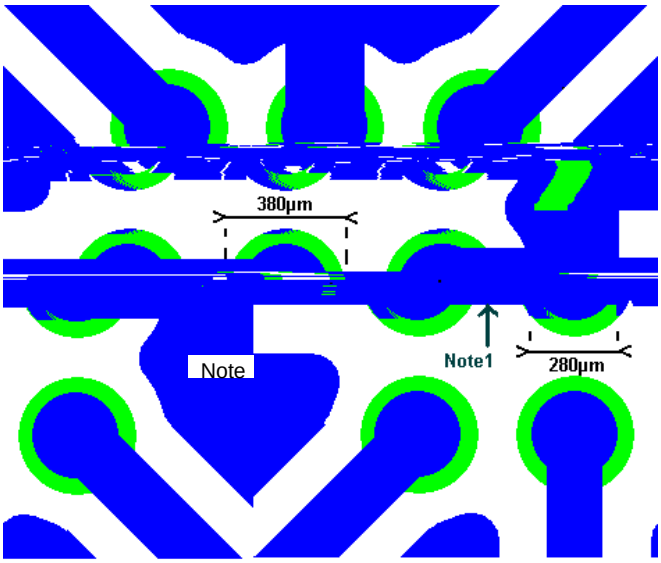


Figure 46. Top Layer of Two Layers Board Dedicated to the 9 Pin Flip Chip Package

Note: This track between Vp pins is only needed when a 2 layers board is used. In case of a typical 4 or more layers, the use of laser vias in pad will optimize the THD+N floor. The demonstration board delivered by ON Semiconductor is a 4 Layers with Top, Ground, Power Supply and Bottom.

Bill of Materials

Item	Part Description	Ref	PCB Footprint	Manufacturer	Part Number
1	NCP2820 Audio Amplifier	U1			NCP2820
2	SMD Resistor 150 k	R1, R2	0603	Vishay−Draloric	CRCW0603
3	Ceramic Capacitor 100 nF, 50 V, X7R	C1, C2	0603	TDK	C1608X7R1H104KT
4	Ceramic Capacitor 4.7¸ F, 6.3 V, X5R	C3, C4	0603	TDK	C1608X5R0J475MT

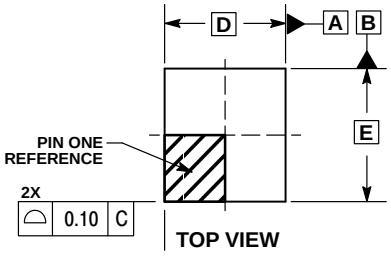
9 PIN FLIP CHIP 1.45x1.45x0.596

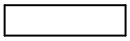
b-Free
strategy and soldering details, please do▮nloa
the

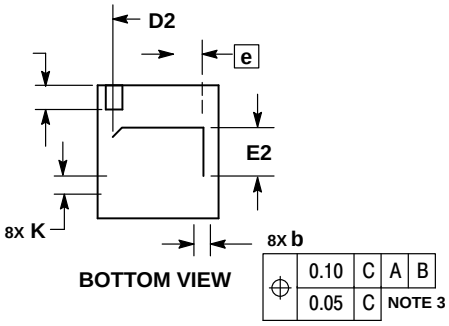
UDFN8 2x2.2, 0.5P
CASE 506AV
ISSUE C

DATE 26 JUN 2013

SCALE 4:1







NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 mm FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.