



Figure 3. NCP1840 Block Diagram

OPERATING RANGES

Rating	Symbol	Min	Max	Unit
Battery Supply Voltage	V _{BAT}	3	5.5	V
Digital Supply Voltage	DV _{CC}	3	5.5	V
Ground				

TYPICAL PERFORMANCE CHARACTERISTICS (V_{BAT} = 4.0 V, DV_{CC} = 3.3 V, I_{OUT} = 160 mA (8 LEDs at 20 mA/ch), C_{IN} = C

Register Writes & Reads

The ability of the NCP1840 to allow the internal registers to be both written and read provides the user with the benefit of being able to easily verify correct register writes and isolate system problem areas while troubleshooting. This ability also allows users to configure the register values according to desired LED performance, read these register values from the part, and then store these settings in external memory for future use. In addition, an over-temperature fault condition can also be read from a specific register, allowing for diagnostic feedback to the system controller.

Write Protocol

Control Bits

The NCP1840 has 3 control bits that are used to dictate the function that will be performed by the part. The following

table contains a description of each of these functions along with their dependencies on the register address, A[4:0], and the data byte, D[7:0].

CB2	CB1	CB0	Function
0	0	0	Turn all LED Channels ON/OFF All channels are turned ON/OFF according to the data in the Output Control Register. The current and PWM duty cycle will depend on each channel's Current Level and PWM Register. The register address field, A[4:0], is ignored along with the data byte, D[7:0]. The Master can issue a STOP condition without sending a data byte.
0	0	1	Program a Single Register (also Read Operation Setting) The register address, A[4:0], defines the register to be written or read. For a write, the data byte, D[7:0], defines the data to be written. The data will be loaded in the register but will not take effect until either a 000 or 010 Control Bit setting is applied. This is also the Control Bit setting required for a Read operation (see Read Protocol).
0	1	0	Program a Single Register and Turn all LED Channels ON/OFF The register address, A[4:0], defines the register to be written to and the data byte, D[7:0], defines the data to be written. After the receipt of the data byte, all channels will be turned ON/OFF according to the data in the Output Control Register. The current and PWM duty cycle will depend on each channel's Current Level and PWM Register.
0	1	1	Program all 8 Current Level Registers All Current Level Registers will be loaded with the data defined by the data byte, D[7:0]. The register address, A[4:0], is ignored. The data will be loaded in the registers but will not take effect until either a 000 or 010 Con- trol Bit setting is applied.
1	0	0	Program all 8 PWM Registers All PWM Registers will be loaded with the data defined by the data byte, D[7:0]. The register address, A[4:0], is ignored. The data will be loaded in the registers but will not take effect until either a 000 or 010 Control Bit setting is applied.
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved

CONTROL BITS DESCRIPTION

Register Address Map

The NCP1840 has a total of 18 different register addresses, as shown in the table below, made up of the following: 8 addresses for the individual channel Current Level Registers, 8 addresses for the individual channel PWM Registers, 1 address for the Output Control Register, and 1 address for the Main Status Register. The 8 Current Level Registers are used to program the output current for each of the 8 channels. The 8 PWM Registers are used to program the PWM duty cycle for each of the 8 channels. The Output Control Register is used to set the status, either ON or OFF, of all 8 channels. The Main Status Register is used to indicate the operating condition of the part: normal operation, low power mode, or over temperature.

REGISTER ADDRESS MAP

	Addr	ess – Bi	nary									
A4	A3	A2	A1	A0	Address – Hex	Function						
0	0	0	0	0	0	LED1 Current Level Register						
0	0	0	0	1	1	LED2 Current Level Register						
0	0	0	1	0	2	LED3 Current Level Register						
0	0	0	1	1	3	LED4 Current Level Register						
0	0	1	0	0	4	LED5 Current Level Register						
0	0	1	0	1	5	LED6 Current Level Register						
0	0	1	1	0	6	LED7 Current Level Register						
0	0	1	1	1	7	LED8 Current Level Register						
0	1	0	0	0	8	LED1 PWM Register						
0	1	0	0	1	9	LED2 PWM Register						

REGISTER ADDRESS MAP11

http://onsemi.com 12	

PWM REGISTER DESCRIPTION

Data – Binary									
D7	D6	D5	D4	D3	D2	D1	D0	Data – Hex	PWM Duty Cycle

Output Control Register

The Output Control Register on the NCP1840 is used to set the status, either ON or OFF, of all 8 channels. As shown in the following table, each bit in the register corresponds to one of the 8 LED channels. Each channel will be turned ON with a 1 loaded into the corresponding bit and will be turned OFF with a 0 loaded into that bit. When an LED channel is turned ON, the current level and PWM duty cycle of that channel will be dictated by the data that is loaded into its Current Level Register and PWM Register. It is important to note that any unused LED channel should not be turned ON.

OUTPUT CONTROL REGISTER DESCRIPTION

Register Bit (1 = ON, 0 = OFF)	D7	D6	D5	D4	D3	D2	D1	D0
Corresponding LED Channel	LED8	LED7	LED6	LED5	LED4	LED3	LED2	LED1

Main Status Register

The Main Status Register of the NCP1840 is used to indicate the operating condition of the part and is read–only. As shown in the following table, bit D0 indicates either normal operation (0) or an over temperature condition (1). When the on–chip temperature sensor detects an over–temperature condition, it will turn off all LED outputs, along with the charge pump, and set bit D0 to a logic one. If the over–temperature condition goes away, bit D0 will automatically reset to a logic zero and the part will resume normal operation. Therefore, bit D0 of this register can be read and used to help determine if an over–temperature condition currently exists on the part. Likewise, bit D2 indicates either normal operation (0) or low power mode operation (1). When all LED outputs are turned OFF and there is no I^2C communication for 5 ms, the part will put itself in a low power mode and set bit D2 to a logic one. When the Master wakes the device up with I^2C communication, bit D2 will be set to a logic zero once the entire chip is ready to run in normal operation. Therefore, when the Master wakes up the device, it can read bit D2 and wait for this bit to change to 0, indicating the return to normal operation.

MAIN STATUS REGISTER DESCRIPTION

D7	D6	D5	D4	D3	D2	D1	D0	
0	0		0 = Normal Operation	0	0 = Normal Operation			
0	0	0	0	0	1 = Low Power Mode	0	1 = Over Temperature	

Fault Management

The NCP1840 has several fault management features intended to provide increased performance and reliability to both the system and the part itself:

- Each LED output will detect if it is shorted to the charge pump output and if so will turn that particular channel's circuitry OFF. This saves power consumption that would otherwise be lost and provides the user with the ability to ensure that unused channels are turned OFF by tying them to the charge pump output.
- The charge pump output will detect any over-current events and automatically limit the current to less than 800 mA. This helps to prevent any damage to the chip and the system due to elevated current on this output.
- The charge pump output will detect a short-circuit event (less than 0.7 V) and limit the current to the soft-start limit of less than 94 mA. This helps to prevent damage to the chip and the system that could potentially be seen with the output being short-circuited to ground.
- The charge pump will reset itself to 1x mode if it reaches an overvoltage level (5.5 V to 6 V). This helps to prevent damage to the chip and the system in the

event that the supply voltage increases while the charge pump is operating in the 1.33x, 1.5x, or 2x mode.

- If the external resistor, R_{BIAS}, used to set the maximum output current and the internal reference current, is too small or otherwise short-circuits, the NCP1840 will detect this over-current condition and turn off the reference current and LED outputs. This helps to prevent damage to the chip and system due to elevated currents that would be present.
- The NCP1840 has an on-chip over temperature sensor that will detect any over-temperature condition (130°C - 163°C) and turn off all LED outputs along with the

Soft Start-Up

Step 4a. Set LEDs 1, 2, 3, 4, 8 to be ON and immediately activate the change with settings loaded in Steps 1–3.

4a.1 Set the Part Address to 1B (hex).

4a.2 Set the Read/Write bit to 0.

4a.3 Set the Control Bits to 010 and set the Register address to 10 (hex) to write to the Output Control Register.

4a.4 Set the Data to 8F (hex), which will set LEDs 1, 2, 3, 4, 8 to be ON.

Note: After this step the LEDs will immediately be activated with the current level and PWM duty cycle settings previously loaded.

Start	Part Address	R/W Ack		Control Bits	Register Address	Ack	Register Data	Ack	Stop
S	0011011								

Step 6. Read back the LED1 PWM Register value.

6.1 Set the part address to 1B (hex).

6.2 Set the Read/Write bit to 0.

6.3 Set the Controls Bits to 001 in order to perform a Read operation.

6.4 Set the Register Address to 08 (hex) in order to read LED1 PWM Register.

6.5 Issue another Start and set the part address to 1B (hex).

6.6 Set the Read/Write bit to 1.

Note: After this step, the NCP1840 will transmit the LED1 PWM Register data byte which should be 20 (hex).

Start	Part Ad- dress	R/W	Ack	Control Bits	Register Address	Ack	Start	Part Address	R/W	Ack	Register Data	Ack	Stop
S	0011011	0	А	001	01000	А	S	0011011	1	А	Data Out	notA	Р

LAYOUT CONSIDERATIONS

Some key layout guidelines are as follows:

- 1. The NCP1840 requires a low-inductance ground.
- 2. Connect Pin 6 and Pin 15 to the "ground pad" of the NCP1840's package see Figure 15.
- 3. Place vias on the "ground pad," connecting the GND of the NCP1840 directly to the PCB ground plane see Figure 15.



Figure 15. Ground Connection Recommendation

4. Use good–quality X5R or X7R ceramic capacitors for C_0 , C_1 , C_2 , and C_{BAT} – see Figure 16.



Figure 16. Schematic Showing Charge Pump and Decoupling Capacitors

5. Charge pump capacitors C_0 , C_1 , C_2 , and decoupling capacitor C_{BAT} should be as physically close to the NCP1840 as possible – see Figure 17.



Figure 17. C_0 , C_1 , C_2 , and C_{BAT} Layout Recommendation

QUAD-MODE is a registered trademark of Semiconductor Components Industries, LLC (SCILLC).

QFN20, 4x4, 0.5P CASE 485E ISSUE C

DATE 13 FEB 2018



GENERIC MARKING DIAGRAM*



*This information is generic. Please refer to device data sheet for actual part marking. Pb–Free indicator, "G" or microdot " ■", may or may not be present. Some products may not follow the Generic Marking.

PIT T*.007 Tw[FROM THE TERMINAL TIP)103.9(.)][1.285 1.115 TD.0102 Tw[4.)@1(COPLANARITY APPLIES DIMENSIONS: MILLIMETERS

*For additional information on our Pb–Free strategy and soldering details, please download the onsemi Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

onsemi, , and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "onsemi" or its affiliates and/or subsidiaries in the United States and/or other countries. onsemi owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of onsemi's product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. Onsemi reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as-is" and onsemi makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does onsemi assume any liability arising out of the application or use of any product or incruit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using onsemi