NCP1397A/B, NCV1397A/B

High Performance Resonant Mode Controller with Integrated High-Voltage Drivers

The NCP1397 is a high performance controller that can be utilized in half bridge resonant topologies such as series resonant, parallel resonant and LLC resonant converters. It integrates 600 V gate drivers, simplifying layout and reducing external component count. With its unique architecture, including a 500 kHz Voltage Controlled Oscillator whose control mode permits flexibility when an ORing function is required, the NCP1397 delivers everything needed to build a reliable and rugged resonant mode power supply.

The NCP1397 provides a suite of protection features with configurable settings to optimize any application. These include: auto−recovery or fault latch−off, brown−out, open optocoupler, soft−start and short−circuit protection. Deadtime is also adjustable to overcome shoot through current.

Features

- High−Frequency Operation from 50 kHz up to 500 kHz
- 600 V High−Voltage Floating Driver
- Adjustable Minimum Switching Frequency with ±3% Accuracy
- Adjustable Deadtime from 100 ns to 2 μs.
- Startup Sequence Via an Externally Adjustable Soft−Start
- Brown−Out Protection for a Simpler PFC Association
- Latched Input for Severe Fault Conditions, e.g. Over Temperature or OVP
- Timer−Based Input with Auto−Recovery Operation for Delayed Event Reaction
- Latched Overcurrent Protection
- Disable Input for Immediate Event Reaction or Simple ON/OFF Control
- V_{CC}

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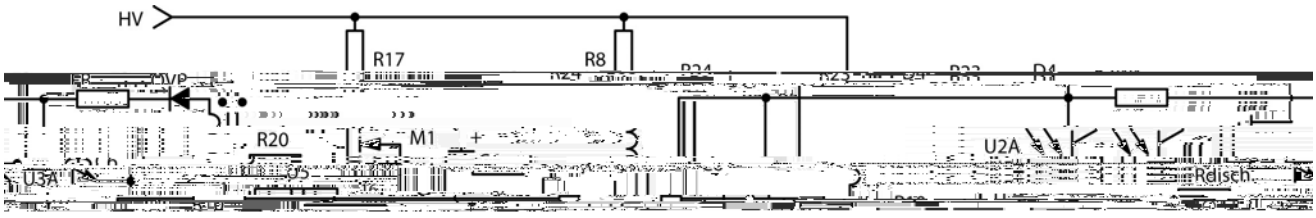


Figure 1. Typical Application Example

PIN FUNCTION DESCRIPTION

Pin #	Pin Name	Function	Pin Description
1	CSS(dis)	Soft−Start Discharge	Soft−start capacitor discharge pin. Connect to the soft−start capacitor to reset it before startup or during overload conditions.
2	Fmax	Maximum frequency clamp	A resistor sets the maximum frequency excursion
3	Ctimer	Timer duration	Sets the timer duration in presence of a fault
4	Rt	Minimum frequency clamp	Connecting a resistor to this pin, sets the minimum oscillator frequency reached for V_{FB} = 1 V.
5	BO		

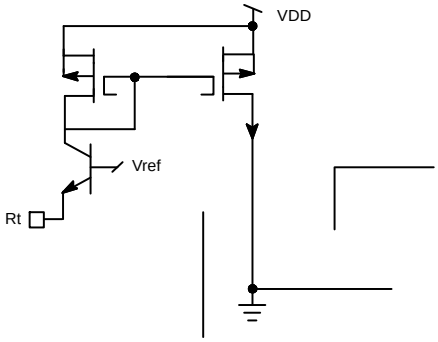


Figure 3. Internal Circuit Architecture (NCP1397B)

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
High Voltage bridge pin, pin 14	V_{BRIDGE}	−1 to 600	V
Floating supply voltage, ground referenced	V_{BOOT} − V_{BRIDGE}	0 to 20	V
High side output voltage	$V_{DRV(HI)}$	V_{BRIDGE}−0.3 to V_{BOOT}+0.3	V
Low side output voltage	$V_{DRV(LO)}$	−0.3 to V_{CC}+0.3	V
Allowable output slew rate	dV_{BRIDGE}/dt	50	V/ns
Power Supply voltage, pin 12	V_{CC}	20	V
Maximum voltage, all pins (except pin 11 and 10)	−	−0.3 to 10	V
Thermal Resistance Junction−to−Air, SOIC version	$R_{\theta JA}$	130	°C/W
Storage Temperature Range	−	−60 to +150	°C
ESD Capability, Human Body Model (HBM) (All pins except HV pins)	−	2	kV
ESD Capability, Machine Model (MM)	−	200	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. This device(s) contains ESD protection and exceeds the following tests:
   Human Body Model 2000 V per JEDEC Standard JESD22−A114E
   Machine Model 200 V per JEDEC Standard JESD22−A115−A
2. This device meets latchup tests defined by JEDEC Standard JESD78.

ELECTRICAL CHARACTERISTICS

(For typical values T_J = 25°C, for min/max values T_J = −40°C to +125°C, Max T_J = 150°C, V_{CC} = 12 V unless otherwise noted)

Symbol	Rating	Pin	Min	Typ	Max	Unit
SUPPLY SECTION						
$V_{CC(on)}$	Turn−on threshold level, V_{CC} going up	12	9.7	10.5	11.3	V
$V_{CC(min)}$	Minimum operating voltage after turn−on	12	8.7	9.5	10.3	V
$V_{boot(on)}$	Startup voltage on the floating section	16−14	8	9	10	V
$V_{boot(min)}$	Cutoff voltage on the floating section	16−14	7.4	8.4	9.4	V
$I_{startup}$	Startup current, $V_{CC} < V_{CC(on)}$	12	−	−	300	μA
$V_{CC(reset)}$	V_{CC} level at which the internal logic gets reset	12	−	6.6	−	V
I_{CC1}	Internal IC consumption, no output load on pin 15/14 – 11/10, F_{SW} = 300 kHz	12	−	4	−	mA
I_{CC2}	Internal IC consumption, 1 nF output load on pin 15/14 – 11/10, F_{SW} = 300 kHz	12	−	11	−	mA
I_{CC3}	Consumption in fault or disable mode (All drivers disabled, Rt = 34 kΩ, R_{DT} = 10 kΩ)	12	−	1.5	−	mA
VOLTAGE CONTROL OSCILLATOR (VCO)						
$F_{SW(min)}$	Minimum switching frequency, Rt = 34 kΩ on pin 4, V_{pin6} = 0.8 V, DT = 300 ns	4	58.2	60	61.8	kHz
$F_{SW(max)}$	Maximum switching frequency, $R_{f(max)}$ = 1.9 kΩ on pin 2, V_{pin6} > 5.3 V, Rt = 34 kΩ, DT = 300 ns	2	440	500	560	kHz
FB_{SW}	Feedback pin swing above which Δf = 0	6	−	5.3	−	V
DC	Operating duty−cycle symmetry	11−15	48	50	52	%
T_{del1}	Delay before driver restart from fault or disable mode	−	−	700	−	ns
T_{del2}	Delay before driver restart after $V_{CC(on)}$ event (Note 4)	−	−	11	−	μs
$V_{ref(Rt)}$	Reference voltage for Rt pin	4	2.18	2.3	2.42	V
FEEDBACK SECTION						
R_{FB}	Internal pulldown resistor	6	−	20	−	kΩ
$V_{FB(min)}$	Voltage on pin 6 below which the FB level has no VCO action	6	−	1.1	−	V
$V_{FB(off)}$	Voltage on pin 6 below which the controller considers the FB fault	6	240	280	320	mV
$V_{FBoff(hyste)}$						

ELECTRICAL CHARACTERISTICS (continued)
(For typical values T_J = 25°C, for min/max values T_J = −40°C to +125°C, Max T_J = 150°C, V_{CC} = 12 V unless otherwise noted)

Symbol	Rating	Pin	Min	Typ	Max	Unit
TIMERS						
I_{timer1}	Timer capacitor charge current during feedback fault or when $V_{ref(fault)} < V_{pin9} < V_{ref(OCP)}$	3	150	175	190	μA
I_{timer2}	Timer capacitor charge current when $V_{pin9} > V_{ref(OCP)}$ ($I_{charge1}$ + $I_{charge2}$) – A version only	3	1.1	1.3	1.5	mA
T_{timer}	Timer duration with a 1 μF capacitor and a 1 MΩ resistor, I_{timer1} current applied	3	−	24	−	ms
T_{timerR}	Timer recurrence in permanent fault, same values as above	3	−	1.4	−	s
$V_{timer(on)}$	Voltage at which pin 3 stops output pulses	3	3.8	4	4.2	V
$V_{timer(off)}$	Voltage at which pin 3 restarts output pulses	3	0.95	1	1.05	V
$R_{SS(dis)}$	Soft−start discharge switch channel resistance	1	−	100	−	Ω
PROTECTION						
$V_{ref(Skip)}$	Reference voltage for Skip/Disable input (Note 4)	8	630	660	690	mV
$Hyste_{(Skip)}$	Hysteresis for Skip/Disable (Note 4)	8	−	45	−	mV
$V_{ref(Fault)}$	Reference voltage for Fault comparator	9	0.99	1.04	1.09	V
$Hyste_{(Fault)}$	Hysteresis for fault comparator input	9	−	60	−	mV
$V_{ref(OCP)}$	Reference voltage for OCP comparator	9	1.47	1.55	1.63	V
$Hyste_{(OCP)}$	Hysteresis for OCP comparator input	9	−	90	−	mV
$T_{p(Disable)}$	Propagation delay from disable input to the drive shutdown	8	−	60	100	ns
$IBO_{(bias)}$	Brown−Out input bias current	5	−	0.02	−	μA
VBO	Brown−Out level	5	0.99	1.04	1.09	V
IBO	Hysteresis current, V_{pin5} > VBO	5	25	28	31	μA
VI_{atch}	Latching voltage	5	3.7	4	4.3	V

TYPICAL CHARACTERISTICS

APPLICATION INFORMATION

The NCP1397A/B includes all necessary features to help

This techniques allows us to detect a fault on the converter in case the FB pin cannot rise above 0.3 V (to actually close the loop) in less than a duration imposed by the programmable timer. Please refer to the fault section for detailed operation of this mode.

As shown on Figure 26, the internal dynamics of the VCO control voltage will be constrained between 0.5 V and 2.3 V, whereas the feedback loop will drive Pin 6 (FB) between 1.1 V and 5.3 V. If we take the default FB pin excursion numbers, 1.1 V = 50 kHz, 5.3 V = 500 kHz, then the VCO maximum slope will be:

$$\frac{500\ k - 50\ k}{4.2} = 107\ kHz/V$$

Figures 27 and 28 portray the frequency evolution depending on the feedback pin voltage level in a different frequency clamp combination.

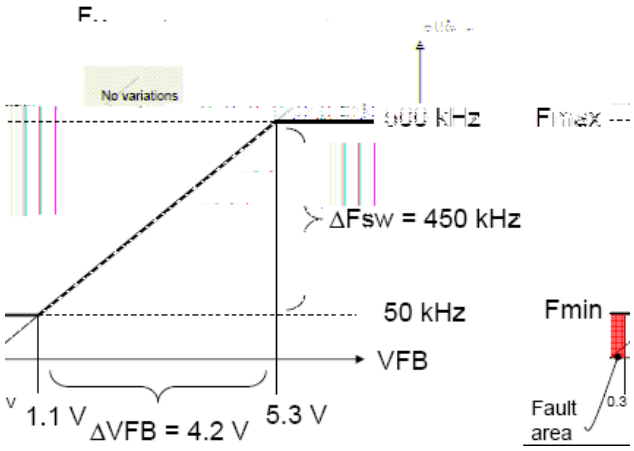


Figure 27. Maximal Default Excursion, Rt = 41 kΩ on Pin 4 and $R_{F(max)}$ = 1.9 kΩ on Pin 2

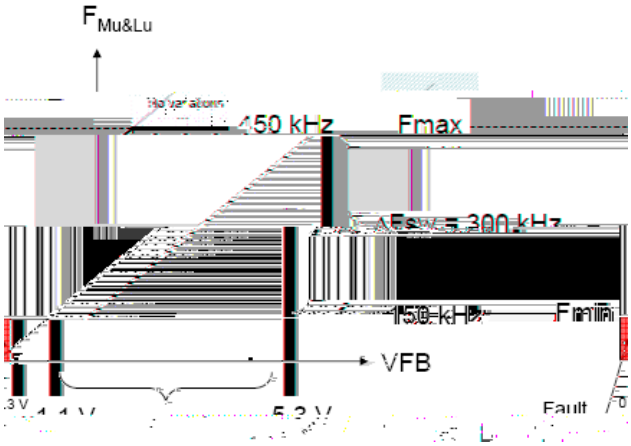
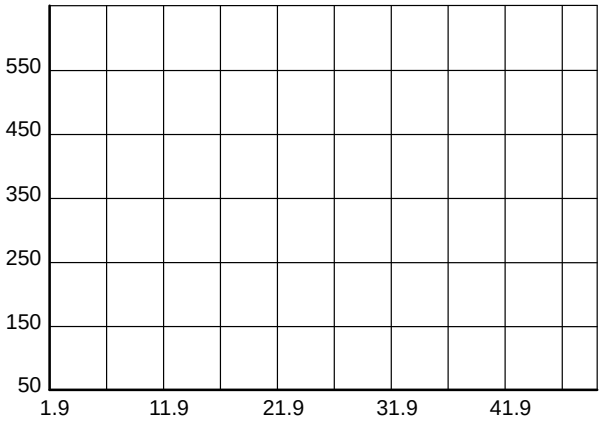


Figure 28. Here a Different Minimum Frequency was Programmed as well as a Maximum Frequency Excursion

Please note that the previous small−signal VCO slope has now been reduced to 300k / 4.1 = 71 kHz / V on M_{upper} and M_{lower} outputs. This offers a mean to magnify the feedback excursion on systems where the load range does not generate a wide switching frequency excursion. Due to this option, we will see how it becomes possible to observe the feedback level and implement skip cycle at light loads. It is important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450
350
250
150
50
1.9
11.9
21.9
31.9
41.9

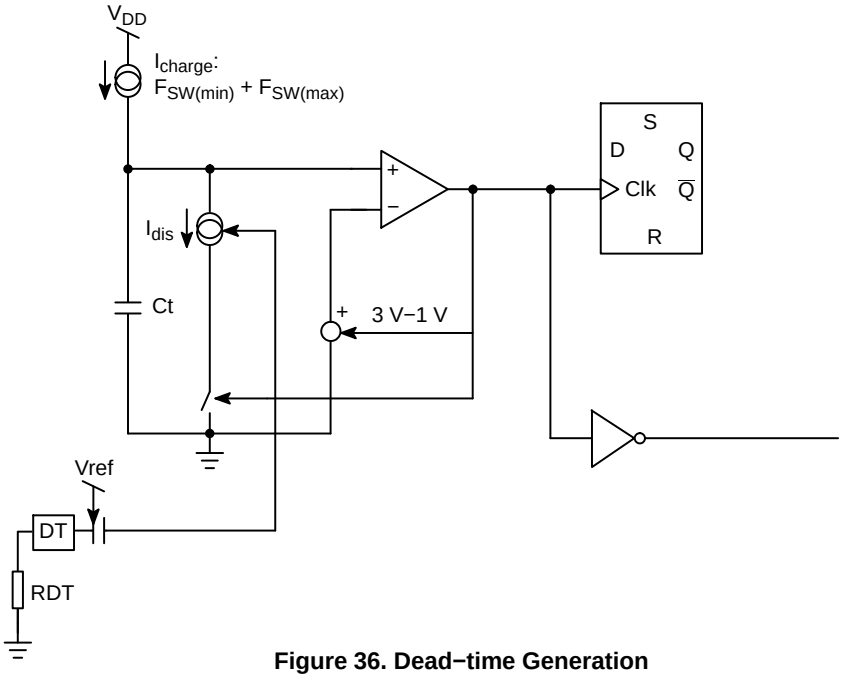
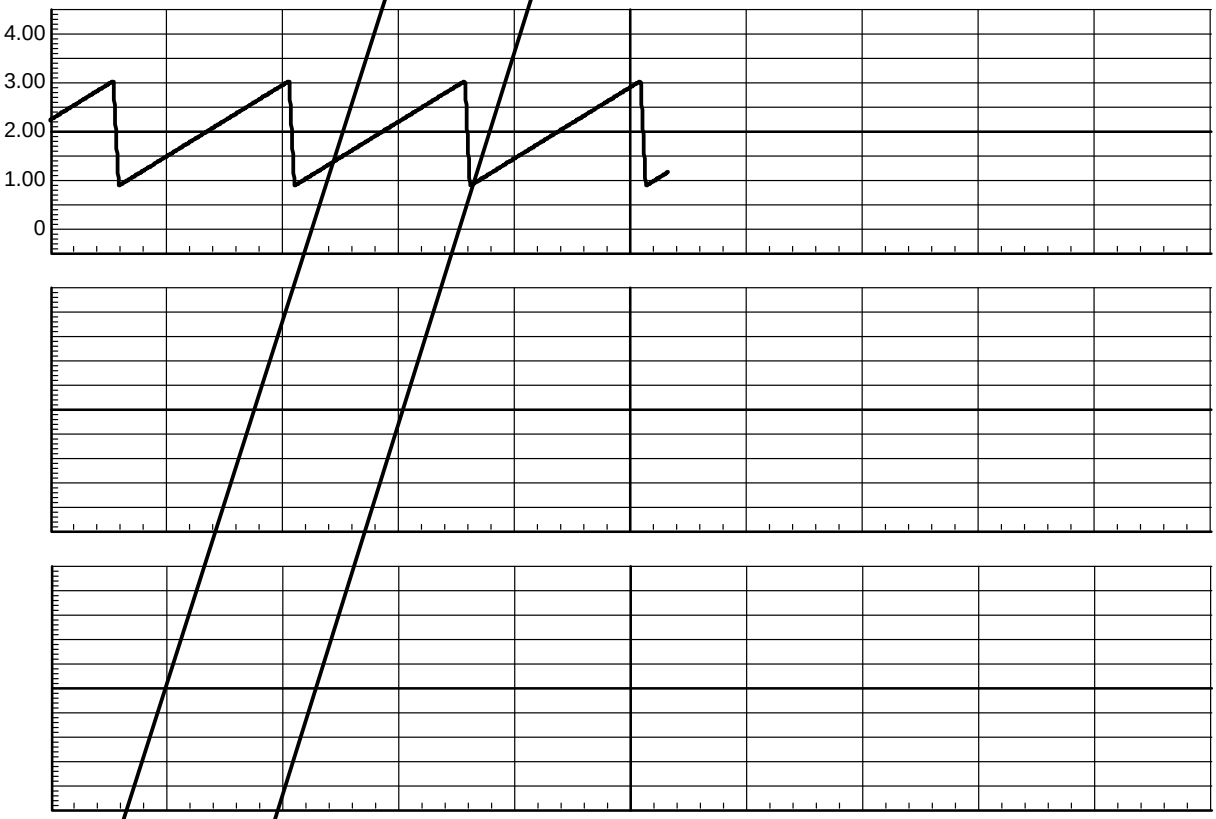


Figure 36. Dead−time Generation


4.00
3.00
2.00
1.00
0

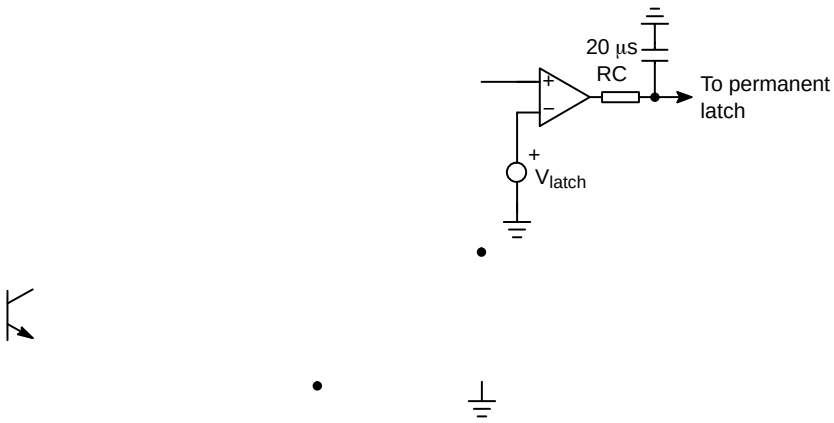


Figure 42. Adding a Comparator on the BO Pin Offers a way to Latch−off the Controller

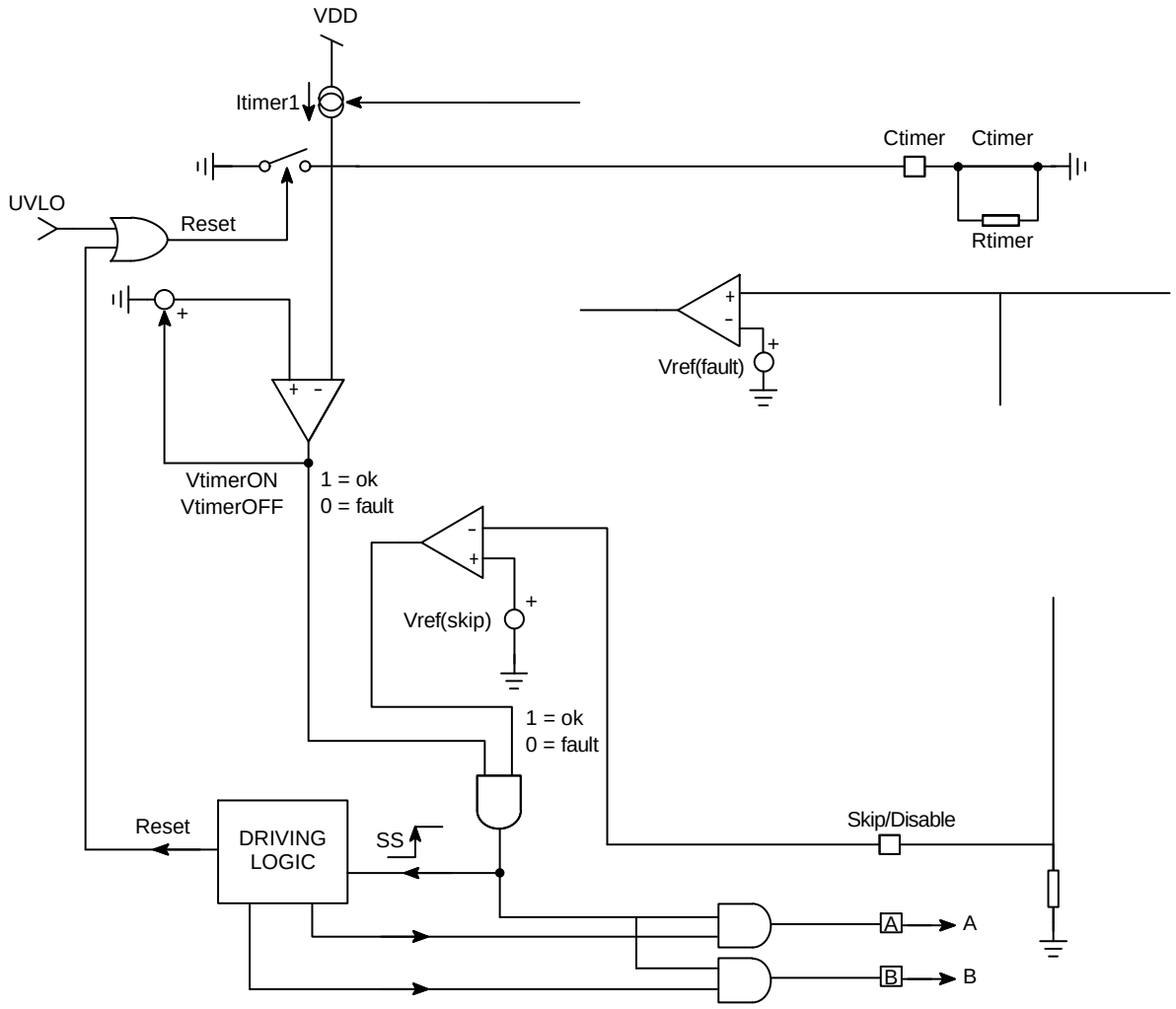


Figure 43. Fault Input Logic for NCP1397A

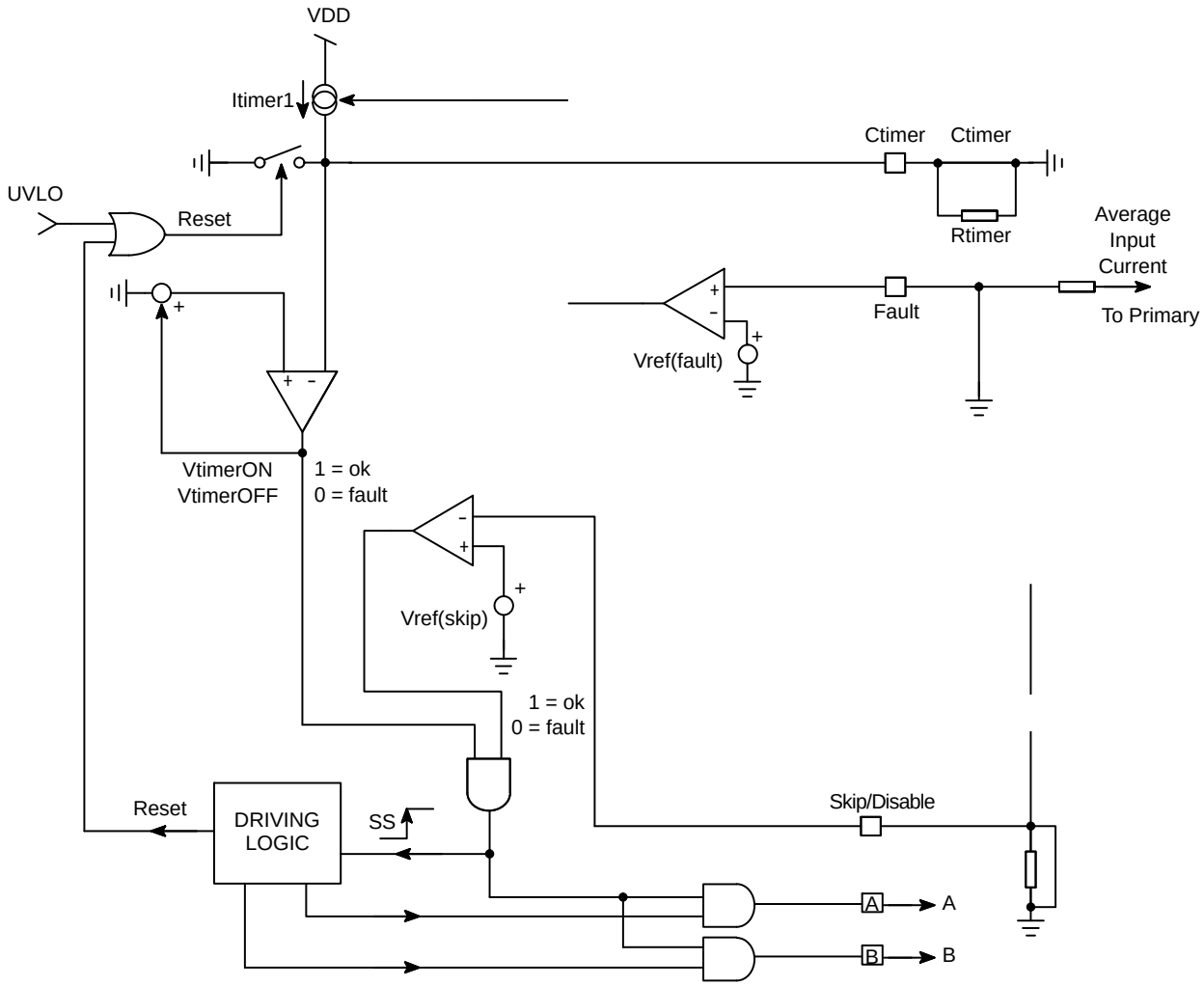


Figure 44. Fault Input Logic for NCP1397B

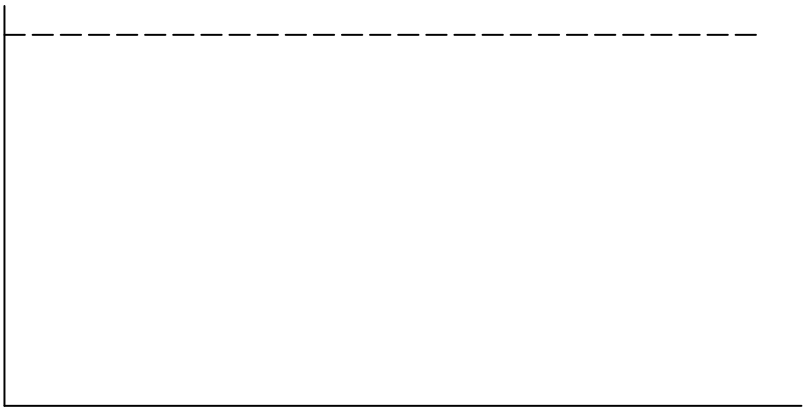


Figure 45. A Resistor Can Easily Program the Capacitor Discharge Time

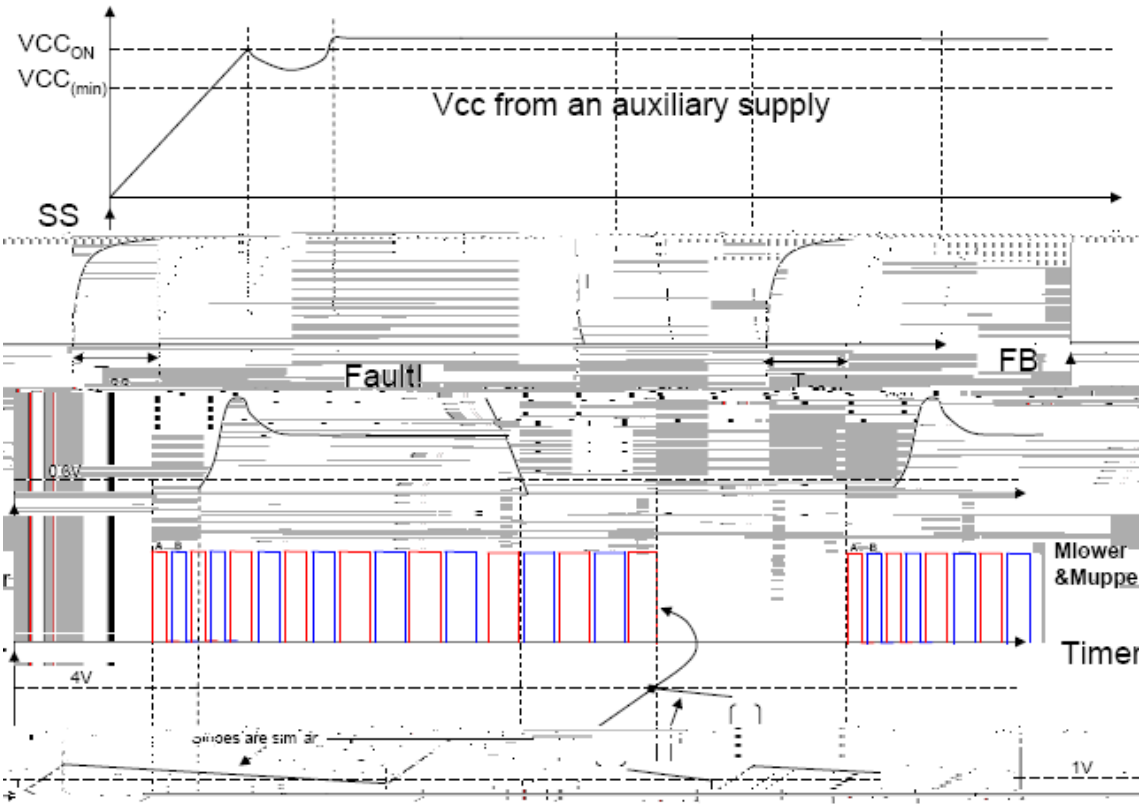


Figure 47. At Power On, Output A is First Activated and the Frequency Slowly Decreases Based on the Soft−Start Capacitor Voltage

Figure 47 depicts an auto−recovery situation, where the timer has triggered the end of output pulses. In that case, the V_{CC} level was given by an auxiliary power supply, hence its stability during the hiccup. A similar situation can arise if the user selects a more traditional startup method, with an auxiliary winding. In that case, the $V_{CC(min)}$ comparator stops the output pulses whenever it is activated, that is to say, when V_{CC} falls below 9.5 V typical. At this time, the V_{CC} pin still receives its bias current from the startup resistor and increases toward $V_{CC(on)}$. When the voltage reaches $V_{CC(on)}$, a standard sequence takes place, involving a soft−start. Figure 48 portrays this behavior.

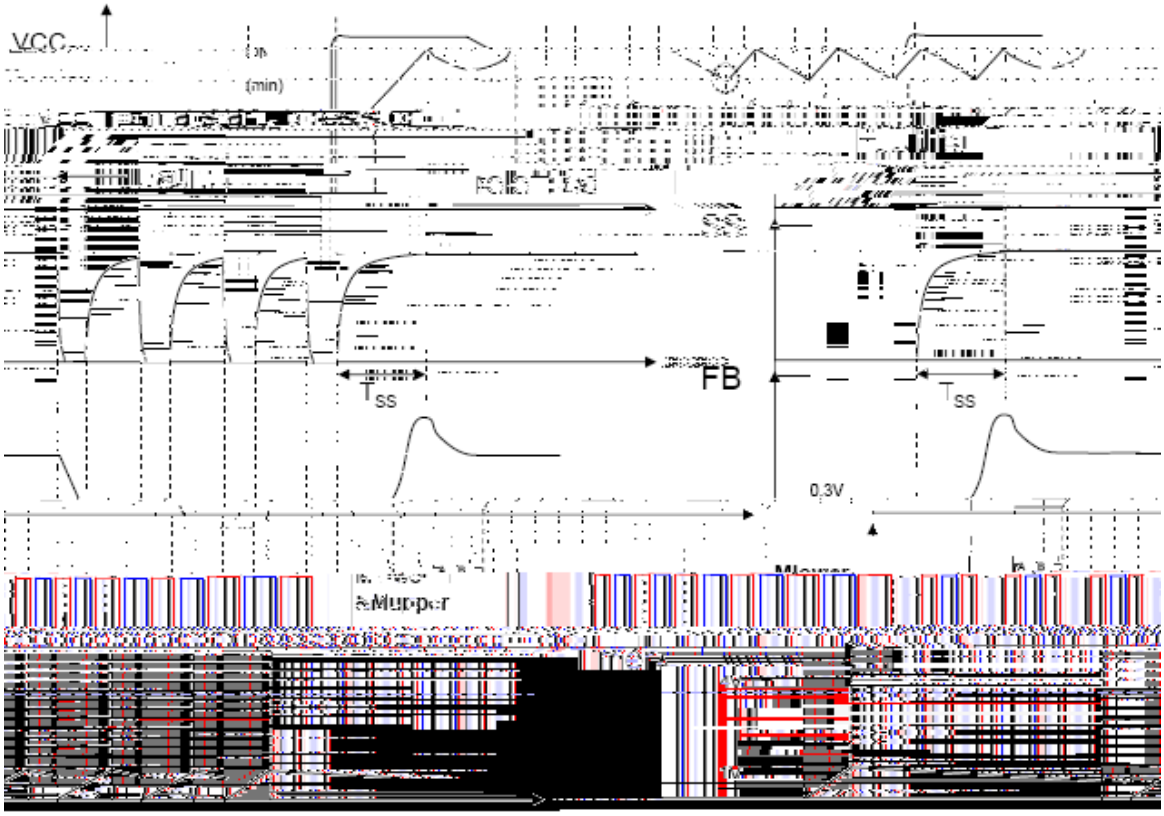


Figure 48. When the V_{CC} is to Low, All Pulses are Stopped Until V_{CC} Goes Back to the Startup Voltage

The High−Voltage Driver

The driver features a traditional bootstrap circuitry, requiring an external high−voltage diode for the capacitor refueling path. Figure 49 shows the internal architecture of the high−voltage section.

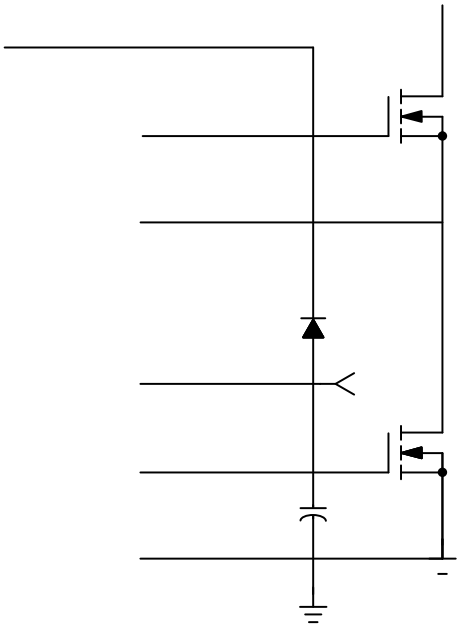
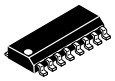


Figure 49. The Internal High−voltage Section of the NCP1397

The device incorporates an upper UVLO circuitry that makes sure enough V_{gs} is available for the upper side MOSFET. The B and A outputs are delivered by the internal logic, as



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