NC 1200

M C -M
C W L -
O -L

Housed in SOIC−8 or PDIP−8 package, the NCP1200 represents a major leap toward ultra−compact Switchmode Power Supplies. Due to a novel concept, the circuit allows the implementation of a complete offline battery charger or a standby SMPS with few external components. Furthermore, an integrated output short−circuit protection lets the designer build an extremely low−cost AC−DC wall adapter associated with a simplified feedback scheme.

With an internal structure operating at a fixed 40 kHz, 60 kHz or 100 kHz, the controller drives low gate−charge switching devices like an IGBT or a MOSFET thus requiring a very small operating power. Due to current−mode control, the NCP1200 drastically simplifies the design of reliable and cheap offline converters with extremely low acoustic generation and inherent pulse−by−pulse control.

When the current setpoint falls below a given value, e.g. the output power demand diminishes, the IC automatically enters the skip cycle mode and provides excellent efficiency at light loads. Because this occurs at low peak current, no acoustic noise takes place.

Adj HV

Finally, the IC is self−supplied from the DC rail, eliminating the need of an auxiliary winding. This feature ensures operation in presence of low output voltage or shorts.

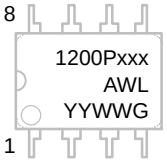
CS

Features

- No Auxiliary Winding Ov1cg theP SUFFIXCASE 62618

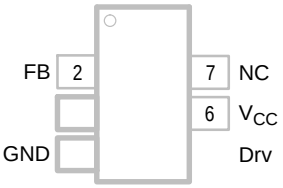
MARKING DIAGRAMS

200Dy
ALYW
▪



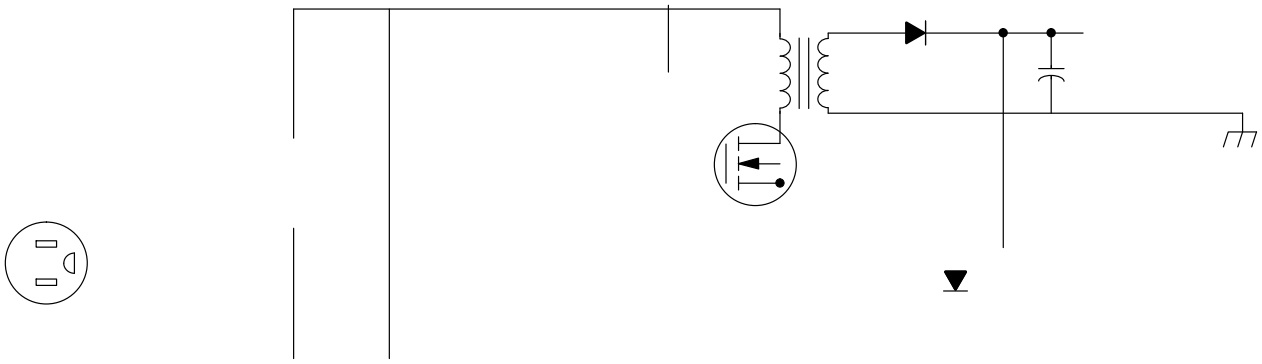
xxx = Device Code: 40, 60 or 100
y = Device Code:
4 for 40
6 for 60
1 for 100
A = Assembly Location
L = Wafer Lot
Y, YY = Year
W, WW = Work Week
G, ▪ = Pb−Free Package

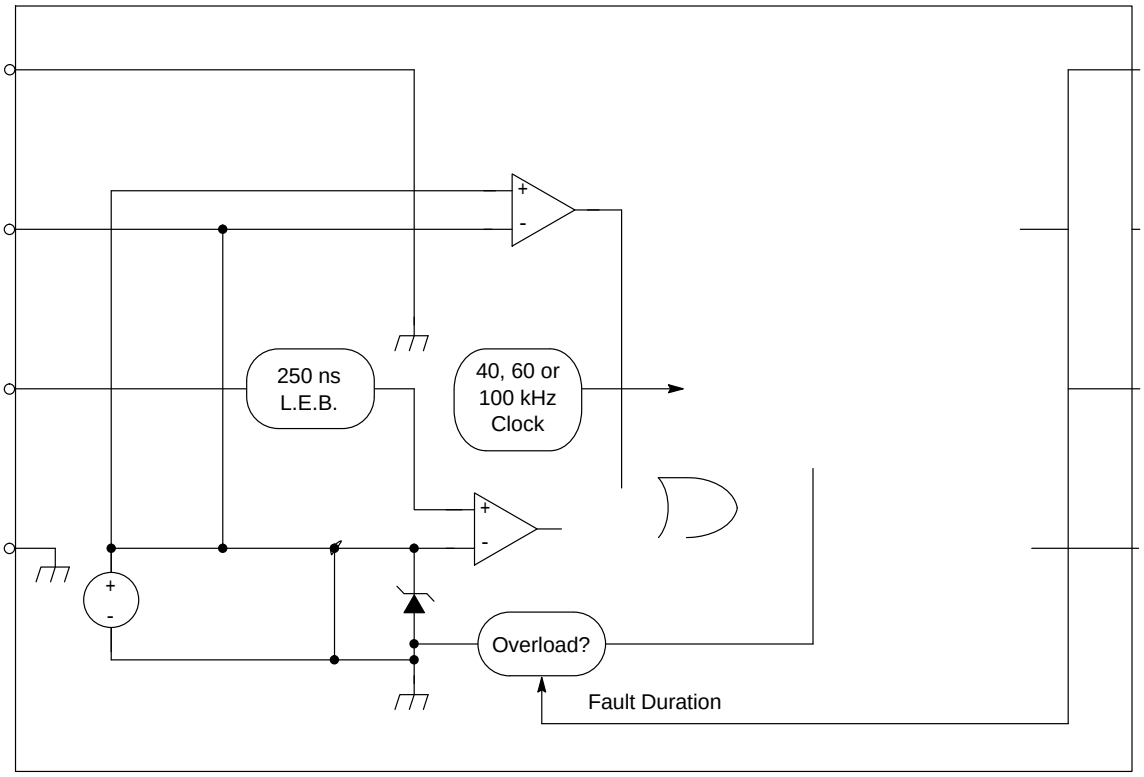
PIN CONNECTIONS



ORDERING INFORMATION

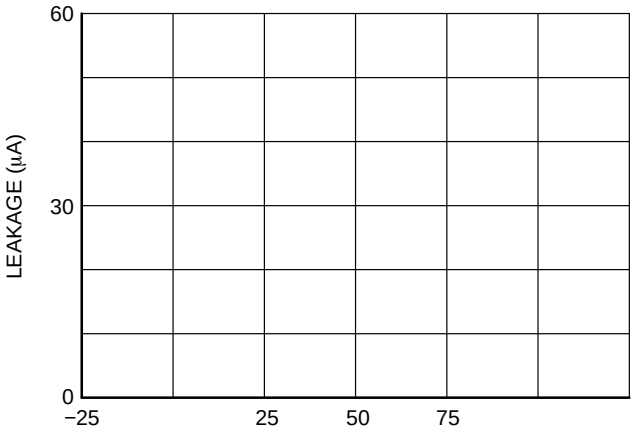
See detailed ordering and shipping information on page 14 of this data sheet.

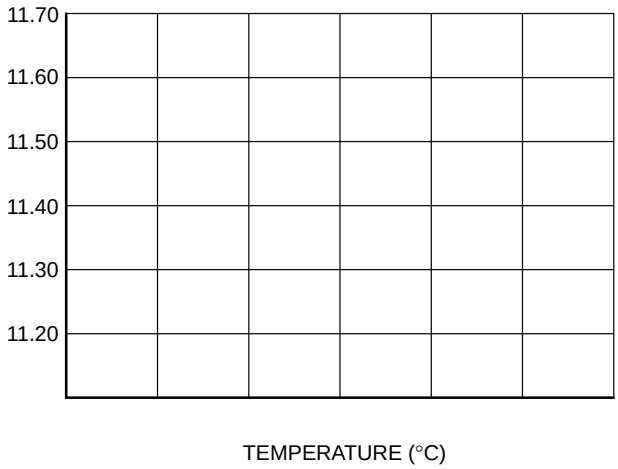


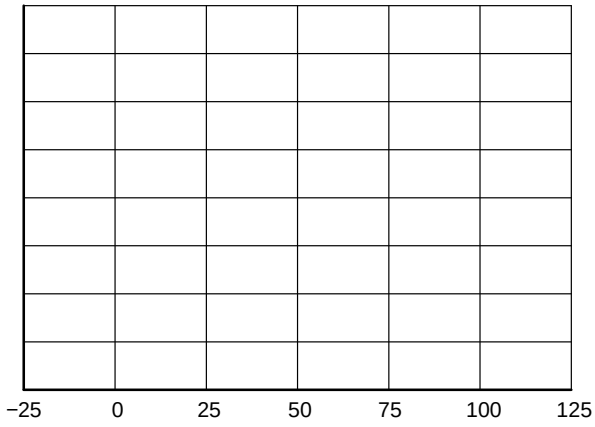

+
-
250 ns
L.E.B.
40, 60 or
100 kHz
Clock
+
-
+
-
Overload?
Fault Duration

ELECTRICAL CHARACTERISTICS (For typical values T_J = +25°C, for min/max values T_J = −25°C to +125°C, Max T_J = 150°C, V_{CC}= 11 V unless otherwise noted)

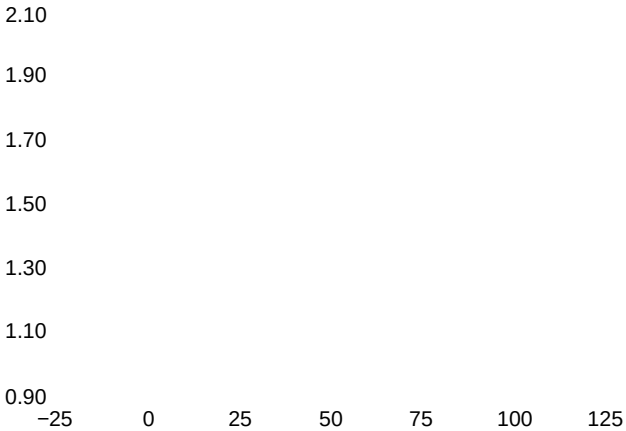
Rating	Pin	Symbol	Min	Typ	Max	Unit
DYNAMIC SELF−SUPPLY (All Frequency Versions, Otherwise Noted)						
V_{CC} Increasing Level at Which the Current Source Turns−off	6	V_{CCOFF}	10.3	11.4	12.5	V
V_{CC} Decreasing Level at Which the Current Source Turns−on	6	V_{CCON}	8.8	9.8	11	V
V_{CC} Decreasing Level at Which the Latchoff Phase Ends	6	$V_{CClatch}$	−	6.3	−	V
Internal IC Consumption, No Output Load on Pin 5	6	I_{CC1}	−	710	880 Note 1	μA
Internal IC Consumption, 1 nF Output Load on Pin 5, F_{SW} = 40 kHz	6	I_{CC2}	−	1.2	1.4 Note 2	mA
Internal IC Consumption, 1 nF Output Load on Pin 5, F_{SW} = 60 kHz	6	I_{CC2}	−	1.4	1.6 Note 2	mA
Internal IC Consumption, 1 nF Output Load on Pin 5, F_{SW} = 100 kHz	6	I_{CC2}	−	1.9	2.2 Note 2	mA
Internal IC Consumption, Latchoff Phase	6	I_{CC3}	−	350	−	μA
INTERNAL CURRENT SOURCE						
High−voltage Current Source, V_{CC} = 10 V	8	I_{C1}	2.8	4.0	−	mA
High−voltage Current Source, V_{CC} = 0 V	8	I_{C2}	−	4.9	−	mA
DRIVE OUTPUT						
Output Voltage Rise−time @ CL = 1 nF, 10−90% of Output Signal	5	T_r	−	67	−	ns
Output Voltage Fall−time @ CL = 1 nF, 10−90% of Output Signal	5	T_f	−	28	−	ns
Source Resistance (drive = 0, Vgate = V_{CCHMAX} − 1 V)	5	R_{OH}	27	40	61	Ω
Sink Resistance (drive = 11 V, Vgate = 1 V)	5	R_{OL}	5	12	25	Ω
CURRENT COMPARATOR (Pin 5 Un−loaded)						
Input Bias Current @ 1 V Input Level on Pin 3	3	I_{IB}	−	0.02	−	μA
Maximum internal Current Setpoint	3	I_{Limit}	0.8	0.9	1.0	V
Default Internal Current Setpoint for Skip Cycle Operation	3	I_{Lskip}	−	350	−	mV

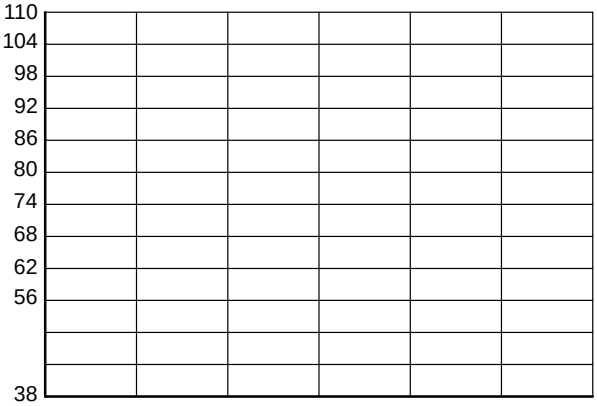

60
30
0
LEAKAGE (μA)
−25
25
50
75


11.70
11.60
11.50
11.40
11.30
11.20
TEMPERATURE (°C)


−25
0
25
50
75
100
125

750


2.10
1.90
1.70
1.50
1.30
1.10
0.90
−25
0
25
50
75
100
125


110
104
98
92
86
80
74
68
62
56
38

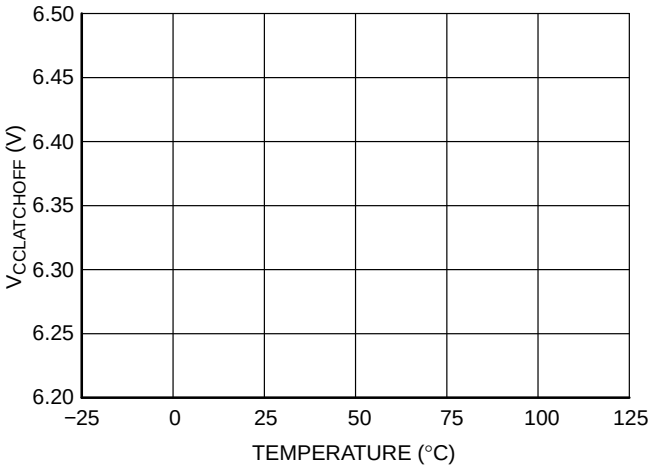


Figure 9. V_{CC} Latchoff vs. Temperature

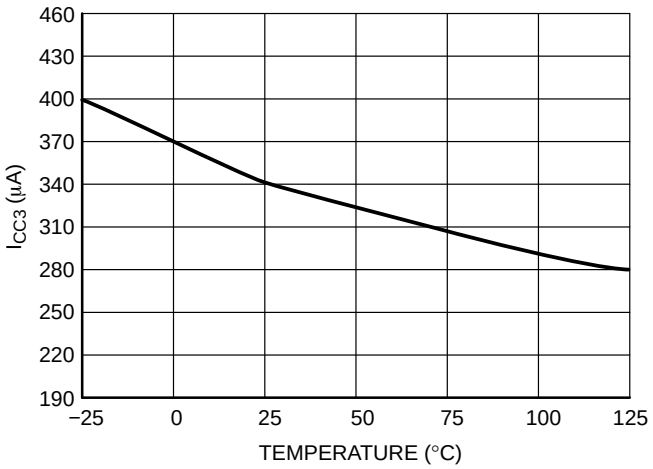


Figure 10. I_{CC3} vs. Temperature

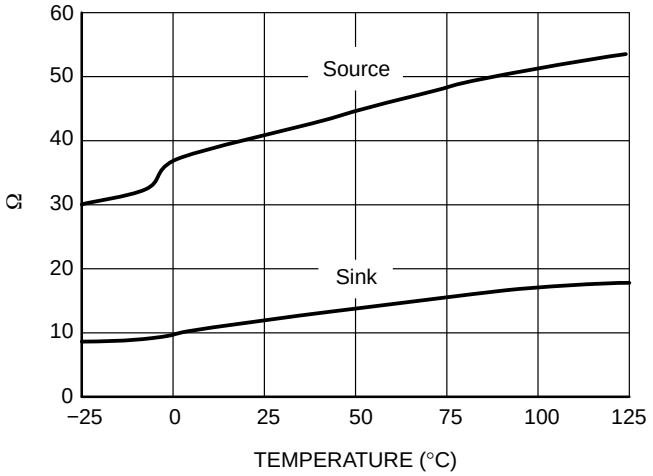


Figure 11. DRV Source/Sink Resistances

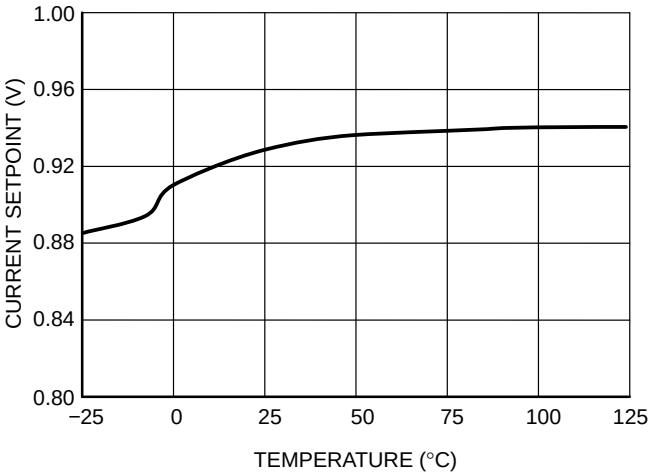


Figure 12. Current Sense Limit vs. Temperature

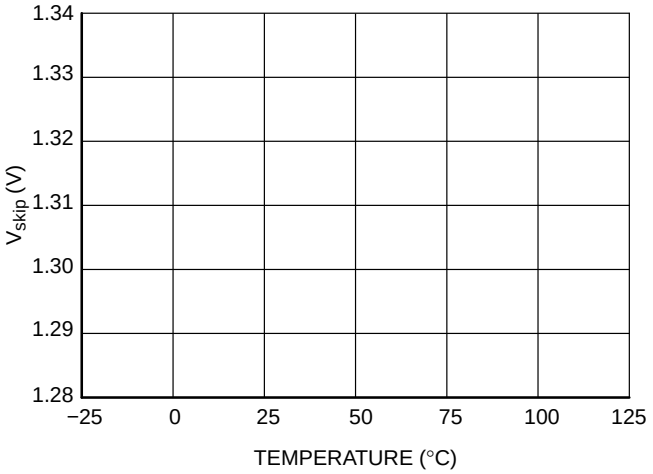


Figure 13. V_{skip} vs. Temperature

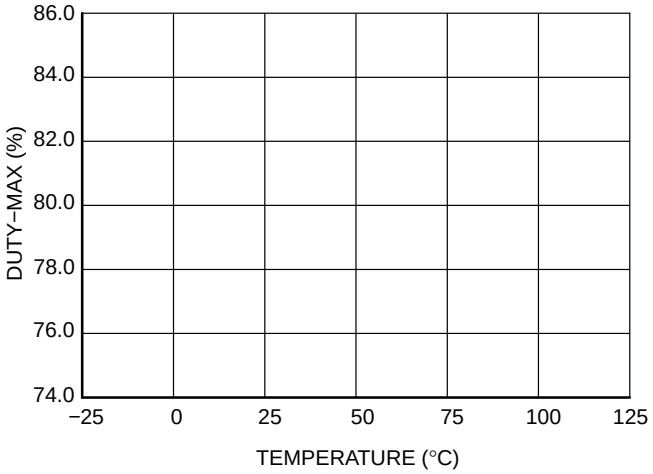


Figure 14. Max Duty Cycle vs. Temperature

APPLICATIONS INFORMATION

INTRODUCTION

The NCP1200 implements a standard current mode architecture where the switch−off time is dictated by the peak current setpoint. This component represents the ideal candidate where low part−count is the key parameter, particularly in low−cost AC−DC adapters, auxiliary supplies etc. Due to its high−performance High−Voltage technology, the NCP1200 incorporates all the necessary components normally needed in UC384X based supplies: timing components, feedback devices, low−pass filter and self−supply. This later point emphasizes the fact that ON Semiconductor's NCP1200 does NOT need an auxiliary winding to operate: the product is naturally supplied from the high−voltage rail and delivers a V_{CC} to the IC. This system is called the Dynamic Self−

3. Permanently force the V_{CC} level above V_{CCH} with an auxiliary winding. It will automatically disconnect the internal startup source and the IC will be fully self−supplied from this winding.

Power Dissipation

The NCP1200 is directly supplied from the DC rail through the internal DSS circuitry. The current flowing through the DSS is therefore the direct image of the NCP1200 current consumption. The total power dissipation

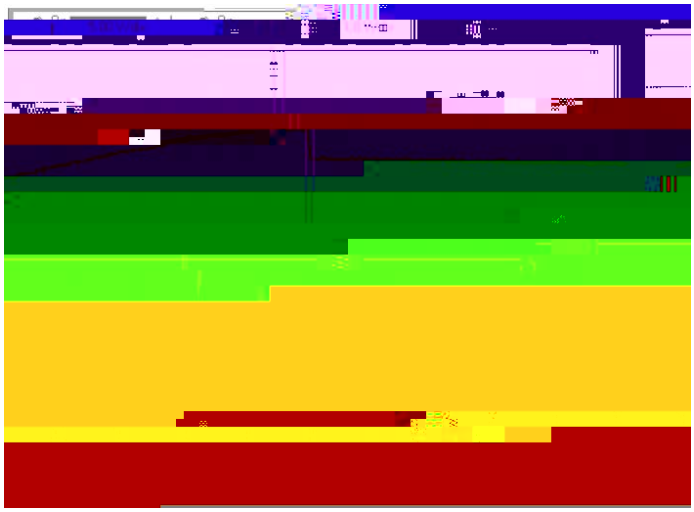


Figure 21. A negative spike takes place on the Bulk capacitor at the switch−off sequence

Simple and inexpensive cures exist to prevent from internal parasitic SCR activation. One of them consists in inserting a resistor in series with the high−voltage pin to keep the negative current to the lowest when the bulk becomes negative (Figure 22). Please note that the negative spike is clamped to –2 x Vf due to the diode bridge. Please refer to AND8069/D for power dissipation calculations.

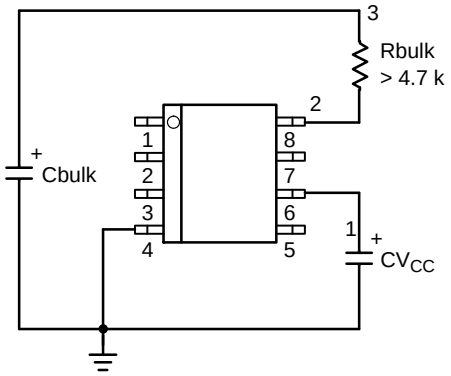


Figure 22. A simple resistor in series avoids any latchup in the controller

Another option (Figure 23) consists in wiring a diode from V_{CC} to the bulk capacitor to force V_{CC} to reach UVLOlow sooner and thus stops the switching activity before the bulk capacitor gets deeply discharged. For security reasons, two diodes can be connected in series.

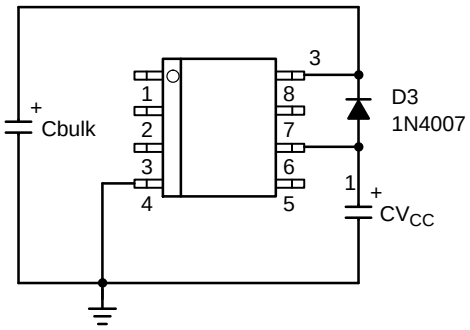
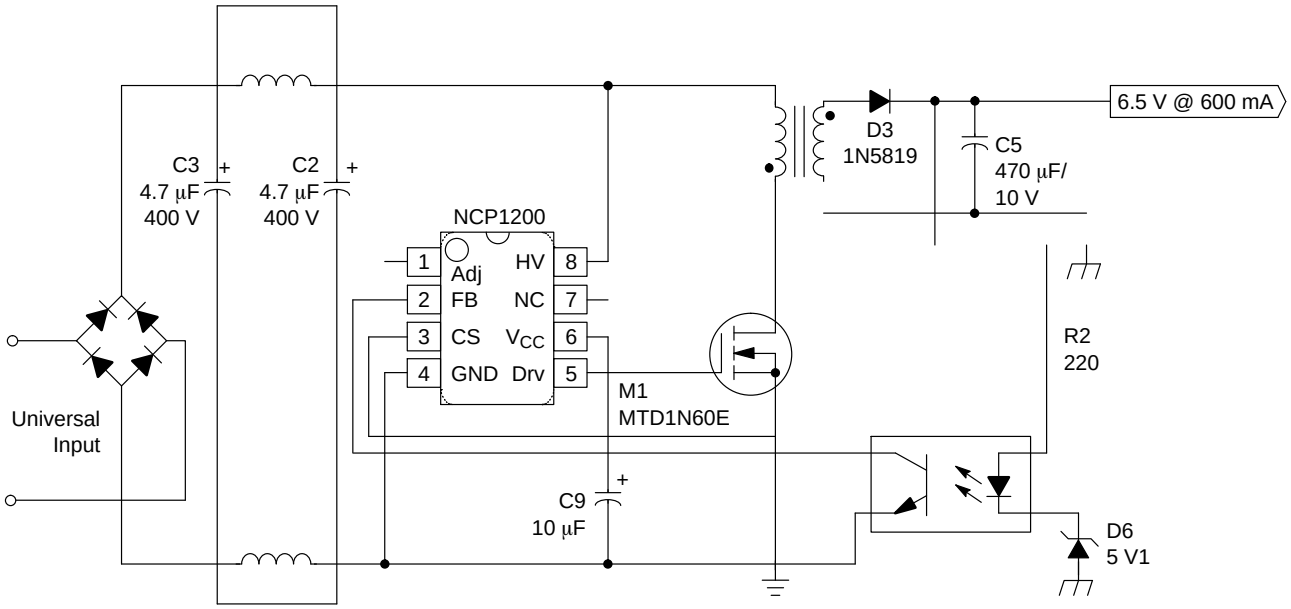


Figure 23. or a diode forces V_{CC} to reach UVLOlow sooner

A Typical Application

Figure 24 depicts a low−cost 3.5 W AC−DC 6.5 V wall adapter. This is a typical application where the wall−pack must deliver a raw DC level to a given internally regulated apparatus: toys, calculators, CD players etc. Due to the inherent short−circuit protection of the NCP1200, you only need a bunch of components around the IC, keeping the final cost at an extremely low level. The transformer is available from different suppliers as detailed on the following page.


C3
4.7 μF
400 V
C2
4.7 μF
400 V
NCP1200
1
Adj
2
FB
3
CS
4
GND
HV
8
NC
7
VCC
6
Drv
5
D3
1N5819
C5
470 μF/
10 V
6.5 V @ 600 mA
R2
220
M1
MTD1N60E
C9
10 μF
D6
5 V1
Universal
Input

Improving the Output Drive Capability

The NCP1200 features an asymmetrical output stage used to soften the EMI signature. Figure 25 depicts the way the driver is internally made:

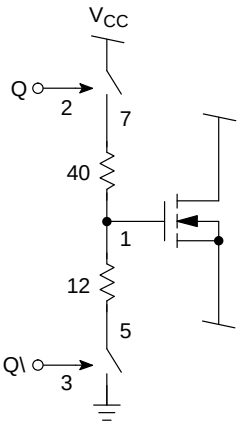


Figure 25. The higher ON resistor slows down the MOSFET while the lower OFF resistor ensures fast turn−off.

In some cases, it is possible to expand the output drive capability by adding either one or two bipolar transistors. Figures 26, 27, and 28 give solutions whether you need to improve the turn−on time only, the turn−off time or both. Rd is there to damp any overshoot resulting from long copper traces. It can be omitted with short connections. Results showed a rise fall time improvement by 5X with standard 2N2222/2N2907:

If the leakage inductance is kept low, the MTD1N60E can withstand *accidental* avalanche energy, e.g. during a high−voltage spike superimposed over the mains, without the help of a clamping network. If this leakage path permanently forces a drain−source voltage above the MOSFET BVdss (600 V), a clamping network is mandatory and must be built around Rclamp and Clamp. Dclamp shall react extremely fast and can be a MUR160 type. To calculate the component values, the following formulas will help you:

$$R_{clamp} = \frac{2 \cdot V_{clamp} \cdot (V_{clamp} - (V_{out} + Vf\,sec) \cdot N)}{L_{leak} \cdot Ip^2 \cdot Fsw}$$

$$C_{clamp} = \frac{V_{clamp}}{V_{ripple} \cdot Fsw \cdot R_{clamp}}$$

with:

V_{clamp}: the desired clamping level, must be selected to be between 40 V to 80 V above the reflected output voltage when the supply is heavily loaded.

V_{out} + Vf: the regulated output voltage level + the secondary diode voltage drop

L_{leak}: the primary leakage inductance

N: the Ns:Np conversion ratio

F_{SW}: the switching frequency

V_{ripple}: the clamping ripple, could be around 20 V

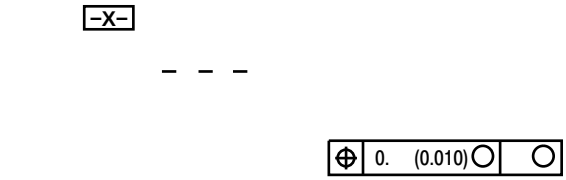
Another option lies in implementing a snubber network which will damp the leakage oscillations but also provide more capacitance at the MOSFET's turn−off. The peak voltage at which the leakage forces the drain is calculated by:

$$V_{max} = Ip \cdot \sqrt{\frac{L_{leak}}{C_{lump}}}$$

where C_{lump} represents the total parasitic capacitance seen at the MOSFET opening. Typical values for Rsnubber and Csnubber in this 4W application could respectively be 1.5 kΩ and 47 pF. Further tweaking is nevertheless necessary to tune the dissipated power versus standby power.

Available Documents

"Implementing the NCP1200 in Low−il0sTT6 1AC/TT5 1 Tf1.



C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0	8	0	8
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

0. (0.010) 1 0 1 1 0 0 1 . 0 0 0 0 . 1 1 0 1 1 . 1 0 . 0 0 0 1 . 1 1 0 0 1 1 0 ( ) 0 1 . 1 1 0 0 1 1 . 1 1 . 1 0 0 . 0 0 0 . 1 1 . 1 0 0 . 0 0 0 1 1 . 1 0 0 0 1 0 0 0 0 .)