DATA SHEET
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High-Voltage Switcher for Low Power Offline SMPS

NCP10670B, NCP10671B, NCP10672B

The NCP1067X products integrate a fixed frequency current mode controller with a 700 V MOSFET. Available in a SOICĭ7 package, the NCP1067X offer a high level of integration, including softĭstart, frequencyĭjittering, shortĭcircuit protection, skipĭcycle, ramp compensation, and a Dynamic SelfĭSupply (eliminating the need for an auxiliary winding).

During nominal load operation, the NCP1067X switches at one of the available frequencies (60 or 100 kHz). When the output power demand diminishes, the IC automatically enters into a skip mode to reduce the standby consumption down.

Protection features include: a timer to detect an overload or a shortĭcircuit event, Overvoltage Protection with autoĭrecovery.

For improved standby performance, the connection of an auxiliary winding or supplying the IC from the output, stops the DSS operation and helps to reduce input power consumption below 25 mW at high line.

NCP1067x can be seamlessly used both in nonĭisolated and in isolated topologies.

Features

- Builtĭin 700 V MOSFET with $R_{DS(on)}$ of 34 Ω (NCP10670/1) and 12 Ω (NCP10672)
- Large Creepage Distance Between HighĭVoltage Pins
- CurrentĭMode Fixed Frequency Operation – 60 or 100 kHz
- Fixed Ramp Compensation
- Direct Feedback Connection for Nonĭisolated Converter
- SkipĭCycle Operation at Low Peak Currents Only
- Dynamic SelfĭSupply: No Need for an Auxiliary Winding
- Internal 4 ms SoftĭStart
- AutoĭRecovery Output Short Circuit Protection with TimerĭBased Detection
- Autoĭ

Table 1. PRODUCTS INFOS & INDICATIVE MAXIMUM OUTPUT POWER

Product	$R_{DS(on)}$	$I_{IPK(0)}$	230 Vac ±15%		85 − 265 Vac	
			Adapter	OpenFrame	Adapter	OpenFrame
NCP10670 60 kHz	34 Ω	100 mA	1.1 W	2.7 W	0.6 W	1.5 W
NCP10671 60 kHz	34 Ω	250 mA	2.7 W	6.7 W	1.5 W	3.7 W
NCP10672 100 kHz	12 Ω	780 mA	6.2 W	15.5 W	3.3 W	7.8 W

1. Informative values only, with T_{amb} = 25 C, T_{case} = 100 C, Self supply via Auxiliary winding and circuit mounted on minimum copper area as recommended.

Table 2. SELECTION TABLE

Device	Frequency	$R_{DS(on)}$	$I_{IPK(0)}$	Package Type
NCP10670	60 kHz	34	100 mA	SOIC−7 (Pb−Free)
NCP10670	100 kHz	34	100 mA	
NCP10671	60 kHz	34	250 mA	
NCP10671	100 kHz	34	250 mA	
NCP10672	60 kHz	12	780 mA	
NCP10672	100 kHz	12	780 mA	

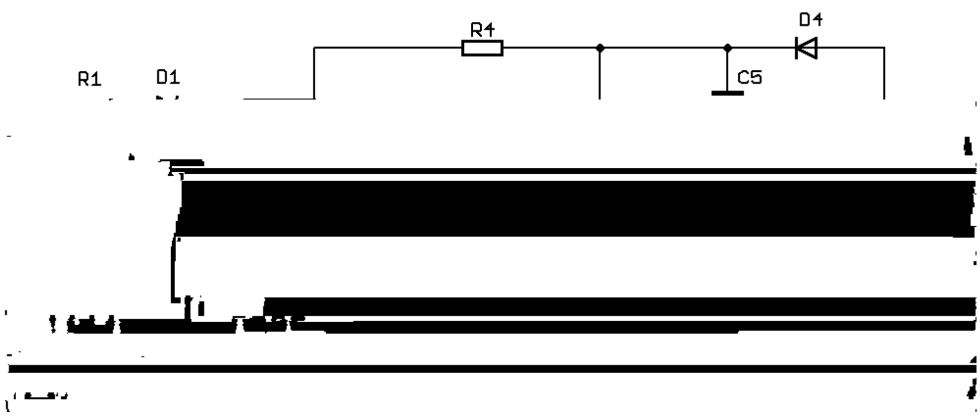


Figure 1. Typical Non−Isolated Application (Buck Converter)

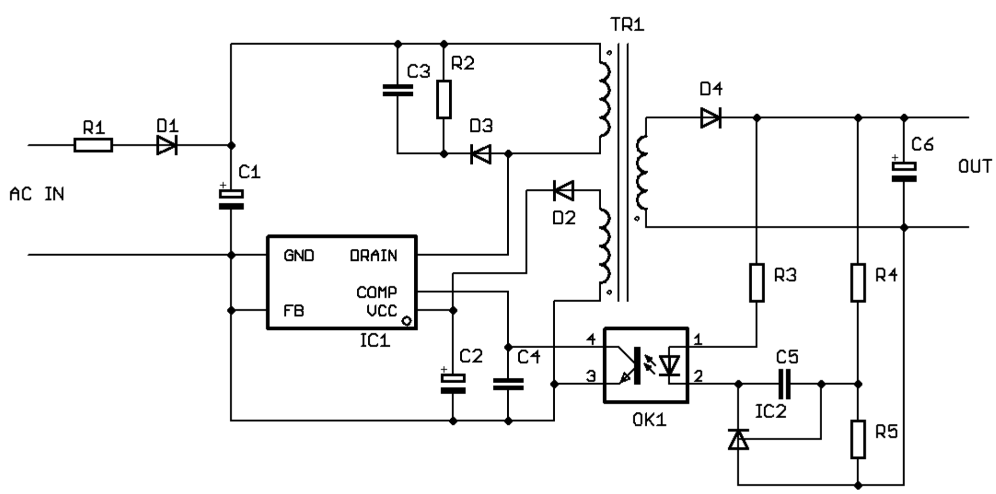


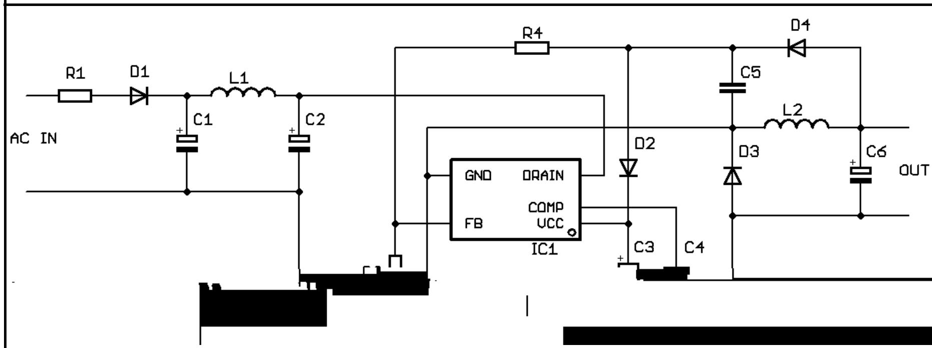
Figure 2. Typical Isolated Application (Flyback Converter)

PIN DESCRIPTION

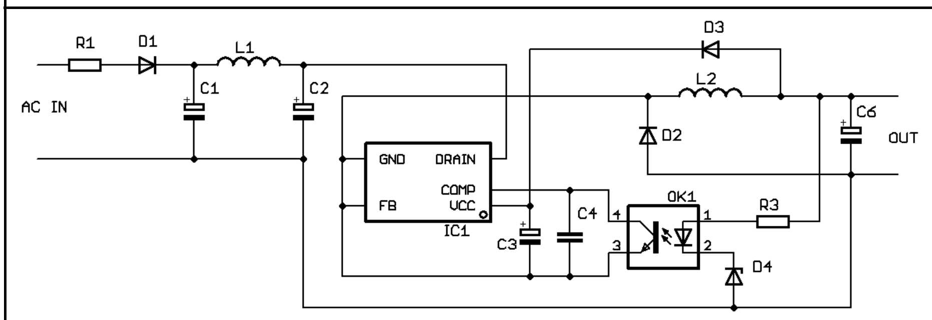
Pin No. SOIC−7	Name	Function	Description
1	V_{CC}	Powers the internal circuitry	This pin is connected to an external capacitor. The V_{CC} includes an auto−recovery over voltage protection.
2	Comp	Compensation	The error amplifier output is available on this pin. The network connected between this pin and ground adjusts the regulation loop bandwidth. Also, by connecting an opto−coupler to this pin, the peak current set point is adjusted accordingly to the output power demand.
3			This missing pin ensures adequate creepage distance
4	Drain	Drain connection	The internal drain MOSFET connection
5−7	GND	The IC Ground	
8	FB	Feedback signal input	This is the inverting input of the trans conductance error amplifier. It is normally connected to the switching power supply output through a resistor divider.

Table 3. TYPICAL APPLICATION

Non Isolated Buck

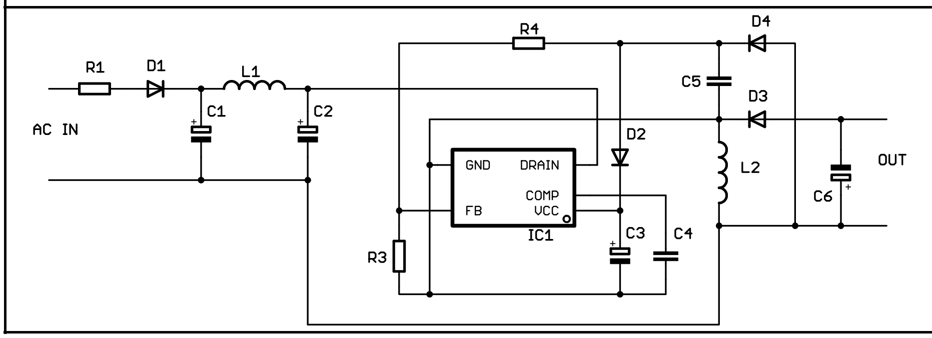


If the output voltage is above 9.0 V typ. (between $V_{CC(on)}$ level and V_{OVP} level) VCC is supplied from output via D2
If the output voltage is below 9.0 V, D2 is redundant, the IC is supplied from DSS
Direct feedback, resistive divider formed by R3, R4 sets output voltage



If the output voltage is above 9.0 V typ. (between $V_{CC(on)}$ level and V_{OVP} level) VCC is supplied from output via D3
If the output voltage is below 9.0 V, D3 is redundant, the IC is supplied from DSS
Optocoupler feedback, output voltage is set by D4

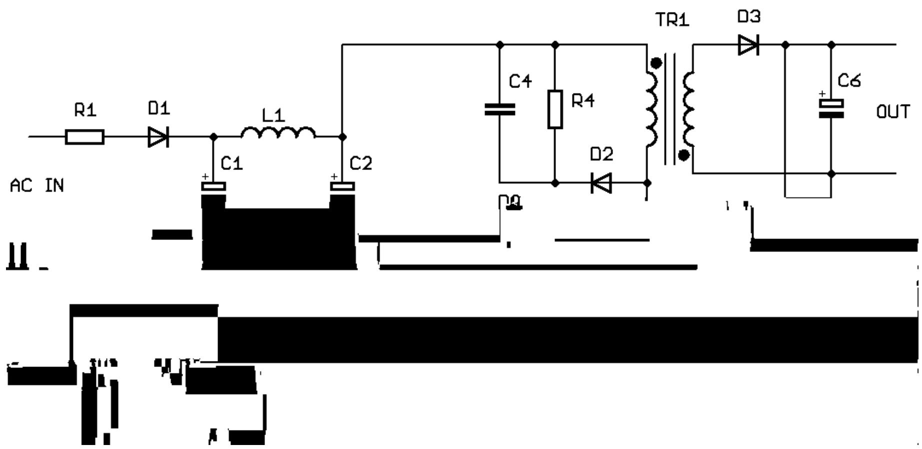
Non Isolated Buck−Boost (Invert)



If the output voltage is above 9.0 V typ. between $V_{CC(on)}$ level and V_{OVP} level, VCC is supplied from output via D2
If the output voltage is below 9.0 V, D2 is redundant, the IC is supplied from DSS
Direct feedback, resistive divider formed by R3, R4 sets output voltage

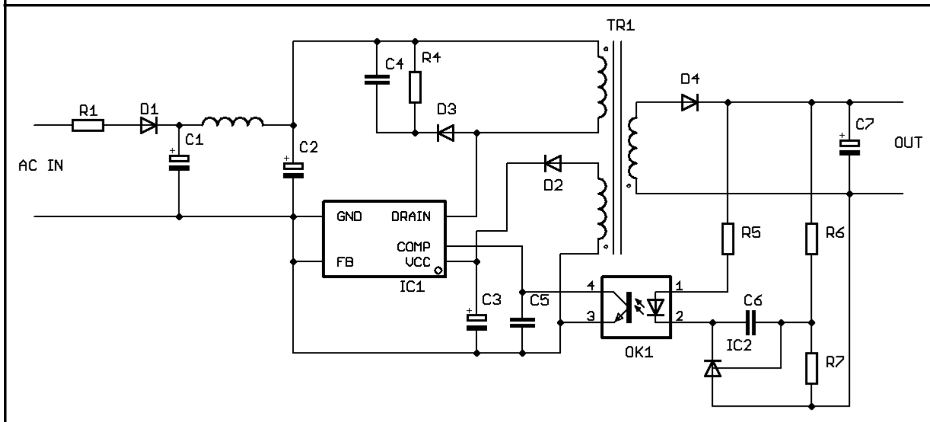
Table 3. TYPICAL APPLICATION

Non Isolated Flyback

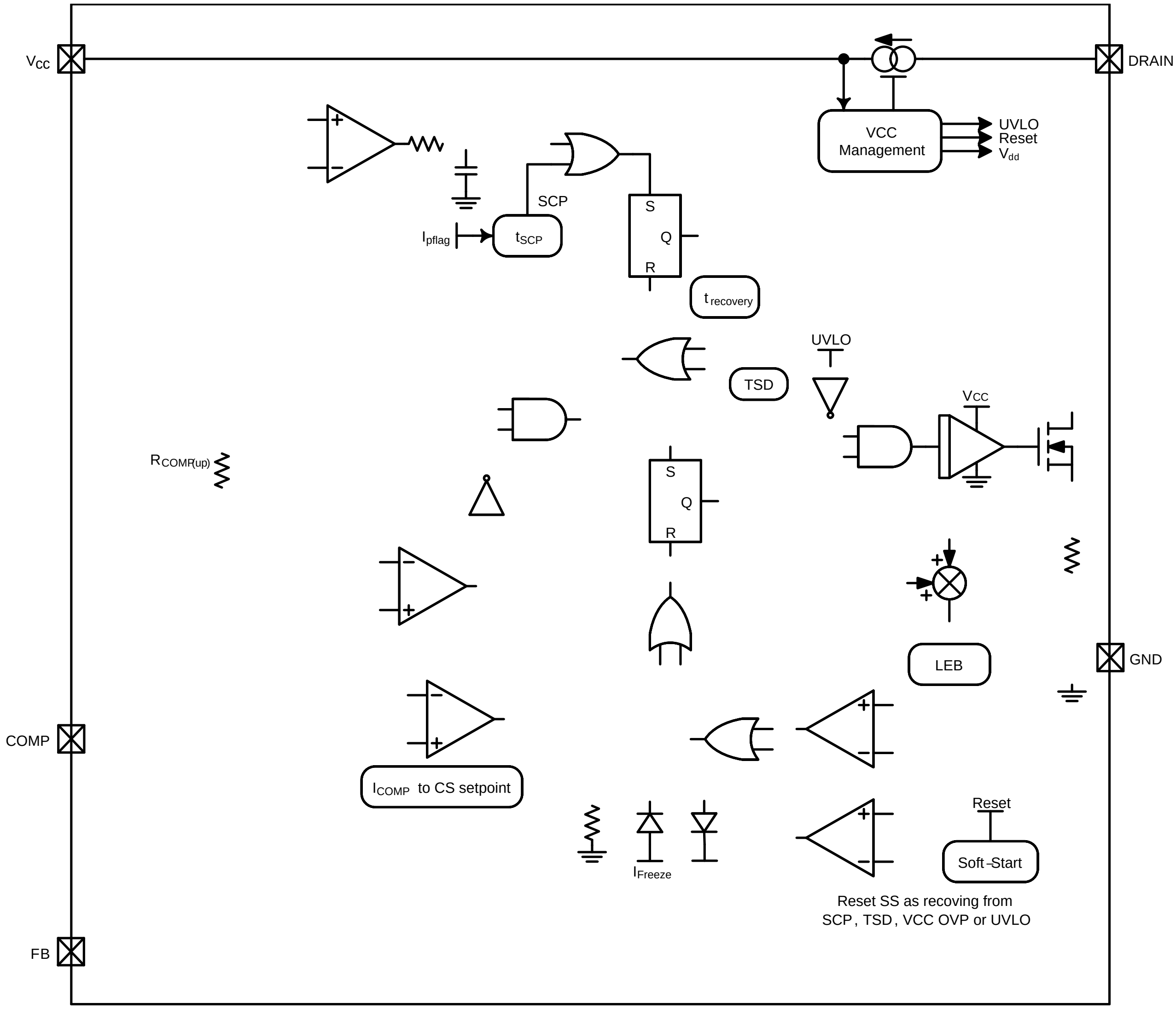


If the output voltage is above 9.0 V typ. between $V_{CC(on)}$ level and V_{OVP} level –VCC supplied from output via D4
If the output voltage is below 9.0 V, D4 is redundant, the IC is supplied from DSS
Resistive divider formed by R2, R3 sets output voltage

Isolated Flyback



VCC supplied from auxiliary winding
Optocoupler feedback, resistive divider formed by R6, R7 sets output voltage


VCC
DRAIN
VCC
Management
UVLO
Reset
Vdd
SCP
S
Q
R
Ipflag
tSCP
t recovery
UVLO
TSD
VCC
RCOMP(up)
S
Q
R
LEB
GND
COMP
ICOMP to CS setpoint
IFreeze
Reset
Soft-Start
Reset SS as recoving from
SCP, TSD, VCC OVP or UVLO
FB

MAXIMUM RATINGS (All voltages related to GND terminal)

Symbol	Parameter	Rating	Units
V_{CC}	Power supply voltage, V_{CC} pin, continuous voltage	−0.3 to 20	V
Vinmax	Voltage on all pins, except Drain and V_{CC}		

ELECTRICAL CHARACTERISTICS

(Tj = 25 C, for min/max values Tj = −40 C to +125 C, Vcc = 14 V unless otherwise noted)

Symbol	Rating	Pin	Min	Typ	Max	Unit
SUPPLY SECTION AND V_{CC} MANAGEMENT						
$V_{CC(on)}$	V_{CC} increasing level at which the switcher starts operation	1	8.4	9.0	9.5	V
$V_{CC(min)}$	V_{CC} decreasing level at which the HV current source restarts	1	7.0	7.5	7.8	V
$V_{CC(off)}$	V_{CC} decreasing level at which the switcher stops operation (UVLO)	1	6.7	7.0	7.2	V
I_{CC1}	Internal IC consumption, NCP10670 switching at 60 kHz Internal IC consumption, NCP10670 switching at 100 kHz Internal IC consumption, NCP10671 switching at 60 kHz Internal IC consumption, NCP10671 switching at 100 kHz Internal IC consumption, NCP10672 switching at 60 kHz Internal IC consumption, NCP10672 switching at 100 kHz	1	– – – – – –	0.84 0.88 0.84 0.88 0.91 1.00	1.05 1.10 1.05 1.10 1.15 1.25	mA
I_{CCskip}	Internal IC consumption, COMP is 0 V (No switching on MOSFET)	1	–	340	–	μA
POWER SWITCH CIRCUIT						
$R_{DS(on)}$	Power Switch Circuit on−state resistance NCP10670, NCP10671 (Id = 50 mA) Tj = 25 C Tj = 125 C NCP10672 (Id = 50 mA) Tj = 25 C Tj = 125 C	4	 – – – –	 34 65 12 22	 41 72 14 24	 Ω Ω Ω Ω
BV_{DSS}	Power Switch Circuit & Startup breakdown voltage ($ID_{(off)}$ = 120 μA, Tj = 25 C)	4	700	–	–	V
$I_{DSS(off)}$	Power Switch & Startup breakdown voltage off−state leakage current Tj = 125 C (Vds = 700 V) Tj = 25 C (Vds = 700 V)	4	 – –	 7 1	 – –	 μA μA
 t_r t_f	Switching characteristics (R_L = 50 Ω, V_{DS} set for I_{drain} = 0.7 x Ilim) Turn−on time (90% − 10%) Turn−off time (10% − 90%)	4	 – –	 20 10	 – –	 ns ns
$t_{on(min)}$	Minimum on time NCP10670 NCP10671 NCP10672	4	 – – –	 200 200 230	 – – –	 ns ns ns
INTERNAL START−UP CURRENT SOURCE						
I_{start1}	High−voltage current source, V_{CC} = $V_{CC(on)}$ – 200 mV	4	4	8	12	mA
I_{start2}	High−voltage current source, V_{CC} = 0 V	4	–	0.4	–	mA
V_{CCTH}	VCC Transient level for Istart1 to Istart2 toggling point	1	–	1.2	–	V
$V_{start(min)}$	Minimum startup voltage, V_{CC} = 0 V	4	–	–	22	V
CURRENT COMPARATOR						
I_{IPK}	Maximum internal current setpoint at 50% duty cycle FB = 2 V, Tj = 25 C NCP10670 NCP10671 NCP10672	 – – –	 – – –	 83 208 650	 – – –	 mA mA mA
$I_{IPK(0)}$	Maximum internal current setpoint at beginning of switching cycle FB = 2 V, Tj = 25 C NCP10670 NCP10671 NCP10672	 – – –	 85 223 702	 100 250 780		

ELECTRICAL CHARACTERISTICS
(Tj = 25 C, for min/max values Tj = −40 C to +125 C, Vcc = 14 V unless otherwise noted) (continued)

Symbol	Rating	Pin	Min	Typ	Max	Unit
[redacted]						
[redacted]				120 250 710	– – –	mA mA mA
[redacted]				4	–	ms
[redacted]				70	–	ns
[redacted]				130 130 160	– – –	ns ns ns
[redacted]						
[redacted]				60	66	kHz
[redacted]				100	110	kHz
[redacted]				6	–	%
[redacted]				300	–	Hz
[redacted]				66	72	%
[redacted]						
[redacted]				3.3	3.4	V
[redacted]				1	–	µA
[redacted]				2	–	mS
[redacted]				+150/−150	–	µA

[redacted]

ELECTRICAL CHARACTERISTICS
(Tj = 25 C, for min/max values Tj = −40 C to +125 C, Vcc = 14 V unless otherwise noted) (continued)

Symbol	Rating	Pin	Min	Typ	Max	Unit

TYPICAL CHARACTERISTICS (continued)

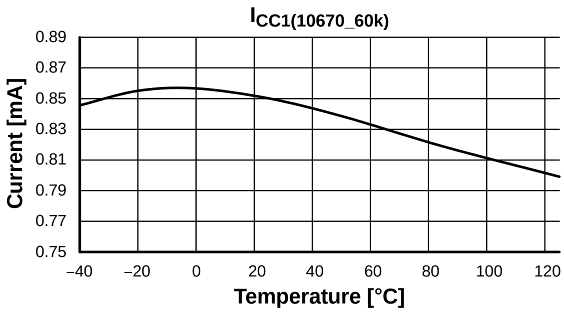


Figure 9. $I_{CC1\ (10670\_60k)}$ vs. Temperature

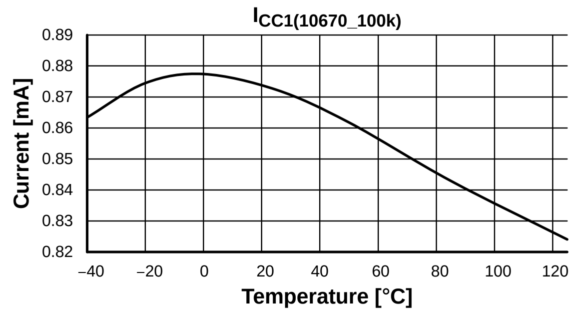


Figure 10. $I_{CC1\ (NCP10670\_100k)}$ vs. Temperature

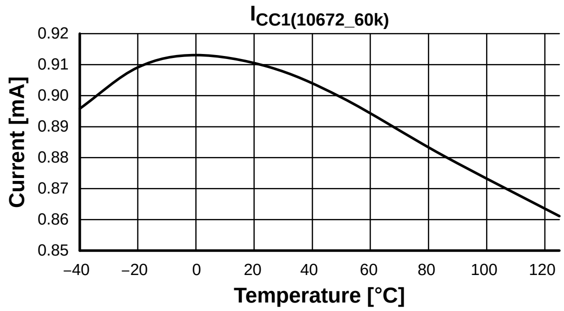


Figure 11. $I_{CC1\ (10672\_60k)}$ vs. Temperature

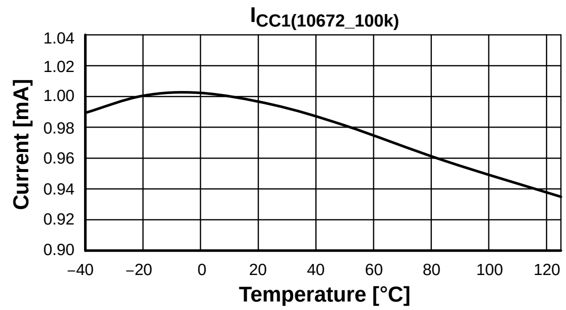


Figure 12. $I_{CC1\ (10672\_100k)}$ vs. Temperature

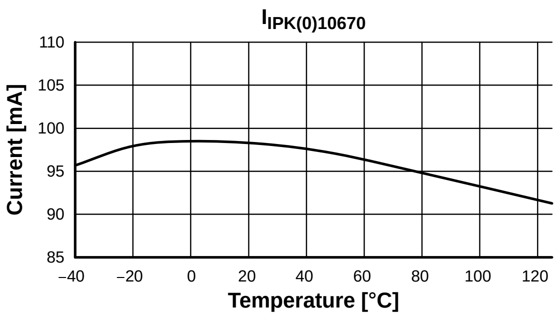
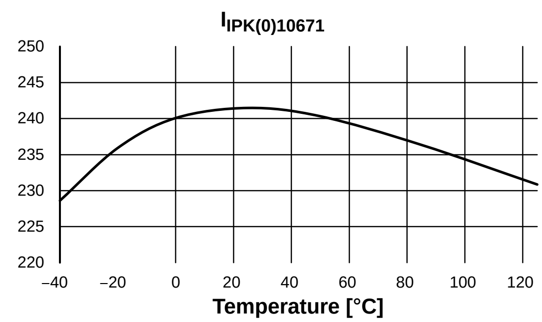
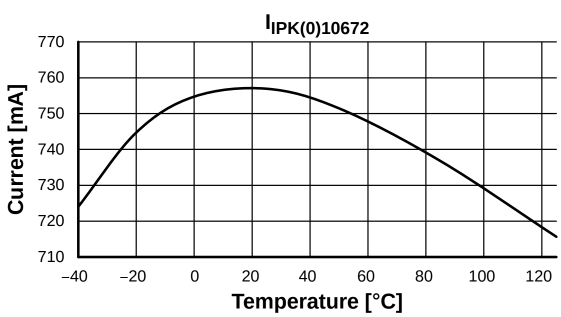
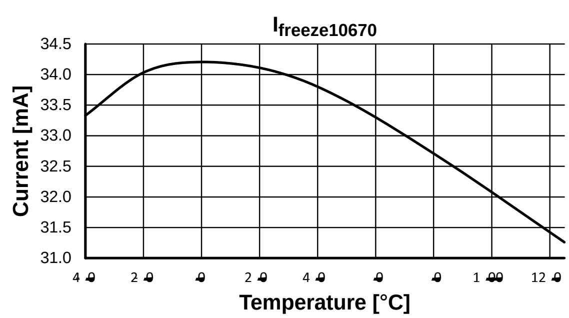


Figure 13. IIPK(vs. TemperaturewwwPK(vs. Temperaturel







TYPICAL CHARACTERISTICS (continued)

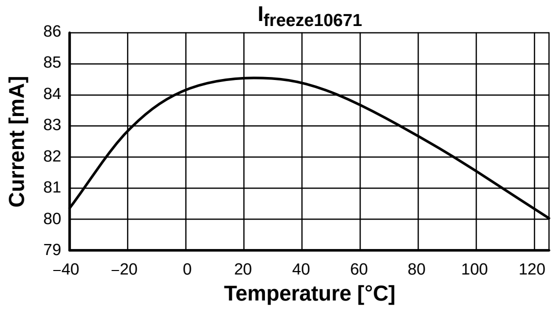


Figure 17. $I_{freeze10671}$ vs. Temperature

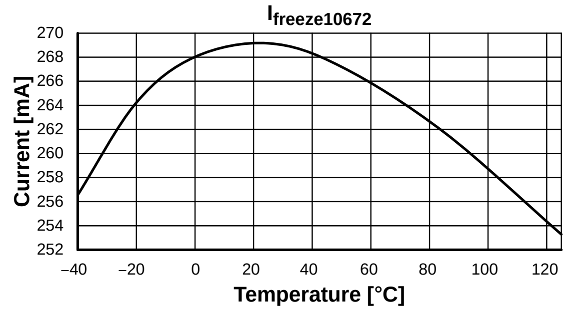


Figure 18. $I_{freeze10672}$ vs. Temperature

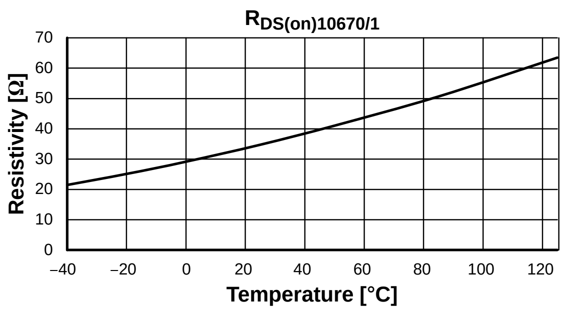


Figure 19. $R_{DS(on)10670/1}$ vs. Temperature

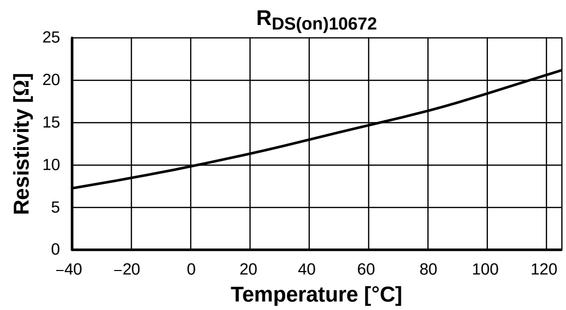


Figure 20. $R_{DS(on)10672}$ vs. Temperature

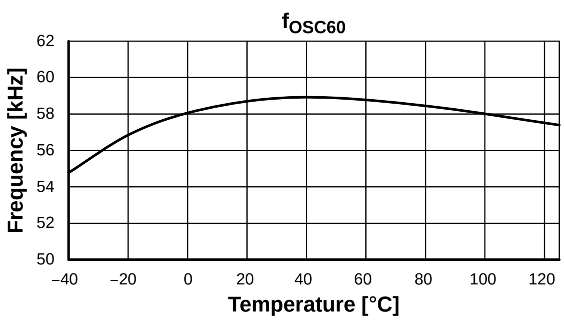


Figure 21. f_{OSC60} vs. Temperature

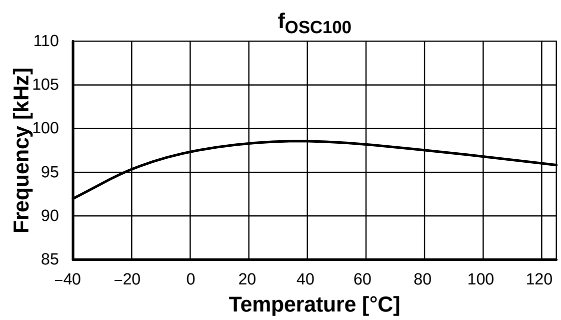


Figure 22. f_{OSC100} vs. Temperature

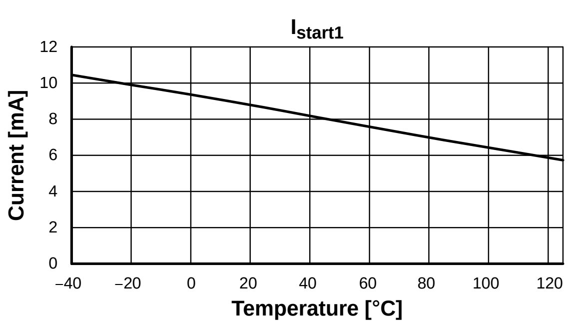


Figure 23. I_{start1} vs. Temperature

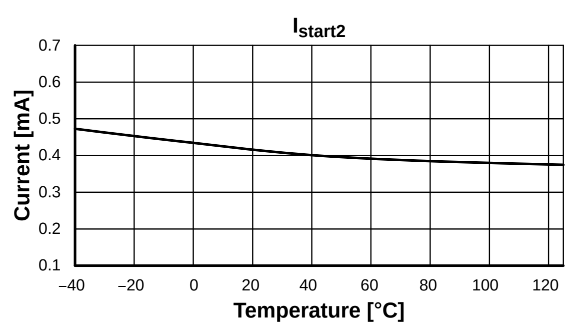


Figure 24. I_{start2} vs. Temperature

TYPICAL CHARACTERISTICS (continued)

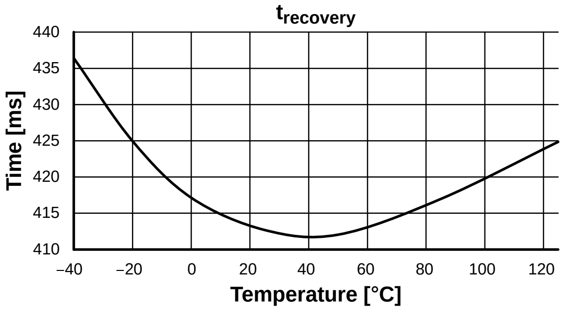


Figure 25. $t_{recovery}$ vs. Temperature

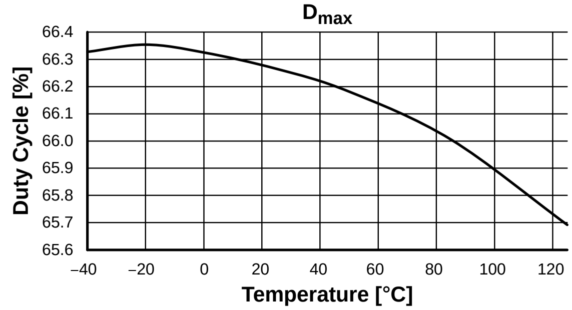
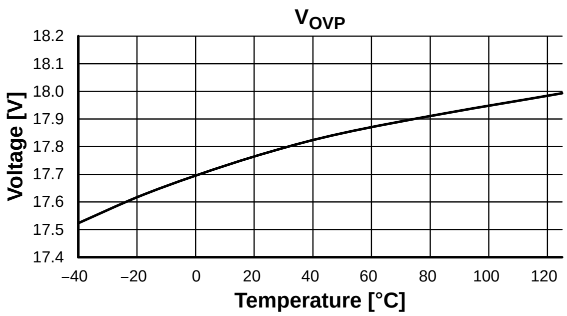
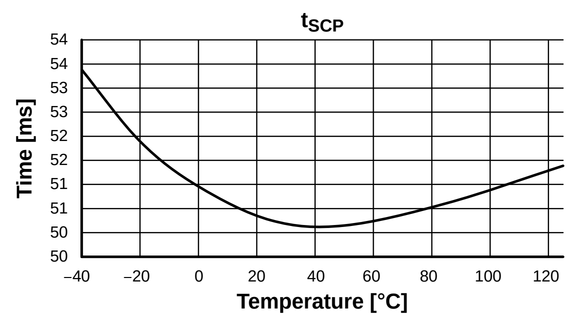
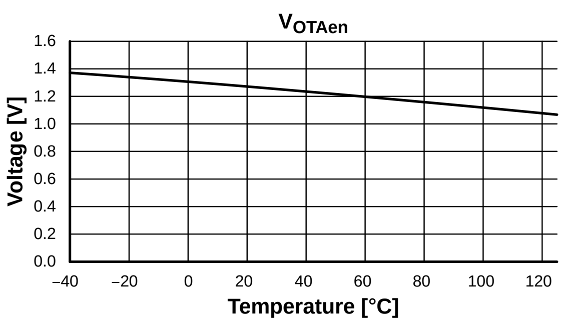
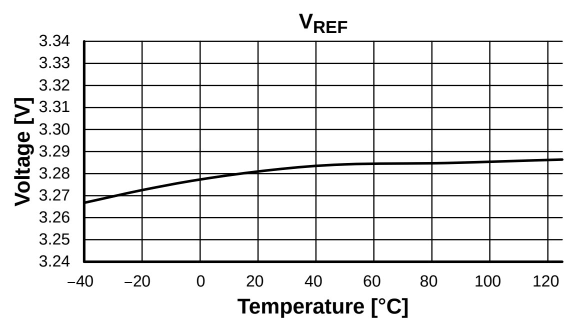


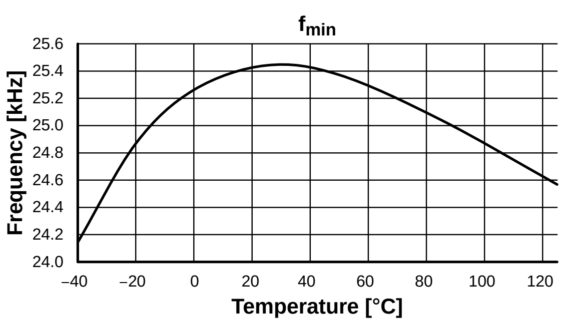
Figure 26. D

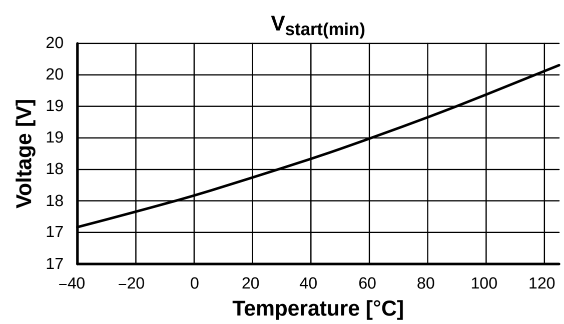












APPLICATION INFORMATION

INTRODUCTION

The NCP1067X offers a complete current ̆mode control solution. The component integrates everything needed to build a rugged and cost effective Switch ̆Mode Power Supply (SMPS) featuring low standby power. The Quick Selection Table is on details the differences between references, mainly peak current setpoints, $R_{DS(on)}$ value and operating frequency.

Current−mode operation: the controller uses current ̆mode control architecture.

700 V – _ Power MOSFET: Due to **onsemi** Very High Voltage Integrated Circuit technology, the circuit hosts a high ̆voltage power MOSFET featuring a 34 or 12 Ω $R_{DS(on)}$ – T_J = 25 C. This value lets the designer build a power supply up to 7.8 W operated on universal mains. An internal current source delivers the startup current, necessary to crank the power supply.

Dynamic Self−Supply: Due to the internal high voltage current source, this device could be used in the application without the auxiliary winding to provide supply voltage.

Short circuit protection: by permanently monitoring the COMP line activity, the IC is able to detect the presence of a short ̆circuit, immediately reducing the output power for a total system protection. A t_{SCP} timer is started as soon as the COMP current is below threshold, $I_{COMPfault}$, which indicates the maximum peak current. If at the end of this timer the fault is still present, then the device enters a safe, auto ̆recovery burst mode, affected by a fixed timer recurrence, $t_{recovery}$. Once the short has disappeared, the controller resumes and goes be sWo

Fault Condition – Short−circuit on V_{CC}

In some fault situations, a short ĭ circuit can purposely occur between V_{CC} and GND. In high line conditions (V_{HV} = 370 V_{DC}) the current delivered by the startup device will seriously increase the junction temperature. For instance, since I_{start1} equals 4 mA (the min corresponds to the highest T_j), the device would dissipate 370 · 4 m 1.48 W. To avoid this situation, the controller includes a novel circuitry made of two startup levels, I_{start1} and I_{start2}. At power

Auto−recovery Over Voltage Protection

The particular NCP1067X arrangement offers a simple way to prevent output voltage runaway when the optocoupler fails. As Figure 36 shows, a comparator monitors the V_{CC} pin. If the auxiliary pushes too much voltage into the C_{VCC} capacitor, then the controller considers an OVP situation and stops the internal drivers. When an OVP occurs, all switching pulses are permanently disabled. After $t_{recovery}$ delay, it resumes the internal drivers. If the failure symptom still exists, e.g. feedback opto

Soft−start

The NCP1067X features a 4 ms soft−start which reduces the power−on stress but also contributes to lower the output overshoot. Figure 38 shows a typical operating waveform. The NCP1067X features a novel patented structure which offers a better soft−start ramp, almost ignoring the start−up pedestal inherent to traditional current−mode supplies:

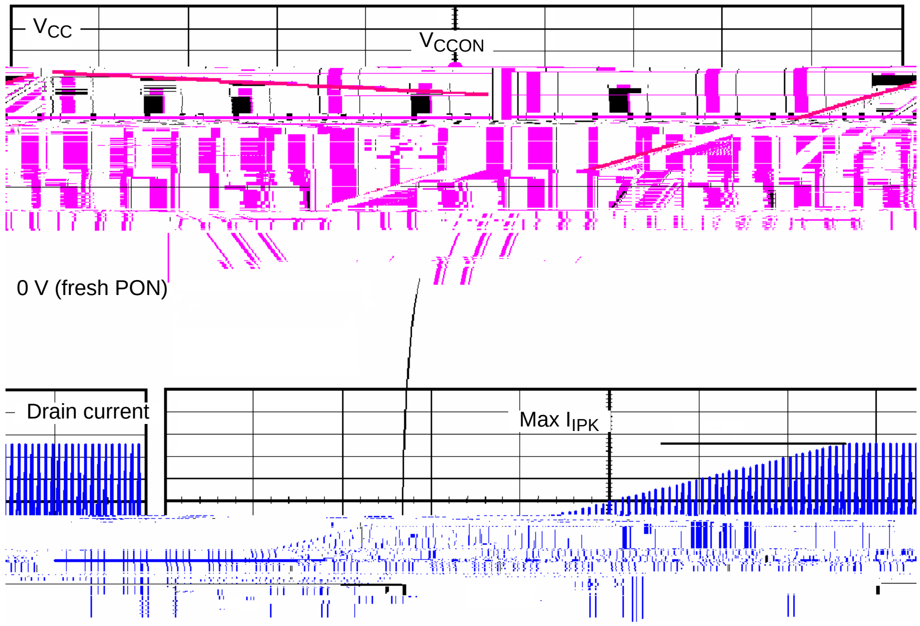


Figure 38. The 4 ms Soft−start Sequence

Ipk Reduction

The internal peak current set−point is following the COMP current information until its level reaches I_{Freeze}. Below this value, the peak current setpoint is frozen to 30% of the $I_{IPK(0)}$. This value is reached at a COMP current level of $I_{COMPskip}$ (120 μA typically). Below this point, if the output power continues to decrease, the part enters skip cycle for the best performance in no−load conditions. Figure 40 depict the adopted scheme for the part.

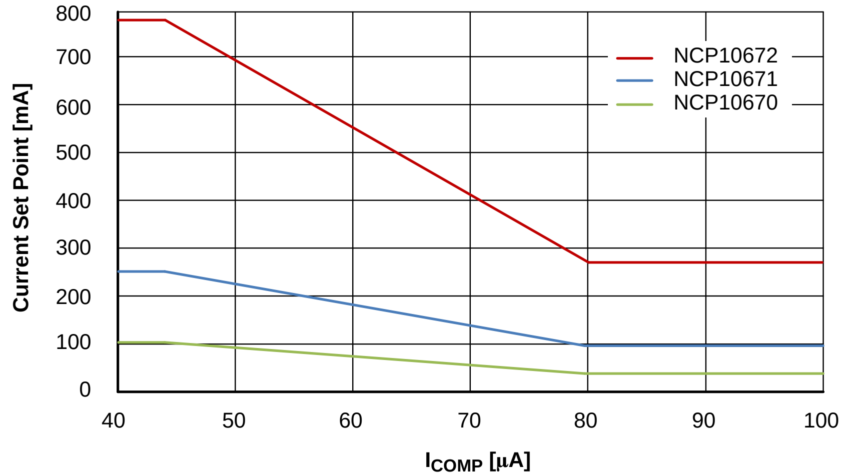


Figure 40. I_{IPK} Set−point is Frozen at Lower Power Demand

Feedback and Skip

Figure 41 depicts the relationship between COMP pin voltage and current. The COMP pin operates linearly as the absolute value of COMP current (I_{COMP}) is above 40 μA. In this linear operating range, the dynamic resistance is 17.7 kΩ typically ($R_{COMP(up)}$)

Figure 42 depicts the skip mode block diagram. When the COMP current information reaches $I_{COMPskip}$, the internal clock to set the flip−flop is blanked and the internal consumption of the controller is decreased. The hysteresis of internal skip comparator is minimized to lower the ripple of the auxiliary voltage for V_{CC} pin and V_{OUT}

FB pin function

The FB pin is used in non isolated SMPS application only. Portion of the output voltage is connected into the pin. The voltage is compared with internal V_{REF} (3.3 V) using

3. Lateral MOSFETs have a poorly doped bodyĭdiode which naturally limits their ability to sustain the avalanche. A traditional RCD clamping network shall thus be installed to protect the MOSFET. In some low power applications, a simple capacitor can also be used since

$$V_{drain,max} = V_{in} + N\,(V_{out} + V_f) + I_{peak}\sqrt{\frac{L_f}{C_{tot}}} \quad \text{(eq. 5)}$$

where L_f is the leakage inductance, C_{tot} the total capacitance at the drain node (which is increased by the capacitor you will wire between drain and source), N the N_P:N_S turn ratio, V_{out} the output voltage, V_f the secondary diode forward drop and finally, I_{peak} the maximum peak current. Worse case occurs when the SMPS is very close to regulation, e.g. the V_{out} target is almost reached and I_{peak} is still pushed to the maximum. For this design, we have selected our maximum voltage around 650 V (at V_{in} = 375 Vdc). This voltage is given by the *RCD* clamp installed from the drain to the bulk voltage. We will see how to calculate it later on.

4. Calculate the maximum operating dutyĭcycle for this flyback converter operated in CCM:

$$d_{max} = \frac{N\,(V_{out} + V_f)}{N\,(V_{out} + V_f) + V}$$

MOSFET Protection

As in any Flyback design, it is important to limit the drain excursion to a safe value, e.g. below the MOSFET BVdss which is 700 V. Figure 47 *a−b−c* present possible implementations:

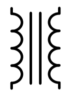
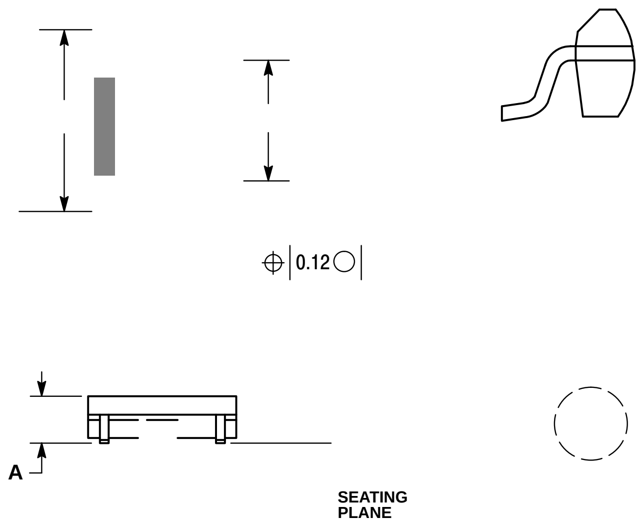


Figure 47. Different Options to Clamp the Leakage Spike

SOIC8 MISSING PIN 3
CASE 751EV
ISSUE O

SCALE 1:1

DATE 19 SEP 2017



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.10mm IN EXCESS OF MAXIMUM MATERIAL CONDITION.
4. DIMENSIONS D & E1 DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15mm PER SIDE. DIMENSIONS D AND E1 ARE DETERMINED AT DATUM F.
5. DATUMS A AND B ARE TO BE DETERMINED AT DATUM F.
6. A1 IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.

	MILLIMETERS	
DIM	**MIN**	**MAX**
A	1.35	1.75
A1	0.10	0.25
b	0.33	0.51
D	4.80	5.00
e	1.27 BSC	