



# NCN8026A

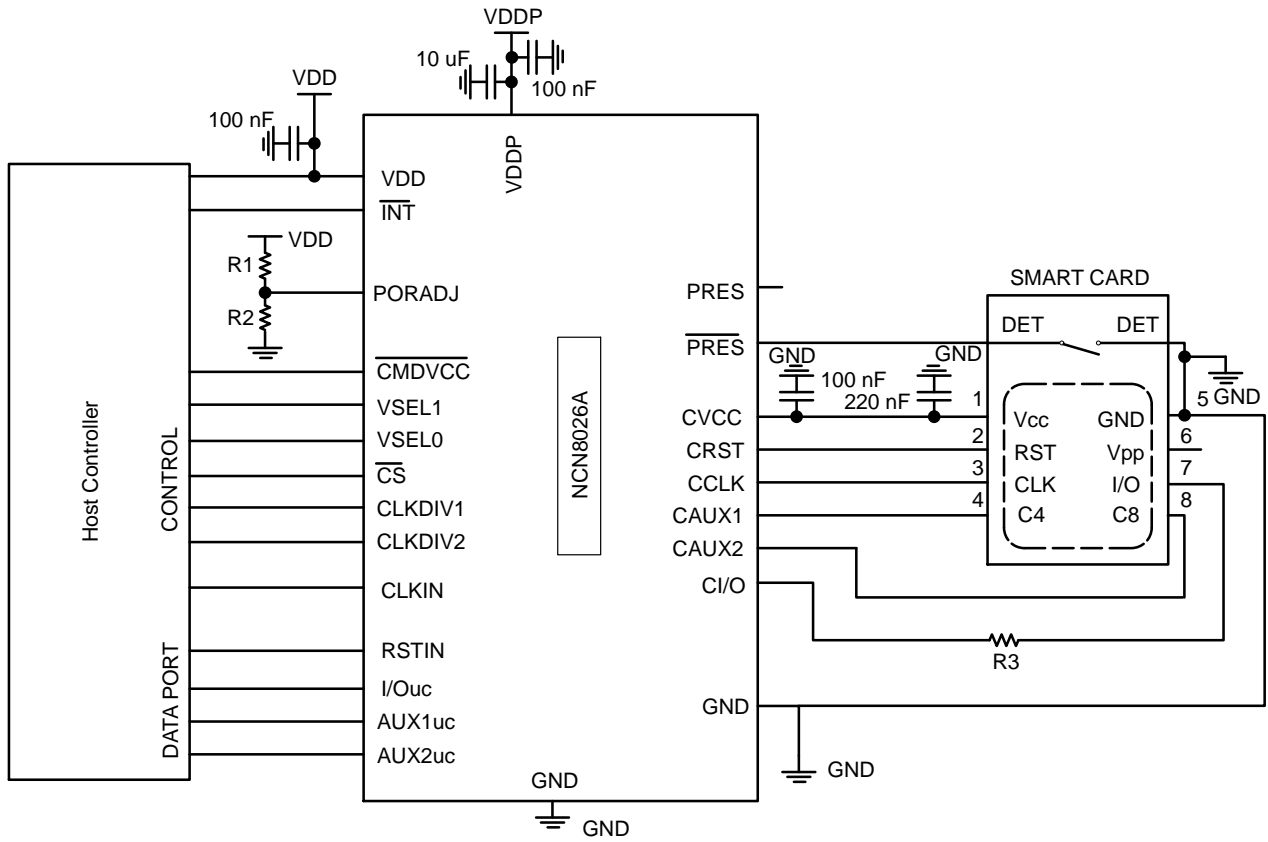


Figure 1. Typical Smart Card Interface Application

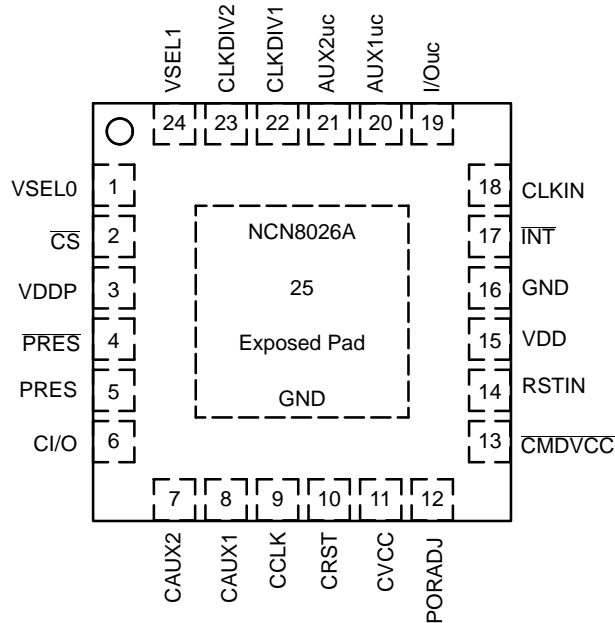


Figure 2. NCN8026A - QFN-24 Pinout (Top View)

# NCN8026A

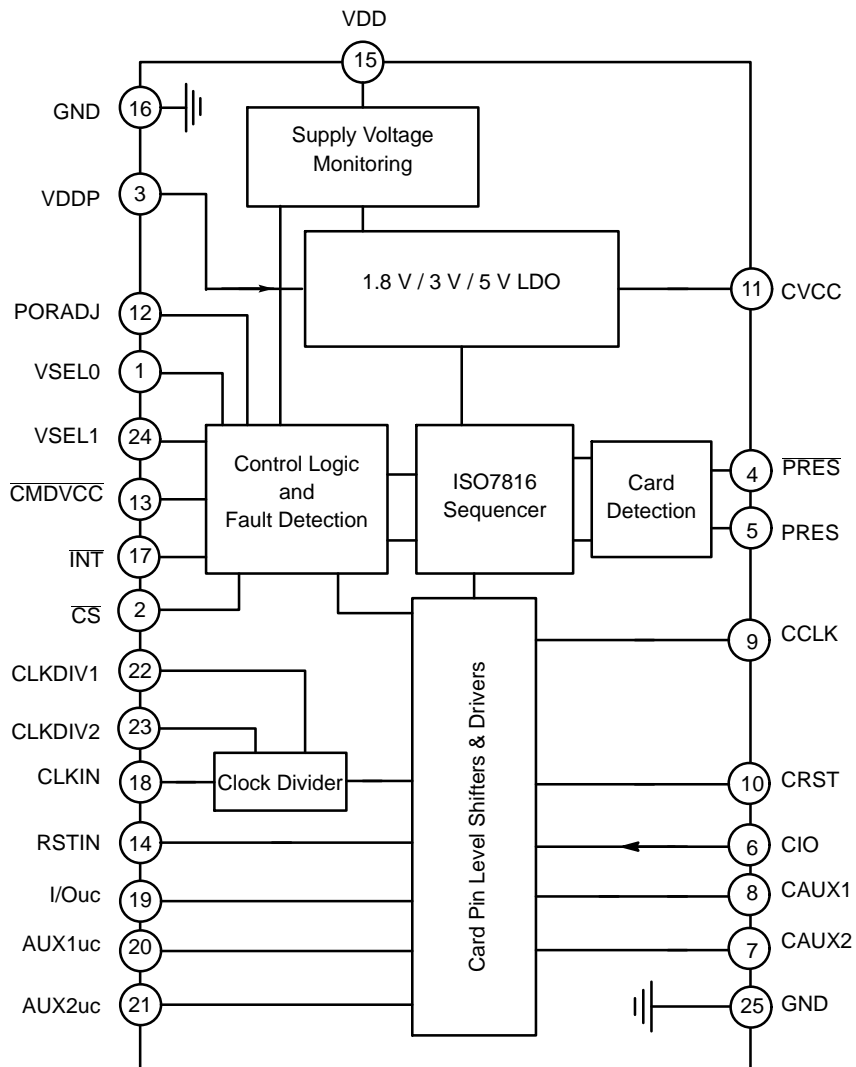


Figure 3. NCN8026A Block Diagram (QFN-24 Pin Numbering)

# NCN8026A

## PIN FUNCTION AND DESCRIPTION

Pin (QFN24)	Name	Type	Description
6	CI/O	Input/Output	This pin handles the connection to the serial I/O (C7) of the card connector. A bi-directional level translator adapts the serial I/O signal between the card and the micro controller. A 11 k $\Omega$ (typical) pull up resistor to CVCC provides a High impedance state for the smart card I/O link.
7	CAUX2	Input/Output	This pin handles the connection to the chip card's serial auxiliary AUX2 I/O pin (C8). A bi-directional level translator adapts the serial I/O signal between the card and the micro controller. A 11 k $\Omega$ (typical) pull up resistor to CVCC provides a High impedance state for the smart card C8 pin.
8	CAUX1	Input/Output	This pin handles the connection to the chip card's serial auxiliary AUX1 I/O pin (C4). A bi-directional level translator adapts the serial I/O signal between the card and the micro controller. A 11 k $\Omega$ (typical) pull up resistor to CVCC provides a High impedance state for the smart card C4 pin.
9	CCLK	Output	This pin is connected to the CLOCK card connector's pin (Chip card's pin C3). The Clock signal comes from the CLKIN input through clock dividers and level shifter.
10	CRST	Output	This pin is connected to the chip card's RESET pin (C2) through the card connector. A level translator adapts the external Reset (RSTIN) signal to the smart card.
11	CVCC	Power Output	This pin is connected to the smart card power supply pin (C1). An internal low dropout regulator is programmable using the pins VSEL0 and VSEL1 to supply either 5 V or 3 V or 1.8 V output voltage. An external distributed ceramic capacitor ranging from 80 nF to 1.2 $\mu$ F recommended must be connected across CVCC and CGND. This set of capacitor (if distributed) must be low ESR (< 100 m $\Omega$ ).
12	PORADJ	Input	Power-on reset threshold adjustment input pin for changing the reset threshold ( $V_{DD}$ UVLO threshold) thanks to an external resistor power divider. Needs to be connected to ground when unused.
13	CMDVCC	Input	Command $V_{CC}$ pin. Activation sequence Enable/Disable pin (active Low). The activation sequence is enabled by toggling $\overline{\text{CMDVCC}}$ High to Low and when a card is present. When $\overline{\text{CMDVCC}}$ = High, the CVCC output is pulled low and the internal LDO is disabled unless the device has been latched by the CS pin.
14	RSTIN	Input	This Reset input connected to the host and referred to VDD (microcontroller side), is connected to the



# NCN8026A

**POWER SUPPLY SECTION** ( $V_{DD} = 3.3\text{ V}$ ;  $V_{DDP} = 5\text{ V}$ ;  $T_{amb} = 25\text{ C}$ ;  $F_{CLKIN} = 5\text{ MHz}$ )

Symbol	Rating	Min
--------	--------	-----

HOST INTERFACE SECTION

# NCN8026A

**SMART CARD INTERFACE SECTION** CI/O, CAUX1, CAUX2, CCLK, CRST, PRES,  $\overline{\text{PRES}}$  ( $V_{DD} = 3.3 \text{ V}$ ;  $V_{DDP} = 5 \text{ V}$ ;  $T_{\text{amb}} = 25$ )



# NCN8026A

**SMART CARD INTERFACE SECTION** CI/O, CAUX1, CAUX2, CCLK, CRST, PRES,  $\overline{\text{PRES}}$  ( $V_{DD} = 3.3\text{ V}$ ;  $V_{DDP} = 5\text{ V}$ ;  $T_{\text{amb}} = 25\text{ C}$ ;  
 $F_{\text{CLKIN}} = 5\text{ MHz}$ )

Symbol	Rating	Min	Typ	Max	Unit
--------	--------	-----	-----	-----	------

|IH|



Finally the Reset level shifter is enabled (typically 2  $\mu$ s after clock channel) (t4)

The clock can also be applied to the card using a **RSTIN mode** allowing controlling the clock starting by setting RSTIN Low (Figure 4). Before running the activation sequence, that is before setting Low  $\overline{\text{CMDVCC}}$  RSTIN is set High. The following sequence is applied:

The Smart Card Interface is enable by setting  $\overline{\text{CMDVCC}}$  LOW (RSTIN is High).

Between t2 (Figure 4) and t5 = 240  $\mu$ s, RSTIN is reset to LOW and CCLK will start precisely at this moment allowing a precise count of clock cycles before toggling CRST Low to High for ATR (Answer To Reset) request.

CRST remains LOW until 240  $\mu$ s; after t5 = 240  $\mu$ s CRST is enabled and is the copy of RSTIN which has no more control on the clock.

If controlling the clock with RSTIN is not necessary (**Normal Mode**), then  $\overline{\text{CMDVCC}}$  can be set LOW with RSTIN LOW. In that case, CLK will start minimum 2  $\mu$ s after the transition on I/O (Figure 5), and to obtain an ATR, CRST can be set High by RSTIN also about 2  $\mu$ s after the clock channel activation ( $T_{\text{act}}$ ).

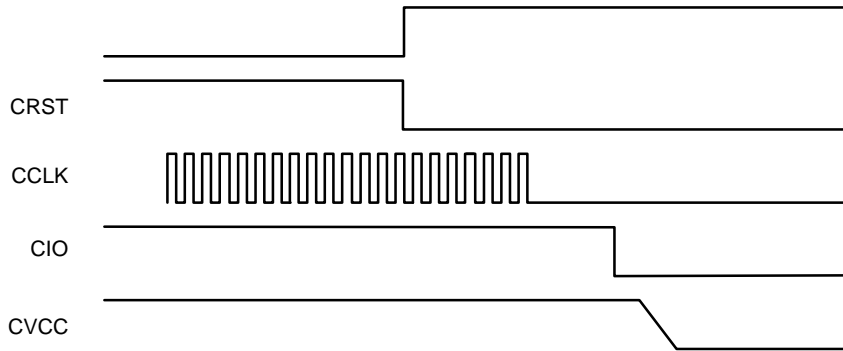
The internal activation sequence activates the different channels according to a specific hardware built in sequencing internally defined but at the end the actual activation

# NCN8026A

## SMART CARD POWER-DOWN

When the communication session is completed the NCN8026A runs a deactivation sequence by setting High  $\overline{\text{CMDVCC}}$ . The below power down sequence is executed:

CRST is forced to Low  
CCLK is set Low 12  $\mu\text{s}$  after CRST.  
CI/O, CAUX1 and CAUX2 are pulled Low  
Finally CVCC supply can be shut off.





# NCN8026A

## APPLICATION SCHEMATIC

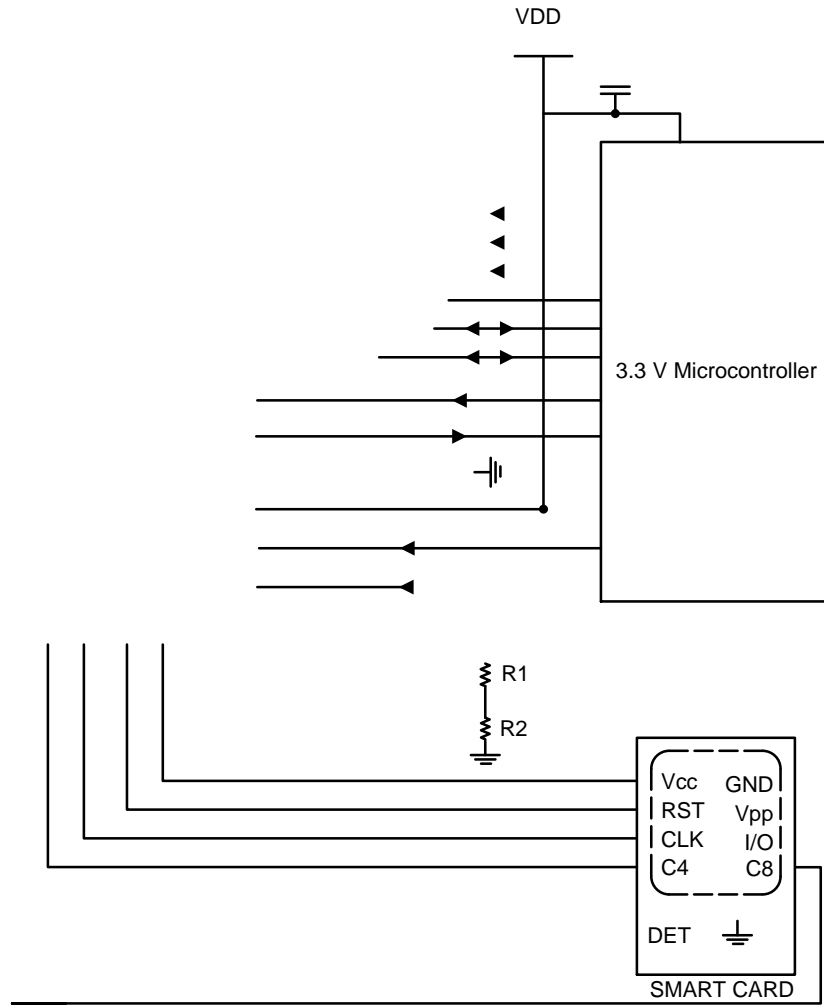
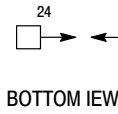
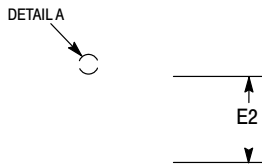
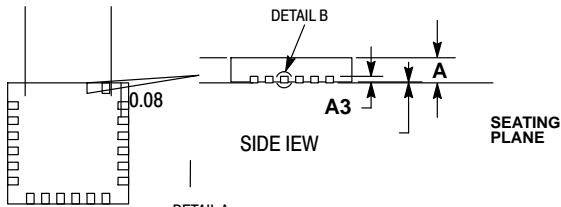
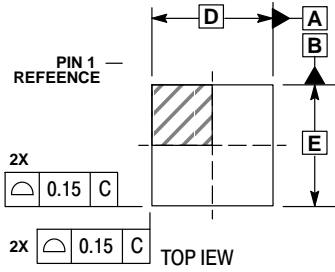


Figure 8. Application Schematic

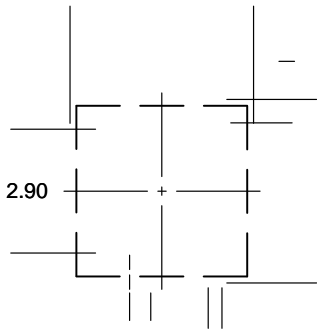
**QFN24, 4x4, 0.5P**  
**CASE 485L**  
**ISSUE B**

DATE 05 JUN 2012

f2.836  
 0.41 cm 0 0  
**SCALE 2:1**



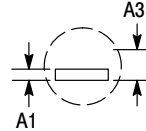
**SOLDERING FOOTPRINT**



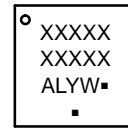
DIMENSIONS: MILLIMETERS

**NOTES:**

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 MM FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.



**GENERIC MARKING DIAGRAM\***



- XXXXX = Specific Device Code
- A = Assembly Location
- L = Wafer Lot
- Y = Year
- W = Work Week
- = Pb-Free Package

(Note: Microdot may be in either location)

**onsemi**, **onsemi**, and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi**'s product/patent coverage may be accessed at [www.onsemi.com/site/pdf/Patent-Marking.pdf](http://www.onsemi.com/site/pdf/Patent-Marking.pdf). **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as-is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi**

---

---