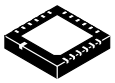
/

The NCN8025 / NCN8025A is a compact and cost−effective single smart card interface IC. It is dedicated for 1.8 V / 3.0 V / 5.0 V smart card reader/writer applications. The card $V_{CC}$ supply is provided by a built−in very low drop out and low noise LDO.

The device is fully compatible with the ISO 7816−3, EMV 4.3, UICC and related standards including NDS and other STB standards (Nagravision, Irdeto...). It satisfies the requirements specifying conditional access into Set−Top−Boxes (STB) or Conditional Access Modules (CAM and CAS).

This smart card interface IC is available in a QFN−24 package (NCN8025A) providing all of the industry−standard features usually required for STB smart card interface. It is also offered in a very compact package profile, QFN−16 (NCN8025), satisfying the requirements of cost−efficiency and space−saving requested by CAM and SIM applications.

For details regarding device implementation refer to application note AND8003/D, available upon request (please contact your local **onsemi** sales office or representative).



A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

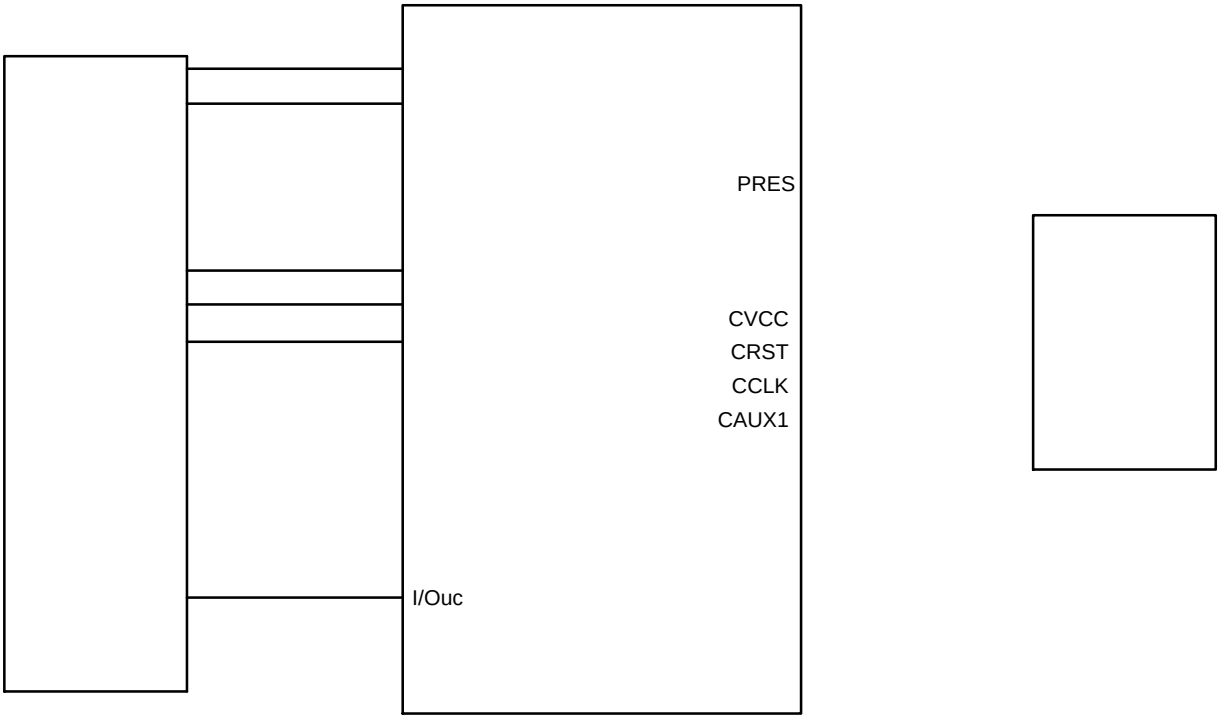
See detailed ordering and shipping information on page 13 of this data sheet.

- Single IC Card Interface
- Fully Compatible with ISO 7816−3, EMV 4.3, UICC and Related Standards Including NDS and Other STB Standards (Nagravision, Irdeto...)
- 3 Bidirectional Buffered I/O Level Shifters (C4, C7 and C8) (QFN−24) − 1 Bidirectional I/O Level Shifter for the QFN−16 compact version
- 1.8 V, 3.0 V or 5.0 V ± 5 % Regulated Card Power Supply Generation such as ICC ≤ 70 mA
- Regulator Power Supply: $V_{DDP}$ = 2.7 V to 5.5 V (@ 1.8 V),
  3.0 V to 5.5 V (@ 3.0 V) & 4.85 V to 5.5 V (@ 5.0 V)
- Independent Power Supply range on Controller Interface such as $V_{DD}$ = 2.7 V to 5.5 V
- Handles Class A, B and C Smart Cards
- Short Circuit Protection on all Card Pins
- Support up to 27 MHz input Clock with Internal Division Ratio 1/1, 1/2, 1/4 and 1/8 through CLKDIV1 and CLKDIV2
- ESD Protection on Card Pins up to +8 kV (Human Body Model)
- Activation / Deactivation Sequences (ISO7816 Sequencer)
- Fault Protection Mechanisms Enabling Automatic Device Deactivation in Case of Overload, Overheating, Card Take−off or Power Supply Drop−out (OCP, OTP, UVP)
- Interrupt Signal $\overline{INT}$ for Card Presence and Faults
- External Under−Voltage Lockout Threshold Adjustment on VDD (PORADJ Pin) (Except QFN−16)
- Available in 2 Package Formats: QFN−24 (NCN8025A) and QFN−16 (NCN8025)
- These are Pb−Free Devices

- Pay TV, Set Top Box Decoder with Conditional Access and Pay−per−View
- Conditional Access Module (CAM / CAS)
- SIM card interface applications (UICC / USIM)
- Point Of Sales and Transaction Terminals
- Electronic Payment and Identification



Publication Order Number:


PRES
CVCC
CRST
CCLK
CAUX1
I/Ouc

| | | | | |
|---|---|---|---|---|
| 6 | – | CAUX2 | | |

| | |
|---|---|
| ESD protection<br>Human Body Model (HBM) (Note 1)<br>Card Pins (card interface pins 3−11)<br>All Other Pins<br>Machine Model (MM)<br>Card Pins (card interface pins 3−11)<br>All Other Pins | <br><br>8 kV<br>2 kV<br><br>400 V<br>150 V |
| Moisture sensitivity (Note 2) QFN−24 and QFN−16 | Level 1 |
| Flammability Rating Oxygen Index: 28 to 34 | UL 94 V−0 @ 0.125 in |
| Meets or exceeds JEDEC Spec EIA/JESD78 IC Latch−up Test | |

1. Human Body Model (HBM), R = 1500 Ω, C = 100 pF.
2. For additional information, see Application Note AND8003/D.

(Note 3)

| | | | |
|---|---|---|---|
| Regulator Power Supply Voltage | $V_{DDP}$ | −0.3 $V_{DDP}$ 5.5 | V |
| Power Supply from Microcontroller Side | $V_{DD}$ | −0.3 $V_{DD}$ 5.5 | V |
| External Card Power Supply | CVCC | −0.3 CVCC 5.5 | V |
| Digital Input Pins | $V_{in}$ | −0.3 $V_{in}$ $V_{DD}$ | V |
| Digital Output Pins (I/Ouc, AUX1uc, AUX2uc, $\overline{INT}$) | $V_{out}$ | −0.3 $V_{out}$ $V_{DD}$ | V |
| Smart card Output Pins | $V_{out}$ | −0.3 $V_{out}$ CVCC | V |
| Thermal Resistance Junction−to−Air (Note 4) QFN−24<br>QFN−16 | $R_{\theta JA}$ | 37<br>48 | C/W |
| Operating Ambient Temperature Range | $T_A$ | −40 to +85 | C |
| Operating Junction Temperature Range | $T_J$ | −40 to +125 | |

CLKIN, RSTIN, I/Ouc, AUX1uc, AUX2uc, CLKDIV1, CLKDIV2, $\overline{CMDVCC}$, VSEL0, VSEL1 ($V_{DD}$ = 3.3 V; $V_{DDP}$ = 5 V; $T_{amb}$ = 25 C; $F_{CLKIN}$ = 10 MHz)

| | | | | | |
|---|---|---|---|---|---|
| $F_{CLKIN}$ | Clock frequency on pin CLKIN (Note 7) | − | − | 27 | MHz |
| $V_{IL}$ | Input Voltage level Low: CLKIN, RSTIN, CLKDIV1, CLKDIV2, $\overline{CMDVCC}$, VSEL0, VSEL1 | −0.3 | − | 0.3 x $V_{DD}$ | V |
| $V_{IH}$ | Input Voltage level High: CLKIN, RSTIN, CLKDIV1, CLKDIV2, $\overline{CMDVCC}$, VSEL0, VSEL1 | 0.7 x $V_{DD}$ | − | $V_{DD}$ + 0.3 | V |
| $\|I_{IL}\|$ | CLKDIV1, CLKDIV2, $\overline{CMDVCC}$, RSTIN, CLKIN, VSEL0, VSEL1 Low Level Input Leakage Current, $V_{IL}$ = 0 V | − | − | 1 | μA |
| $\|I_{IH}\|$ | CLKDIV1, CLKDIV2, $\overline{CMDVCC}$, RSTIN, CLKIN, VSEL0, VSEL1 Low Level Input Leakage Current, $V_{IH}$ = $V_{DD}$ | − | − | 1 | μA |
| $V_{IL}$ | Input Voltage level Low: I/Ouc, AUX1uc, AUX2uc | −0.3 | | 0.5 | V |
| $V_{IH}$ | Input Voltage level High: I/Ouc, AUX1uc, AUX2uc | 0.7 x $V_{DD}$ | | $V_{DD}$ + 0.3 | V |
| $\|I_{IL}\|$ | I/Ouc, AUX1uc, AUX2uc Low level input leakage current, $V_{IL}$ = 0 V | − | − | 600 | μA |
| $\|I_{IH}\|$ | I/Ouc, AUX1uc, AUX2uc High level input leakage current, $V_{IH}$ = $V_{DD}$ | − | − | 10 | μA |
| $V_{OH}$ | I/Ouc, AUX1uc, AUX2uc data channels, @ Cs ≤ 30 pF<br>High Level Output Voltage (CRD_I/O = CAUX1 = CAUX2 = CVCC)<br>$I_{OH}$ = −40 μA for $V_{DD}$ > 2 V ($I_{OH}$ = −20 μA for $V_{DD}$ ≤ 2 V) | 0.75 x $V_{DD}$ | − | $V_{DD}$ + 0.1 | V |
| $V_{OL}$ | Low Level Output Voltage (CRD_I/O = CAUX1 = CAUX2 = 0 V)<br>$I_{OL}$= + 1 mA | 0 | − | 0.3 | V |
| $t_{Ri/Fi}$ | Input Rising/Falling times (Note 7) | − | − | 1.2 | μs |
| $t_{Ro/Fo}$ | Output Rising/Falling times (Note 7) | − | − | 0.1 | μs |
| $R_{pu}$ | I/0uc, AUX1uc, AUX2uc Pull Up Resistor | 8 | 11 | 16 | kΩ |
| $V_{OH}$ | Output High Voltage<br>$\overline{INT}$ @ $I_{OH}$ = −15 μA (source) | 0.75 x $V_{DD}$ | − | − | V |
| $V_{OL}$ | Output Low Voltage<br>$\overline{INT}$ @ $I_{OL}$ = 2 mA (sink) | 0 | − | 0.30 | V |
| *$R_{INT}$* | *$\overline{INT}$ Pull Up Resistor (open−drain output configuration option) (Note 8)* | *40* | *50* | *60* | *kΩ* |

7. Guaranteed by design and characterization.
8. Option available under request (metal change). The current option is an inverter−like output.

CI/O, CAUX1, CAUX2, CCLK, CRST, PRES, $\overline{PRES}$ ($V_{DD}$ = 3.3 V; $V_{DDP}$ = 5 V; $T_{amb}$ = 25 C; $F_{CLKIN}$ = 10 MHz)

| | | | | | |
|---|---|---|---|---|---|
| | CRST @ CVCC = 1.8 V, 3.0 V, 5.0 V | | | | |
| $V_{OH}$ | Output RESET $V_{OH}$ @ $I_{rst}$ = −200 μA | 0.9 x CVCC | − | CVCC | V |
| $V_{OL}$ | Output RESET $V_{OL}$ @ $I_{rst}$ = 200 μA | 0 | − | 0.20 | V |
| $t_R$ | Output RESET Rise time @ $C_{out}$ = 100 pF (Note 9) | − | − | 100 | ns |
| $t_F$ | Output RESET Fall time @ $C_{out}$ = 100 pF (Note 9) | − | − | 100 | ns |
| $t_{R/F}$ | Output Rise/Fall times @ CVCC = 1.8 V & $C_{out}$ = 100 pF (Note 9) | − | − | 200 | ns |
| td | RSTIN to CRST delay − Reset enabled (Note 9) | − | − | 2 | μs |
| | CCLK @ CVCC = 1.8 V, 3.0 V or 5.0 V | | | | |
| $F_{CRDCLK}$ | Output Frequency (Note 9) | − | − | 27 | MHz |
| $V_{OH}$ | Output CCLK $V_{OH}$ @ $I_{clk}$ = −200 μA | 0.9 x CVCC | − | CVCC | V |
| $V_{OL}$ | Output CCLK $V_{OL}$ @ $I_{clk}$ = 200 μA | 0 | − | +0.2 | V |
| $F_{DC}$ | Output Duty Cycle (Note 9) | 45 | − | 55 | % |
| | Rise & Fall time | | | | |
| $t_{rills}$ | Output CCLK Rise time @ $C_{out}$ = 33 pF (Note 9) | − | − | 16 | ns |
| $t_{ulsa}$ | Output CCLK Fall time @ $C_{out}$ = 33 pF (Note 9) | − | − | 16 | ns |
| SR | Slew Rate @ $C_{out}$ = 33 pF (CVCC = 3.0 V or 5.0 V) (Note 9) | 0.2 | − | − | V/ns |
| | CAUX1, CAUX2, CI/O @ CVCC = 1.8 V, 3.0 V, 5.0 V | | | | |
| $V_{IH}$ | Input Voltage High Level | | | | |
| | 1.8 V Mode | 1.0 | − | CVCC + 0.3 | V |
| | 3.0 V Mode | 1.6 | − | CVCC + 0.3 | V |
| | 5.0 V Mode | 2.3 | − | CVCC + 0.3 | V |
| $V_{IL}$ | Input Voltage Low Level | | | | |
| | 1.8 V mode | −0.30 | − | 0.50 | V |
| | 3.0 V mode | −0.30 | − | 0.80 | V |
| | 5.0 V mode | −0.30 | − | 1.00 | V |
| $\|I_{IL}\|$ | Low Level Input current $V_{IL}$ = 0 V | − | | 600 | μA |
| $\|I_{IH}\|$ | High Level Input current $V_{IH}$ = CVCC | − | | 10 | μA |
| $V_{OH}$ | Output $V_{OH}$ | | | | |
| | @ $I_{OH}$ = −40 μA for CVCC = 3.0 V and 5.0 V | 0.8 x CVCC | − | CVCC + 0.1 | V |
| | @ $I_{OH}$ = −20 μA for CVCC = 1.8 V | 0.8 x CVCC | − | CVCC + 0.1 | V |
| $V_{OL}$ | Output $V_{OL}$ | | | | |
| | @ $I_{OL}$ = 1 mA, $V_{IL}$ = 0 V for CVCC = 1.8 V | 0 | − | 0.27 | V |
| | @ $I_{OL}$ = 1 mA, $V_{IL}$ = 0 V for CVCC = 3.0 V and 5.0 V | 0 | − | 0.30 | V |
| $t_{Ri\ /\ Fi}$ | Input Rising/Falling times (Note 9) | − | − | 1.2 | μs |
| $t_{Ro\ /\ Fo}$ | Output Rising/Falling times / $C_{out}$ = 80 pF (Note 9) | − | − | 0.1 | μs |
| $F_{bidi}$ | Maximum data rate through bidirectional I/O, AUX1 & AUX2 channels (Note 9) | − | − | 1 | MHz |
| $R_{PU}$ | CAUX1, CAUX2, CI/O Pull− Up Resistor | 8 | 11 | 16 | kΩ |
| $t_{IO}$ | Propagation delay IOuc −> CI/O and CI/O − | | | | |

can be interesting to adjust this threshold at a higher value and by the way increase the $V_{DD}$ supply dropout detection level which enables a deactivation sequence if the $V_{DD}$ voltage is too low.

For example, there are microcontrollers for which the minimum supply voltage insuring a correct operating is higher than 2.6 V; increasing $UVLO_{VDD}$ ($V_{DD}$ falling) is consequently necessary. Considering for instance a resistor bridge with R1 = 56 kΩ, R2 = 42 kΩ and $V_{POR–}$ = 1.27 V typical the $V_{DD}$ dropout detection level can be increased up to:

$$UVLO = \frac{56k + 42k}{42k} V_{POR-} = 2.96\ V \qquad \text{(eq. 2)}$$

The input clock can be divided by 1/1, 1/2, 1/4, or 1/8, depending upon the specific application, prior to be applied to the smart card driver. These division ratios are programmed using pins CLKDIV1 and CLKDIV2 (see Table 2). The input clock is provided externally to pin CLKIN.

| | | |
|---|---|---|
| 0 | 0 | CLKIN / 8 |
| 0 | 1 | CKLKIN / 4 |
| 1 | 0 | CLKIN |
| 1 | 1 | CLKIN / 2 |

The clock input stage (CLKIN) can handle a 27 MHz maximum frequency signal. Of course, the ratio must be defined by the user to cope with Smart Card considered in a given application

In order to avoid any duty cycle out of the 45% / 55% range specification, the divider is synchronized by the last flip flop, thus yielding a constant 50% duty cycle, whatever be the divider ratio 1/2, 1/4 or 1/8. On the other hand, the output signal Duty Cycle cannot be guaranteed 50% if the division ratio is 1 and if the input Duty Cycle signal is not within the 46% ï 56% range at the CLKIN input.

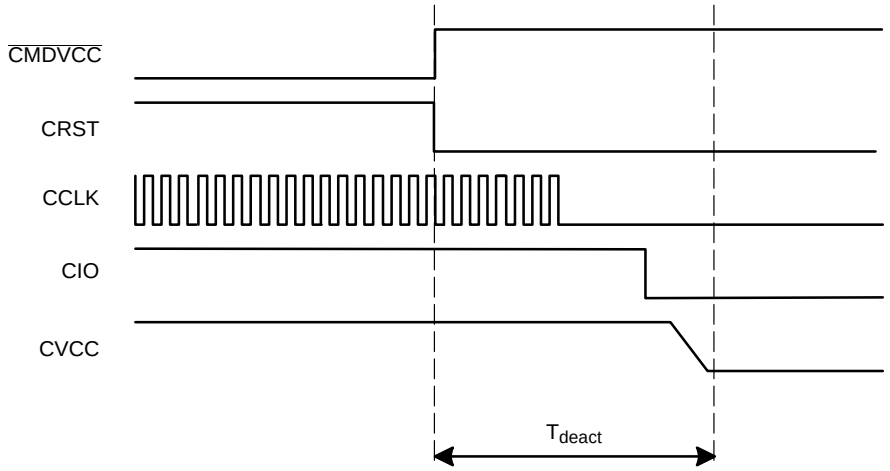
When the signal applied to CLKIN is coming from the external controller, the clock will be applied to the card under the control of the microcontroller or similar device after the activation sequence has been completed.

The three bidirectional level shifters I/O, AUX1 and AUX2 adapt the voltage difference that might exist between the microïcontroller and the smart card. These three channels are identical. The first side of the bidirectional level

–

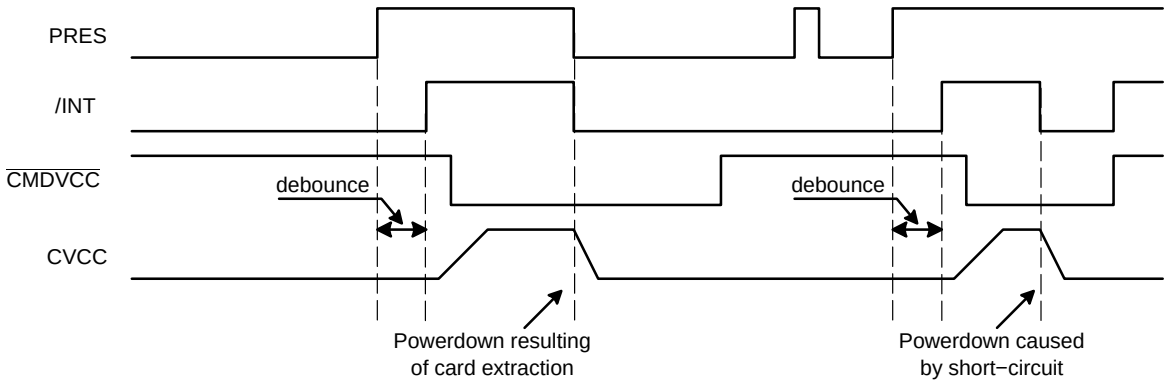
When the communication session is completed the NCN8025 / NCN8025A runs a deactivation sequence by setting High $\overline{\text{CMDVCC}}$. The below power down sequence is executed:

- CRST is forced to Low
- CCLK is set Low 12 μs after CRST.
- CI/O, CAUX1 and CAUX2 are pulled Low
- Finally CVCC supply can be shut off.




In order to protect both the interface and the external smart card, the NCN8025 / NCN8025A provides security features to prevent failures or damages as depicted here after.

- Card extraction detection
- $V_{DD}$ under voltage detection
- Short circuit or overload on CVCC
- DC/DC operation: the internal circuit continuously senses the CVCC voltage (in the case of either over or under voltage situation).
- DC/DC operation: under voltage detection on $V_{DDP}$
- Overheating
- Card pin current limitation: in the case of a short circuit to ground. No feedback is provided to the external MPU.

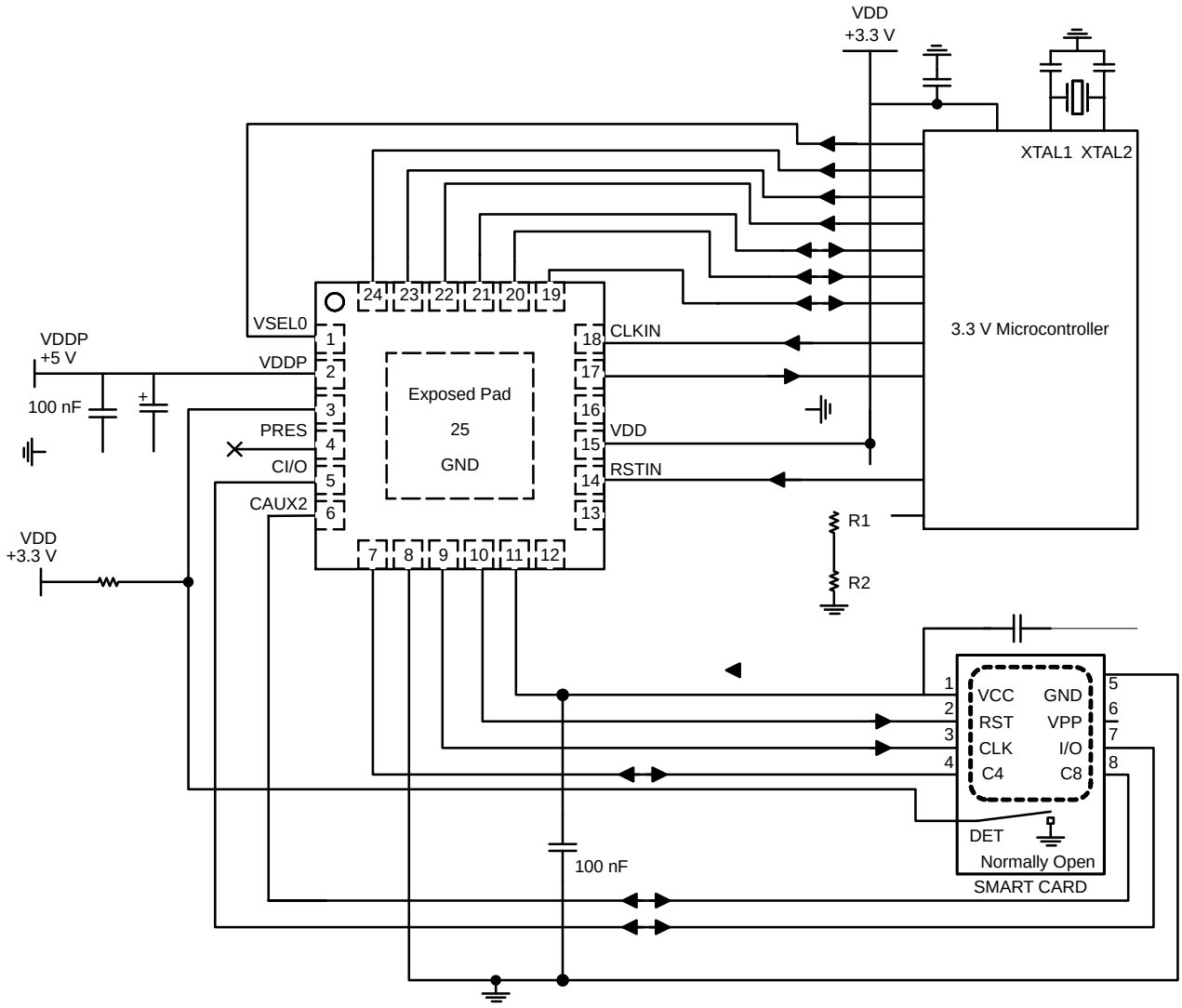



A card session is opened by toggling $\overline{\text{CMDVCC}}$ High to Low.

Before a card session, $\overline{\text{CMDVCC}}$ is supposed to be in a High position. $\overline{\text{INT}}$ is Low if no card is present in the card connector (Normally open or normally closed type). $\overline{\text{INT}}$ is High if a card is present. If a card is inserted ($\overline{\text{INT}}$ = Highv N1oc Tm 20T

As illustrated by Figure 8 the device has a debounce timer of 8 ms typical duration. When a card is inserted, output $\overline{\text{INT}}$ goes High only at the end of the debounce time. When the card is removed a deactivation sequence is automatically and immediately performed and $\overline{\text{INT}}$ goes Low.

The NCN8025 / NCN8025A includes devices to protect the pins against the ESD spike voltages. To cope with the different ESD voltages developed across these pins, the built in structures have been designed to handle either 2 kV, when related to the micro controller side, or 8 kV when connected with the external contacts (HBM model). Practically, the CRST, CCLK, CI/O, CAUX1, CAUX2, PRES and $\overline{\text{PRES}}$ pins can sustain 8 kV. The CVCC pin has the same ESD protection and can source up to 70 mA continuously, the absolute maximum current being internally limited with a max at 150 mA. The CVCC current limit depends on $V_{DDP}$ and CVCC.

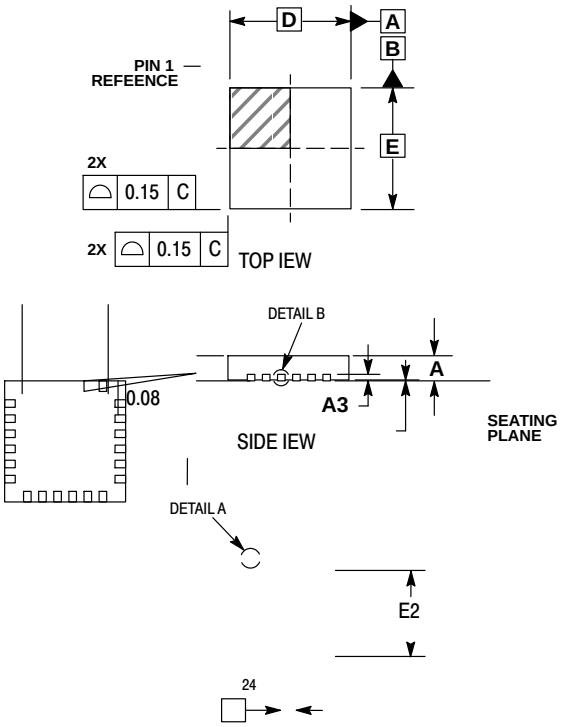


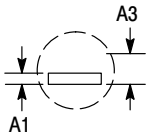
**QFN24, 4x4, 0.5P**
CASE 485L
ISSUE B

DATE 05 JUN 2012

f2.8246041 cm 0 0

**SCALE 2:1**



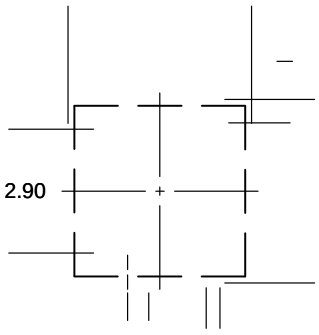

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 MM FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

**GENERIC**
**MARKING DIAGRAM***


XXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

SOLDERING FOOTPRINT

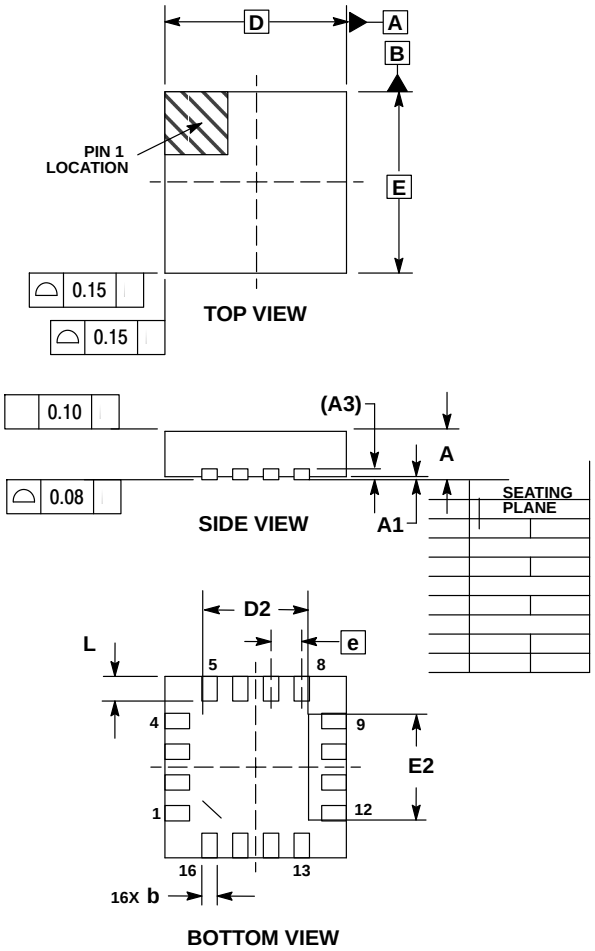



DIMENSIONS: MILLIMETERS

**QFN16 3*3*0.75 MM, 0.5 P**
CASE 488AK−01
ISSUE O

DATE 13 SEP 2004

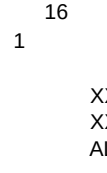
**SCALE 2:1**




NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 MM FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
5. $L_{max}$ CONDITION CAN NOT VIOLATE 0.2 MM SPACING BETWEEN LEAD TIP AND FLAG.

| | | |
|---|---|---|
| **A1** | 0.00 | 0.05 |
| **A3** | 0.20 REF | |
| **b** | 0.18 | 0.30 |

**GENERIC**
**MARKING DIAGRAM***




XXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G”, may or not be present.