nse

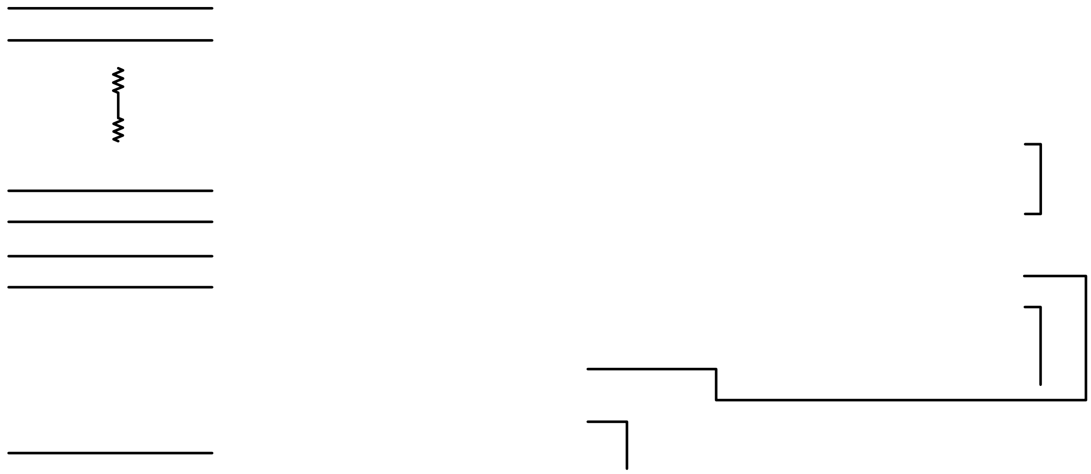
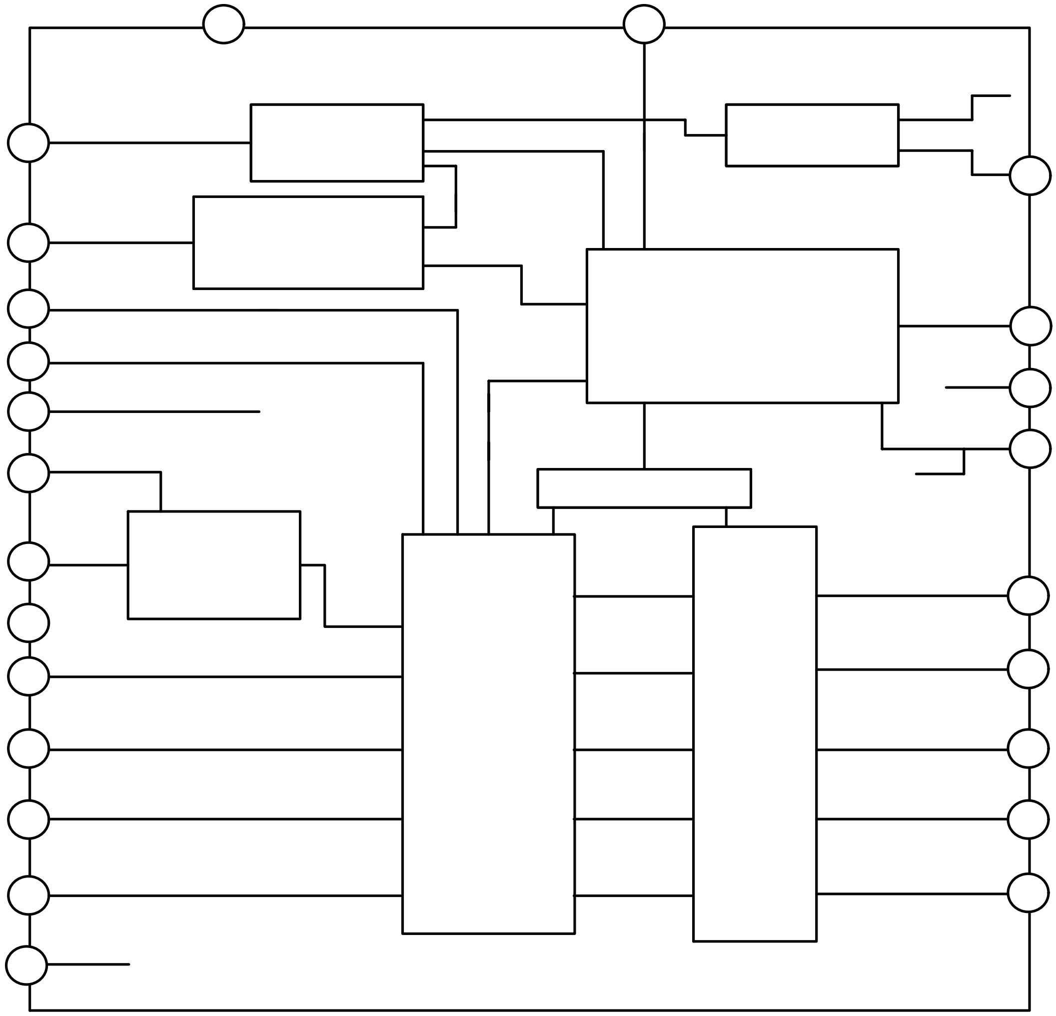


Figure 1. Typical Smart Card Interface Application



PIN FUNCTION AND DESCRIPTION

Pin #	Description

ATTRIBUTES

Characteristics	Values
ESD protection Human Body Model (HBM) (Note 1) Card Pins (Card Interface Pins 9 − 17) All Other Pins Machine Model (MM) Card Pins (Card Interface Pins 9 − 17) All Other Pins	 8 kV 2 kV 400 V 150 V
Moisture sensitivity (Note 2) SOIC−28 and TSSOP−28	Level 3
Flammability Rating Oxygen Index: 28 to 34	UL 94 V−0 @ 0.125 in
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latch−up Test	

1. Human Body Model (HBM), R = 1500 Ω, C = 100 pF.
2. For additional information, see Application Note AND8003/D.

MAXIMUM RATINGS (Note 3)

Rating	Symbol	Value	Unit
DC/DC Converter Power Supply Voltage	V_{DDP}	$-0.3 \le V_{DDP} \le 5.5$	V
Power Supply from Microcontroller Side	V_{DD}	$-0.3 \le V_{DD} \le 5.5$	V

EĿ(u.58900 V)5(Tj5758 0t4 1 Tf1.3.ac.0949V)TjET525.525.203 503.66 27194.589 T659ss m-.jET525.203 501018 Tc(D27.4772 Tm-.0021 TcyD27.4772 wA

0.3

POWER SUPPLY SECTION (V_{DD} = 3.3 V; V_{DDP} = 5 V; T_{amb} = 25 C; F_{CLKIN} = 10 MHz)

Symbol	Rating	Min	Typ	Max	Unit
V_{DDP}	DC/DC Converter Power Supply, CRD_V_{CC} = 5 V $\lvert I_{CC} \rvert \leq$				

HOST INTERFACE SECTION CLKIN, RSTIN, I/Ouc, AUX1uc, AUX2uc, CLKDIV1, CLKDIV2, $\overline{\text{CMDVCC}}$, 5V/$\overline{\text{3V}}$
(V_{DD} = 3.3 V; V_{DDP} = 5 V; T_{amb} = 25 C; F_{CLKIN} = 10 MHz)

Symbol	Rating	Min	Typ	Max	Unit
F_{CLKIN}	Clock Frequency on Pin CLKIN (with Divider Ratio ≥ 2) (Note 6)	−	−	27	MHz
V_{IL}	Input Voltage Level Low: CLKIN, RSTIN, I/Ouc, AUX1uc, AUX2uc, CLKDIV1, CLKDIV2, $\overline{\text{CMDVCC}}$, 5V/$\overline{\text{3V}}$	−0.3	−	0.3 x V_{DD}	V
V_{IH}	Input Voltage Level High: CLKIN, RSTIN, I/O, AUX1, AUX2, CLKDIV1, CLKDIV2, $\overline{\text{CMDVCC}}$, 5V/$\overline{\text{3V}}$	0.7 x V_{DD}	−	V_{DD} + 0.3	V
$\|I_{IL}\|$	CLKDIV1, CLKDIV2, $\overline{\text{CMDVCC}}$, RSTIN, CLKIN, 5V/3V Low Level Input Leakage Current, V_{IL} = 0 V	−	−	1.0	μA
$\|I_{IH}\|$	CLKDIV1, CLKDIV2, $\overline{\text{CMDVCC}}$, RSTIN, CLKIN, 5V/3V Low Level Input Leakage Current, V_{IH} = V_{DD}	−	−	1.0	μA
V_{IL}	Input Voltage Level Low: I/Ouc, AUX1uc, AUX2uc	−0.3	−	0.5	V
V_{IH}	Input Voltage Level High: I/Ouc, AUX1uc, AUX2uc	0.7 x V_{DD}	−	V_{DD} + 0.3	V
$\|I_{IL}\|$	I/Ouc, AUX1uc, AUX2uc Low Level Input Leakage Current, V_{IL} = 0 V	−	−	600	μA
$\|I_{IH}\|$	I/Ouc, AUX1uc, AUX2uc High Level Input Leakage Current, V_{IH} = V_{DD}	−	−	10	μA
V_{OH}	I/Ouc, AUX1uc, AUX2uc data channels, @ Cs ≤ 30 pF High Level Output Voltage (CRD_I/O = CRD_AUX1 = CRD_AUX2 = CRD_V_{CC}) I_{OH} = 0 I_{OH} = −40 μA for V_{DD}				
V_{OL}					
$t_{Ri/Fi}$					
$t_{Ro/Fo}$					

SMART CARD INTERFACE SECTION, CRD_IO, CRD_AUX1, CRD_AUX2, CRD_CLK, CRD_RST, CRD_PRES, $\overline{\text{CRD\_PRES}}$ (V_{DD} = 3.3 V; V_{DDP} = 5 V; T_{amb} = 25 C; F_{CLKIN} = 10 MHz)

Symbol	Rating	Min	Typ	Max	Unit
	CRD_RST @ CRD_V_{CC} = 3.0 V, 5.0 V				
V_{OH}	Output RESET V_{OH} @ I_{rst} = −200 μA	0.9 x CRD_V_{CC}	−	CRD_V_{CC}	V
V_{OL}	Output RESET V_{OL} @ I_{rst} = 200 μA	0	−	0.20	V
V_{OH}	Output RESET V_{OH} @ I_{rst} = −20 mA	0	−	0.4	V
V_{OL}	Output RESET V_{OL} @ I_{rst} = 20 mA	CRD_V_{CC} − 0.4	−	CRD_V_{CC}	V
t_R	Output RESET Risetime @ C_{out} = 100 pF (Note 7)	−	−	100	ns
t_F	Output RESET Falltime @C_{out} = 100 pF (Note 7)	−	−	100	ns
t_d	RSTIN to CRD_RST Delay − Reset Enabled (Note 7)	−	−	2	μs
	CRD_CLK @ CRD_V_{CC} = 3.0 V or 5.0 V				
F_{CRDCLK}	Output Frequency (Note 7)	−	−	18	MHz
V_{OH}	Output CRD_CLK V_{OH} @ I_{clk} = −200 μA	0.9 x CRD_V_{CC}	−	CRD_V_{CC}	V
V_{OL}	Output CRD_CLK V_{OL} @ I_{clk} = 200 μA	0	−	+0.2	V
V_{OH}	Output CRD_CLK V_{OH} @ I_{clk} = −70 mA	0	−	0.4	V
V_{OL}	Output CRD_CLK V_{OL} @ I_{clk} = 70 mA	CRD_V_{CC} −0.4	−	CRD_V_{CC}	V
F_{DC}	Output Duty Cycle (Note 7)	45	−	55	%
	Rise & Fall time (Note 5)				
t_{rills}	Output CRD_CLK Risetime @ C_{out} = 30 pF	−	−	16	ns
t_{ulsa}	Output CRD_CLK Falltime @ C_{out} = 30 pF	−	−	16	ns
SR	Slew Rate @ Cout = 33 pF (Note 7)	0.2	−	−	V/ns

SMART CARD INTERFACE SECTION, CRD_IO, CRD_AUX1, CRD_AUX2, CRD_CLK, CRD_RST, CRD_PRES, $\overline{\textbf{CRD\_PRES}}$ (V_{DD} = 3.3 V; V_{DDP} = 5 V; T_{amb} = 25 C; F_{CLKIN} = 10 MHz)

Symbol	Rating	Min	Typ	Max	Unit
	CRD_PRES, $\overline{\text{CRD\_PRES}}$				
$\lvert I_{IH} \rvert$	High level input leakage current, $V_{IH} = V_{DD}$				
	CRD_PRES		3		
	$\overline{\text{CRD\_PRES}}$				
$\lvert I_{IL} \rvert$	Low level input leakage current, V_{IL} = 0 V				
	CRD_PRES				
	$\overline{\text{CRD\_PRES}}$		3		

bridge with R1 = 56 kΩ, R2 = 42 kΩ and V_{POR-} = 1.20 V typical the V_{DD} dropout detection level can be increased up to:

$$UVLO = \frac{59k + 42k}{42k} V_{POR-} = 2.75\ V$$

The minimum dropout detection voltage should be higher than 2 V.

The maximum detection level may be up to VDD.

CLOCK DIVIDER:

The input clock can be divided by 1/1, 1/2, 1/4, or 1/8, depending upon the specific application, prior to be applied to the smart card driver. These division ratios are programmed using pins CLKDIV1 and CLKDIV2 (see Table 1). The input clock is provided externally to pin CLKIN.

Table 1. Clock Frequency Programming

CLKDIV1	CLKDIV2	F_{CRD_CLK}
0		

If controlling the clock with RSTIN is not necessary (**Normal Mode**), then /CMDVCC can be set LOW with RSTIN LOW. In that case, CLK will start minimum 500 ns after the transition on I/O (Figure 5), and to obtain an ATR, CRST can be set High by RSTIN also about 500 ns after the clock channel activation (tact).

The internal activation sequence activates the different channels according to a specific hardware builtĭit sequencing internally defined but at the end the actual activation sequencing is the responsibility of the application software and can be redefined by the microĭcontroller to comply with the different standards and the different ways the standards manage this activation (for example light differences exist between the EMV and the ISO7816 standards).

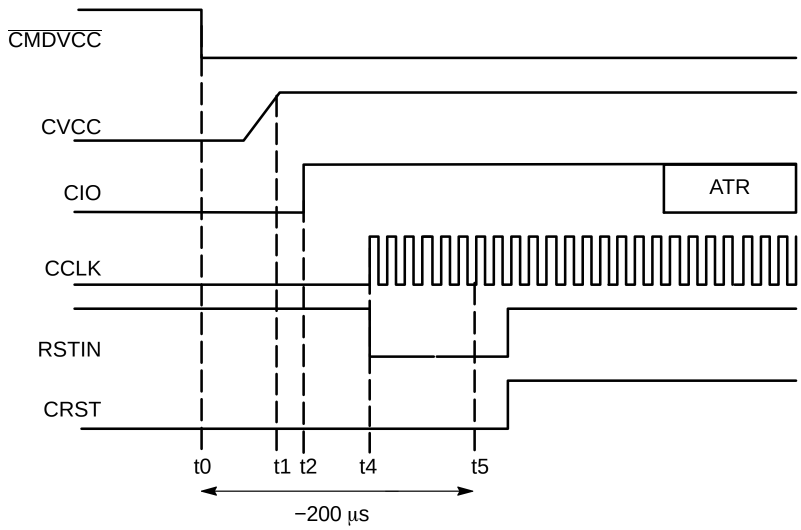


Figure 4. Activation Sequence − RSTIN mode (RSTIN Starting High)

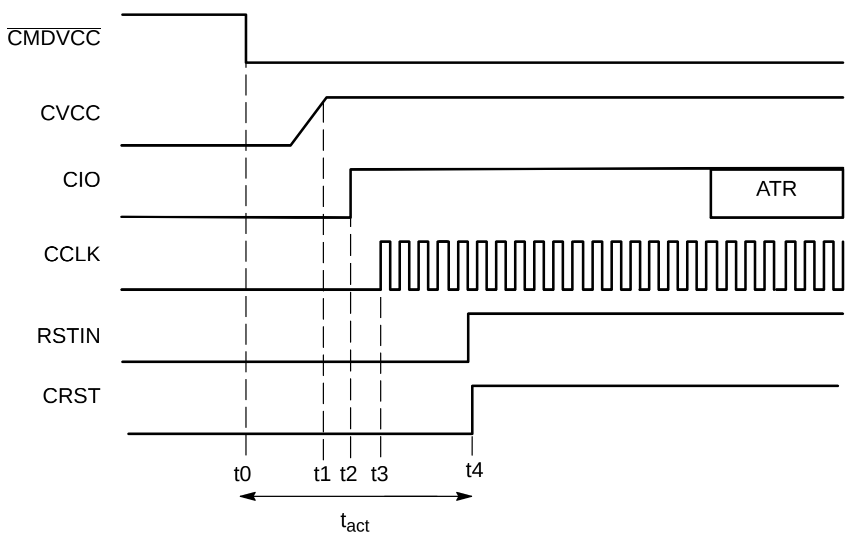


Figure 5. Activation Sequence − Normal Mode

POWER−DOWN

When the communication session is completed the NCN8024R runs a deactivation sequence by setting High $\overline{\text{CMDVCC}}$. The below power down sequence is executed:

CRD_RST is forced to Low

CRD_CLK is set Low 12 µs after CRD_RST.

CRD_IO, CRD_AUX1 and CRD_AUX2 are pulled Low

Finally CRD_V_{CC} supply can be shutĭoff.

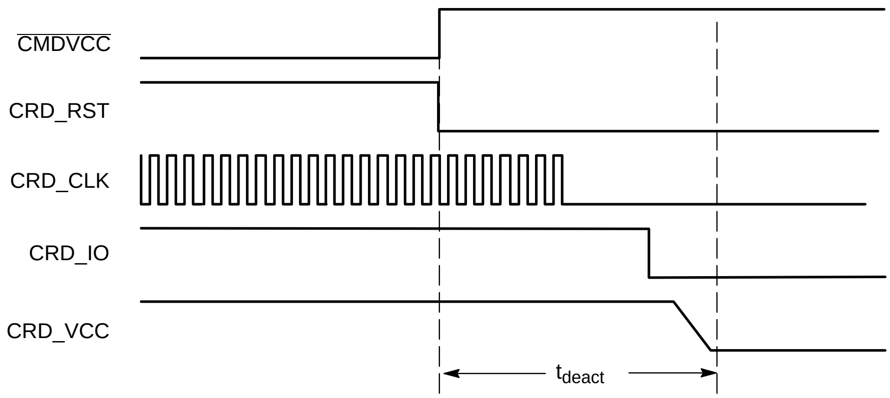


Figure 6. Deactivation Sequence

FAULT DETECTION

In order to protect both the interface and the external smart card, the NCN8024R provides security features to prevent failures or damages as depicted here after.

Card extraction detection

V_{DD} under voltage detection

Shortĭcircuit or overload on CRD_V_{CC}

Card pin current limitation: in the case of a short circuit to ground. No feedback is provided to the external MPU.

LDO operation: the internal circuit continuously senses the CRD_V_{CC} voltage (in the case of either over or under voltage situation).

LDO operation: underĭvoltage detection on V_{DDP} or overload on VUP

Overheating

Card pin current limitation: in the case of a short circuit to ground. No feedback is provided to the external MPU

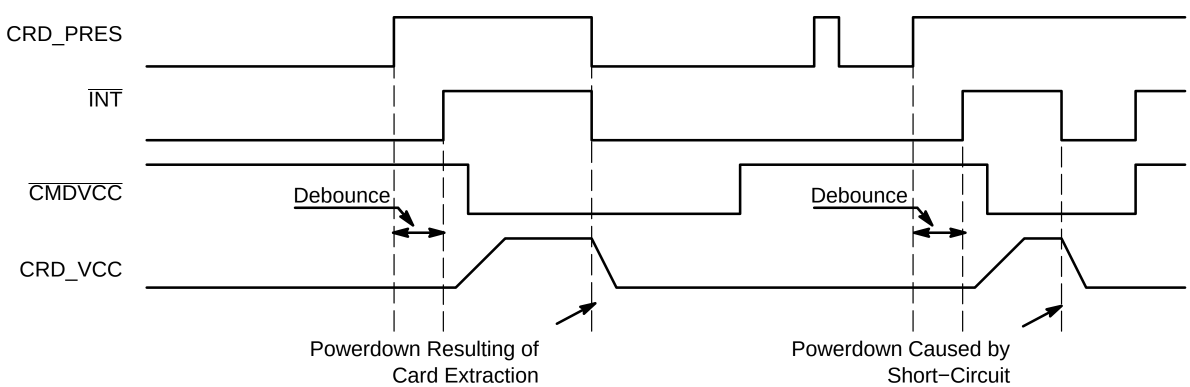


Figure 7. Fault Detection and Interrupt Management

Interrupt Pin Management:

A card session is opened by toggling $\overline{CMDVCC}$ High to Low.

Before a card session, $\overline{CMDVCC}$ is supposed to be in a High position. $\overline{INT}$ is Low if no card is present in the card connector (Normally open or normally closed type). $\overline{INT}$ is High if a card is present. If a card is inserted ($\overline{INT}$ = High) and if V_{DD} drops below the UVLO threshold then $\overline{INT}$ pin drops Low immediately. It turns back High when V_{DD} increases again over the UVLO limit (including hysteresis), a card being still present.

During a card session, $\overline{CMDVCC}$ is Low and $\overline{INT}$ pin goes Low when a fault is detected. In that case a deactivation is immediately and automatically performed (see Figure 6). When the microcontroller resets $\overline{CMDVCC}$ to High it can sense the $\overline{INT}$ level again after having got completed the deactivation.

As illustrated by Figure 7 the device has a debounce timer of 8 ms typical duration. When a card is inserted, output $\overline{INT}$ goes High only at the end of the debounce time. When the card is removed a deactivation sequence is automatically and immediately performed and $\overline{INT}$ goes Low.

ESD PROTECTION

The NCN8024R includes devices to protect the pins against the ESD spikes voltages. To cope with the different ESD voltages developed across these pins, the built in structures have been designed to handle either 2 kV, when related to the micro controller side, or 8 kV when connected with the external contacts (HBM model). Practically, the CRD_RST, CRD_CLK, CRD_IO, CRD_AUX1, CRD_AUX2, CRD_PRES and $\overline{\text{CRD\_PRES}}$ pins can sustain 8 kV. The CRD_VCC pin has the same ESD protection and can source up to 70 mA continuously, the absolute maximum current being internally limited with a max at 150 mA. The CRD_VCC current limit depends on V_{DDP} and CRD_VCC.

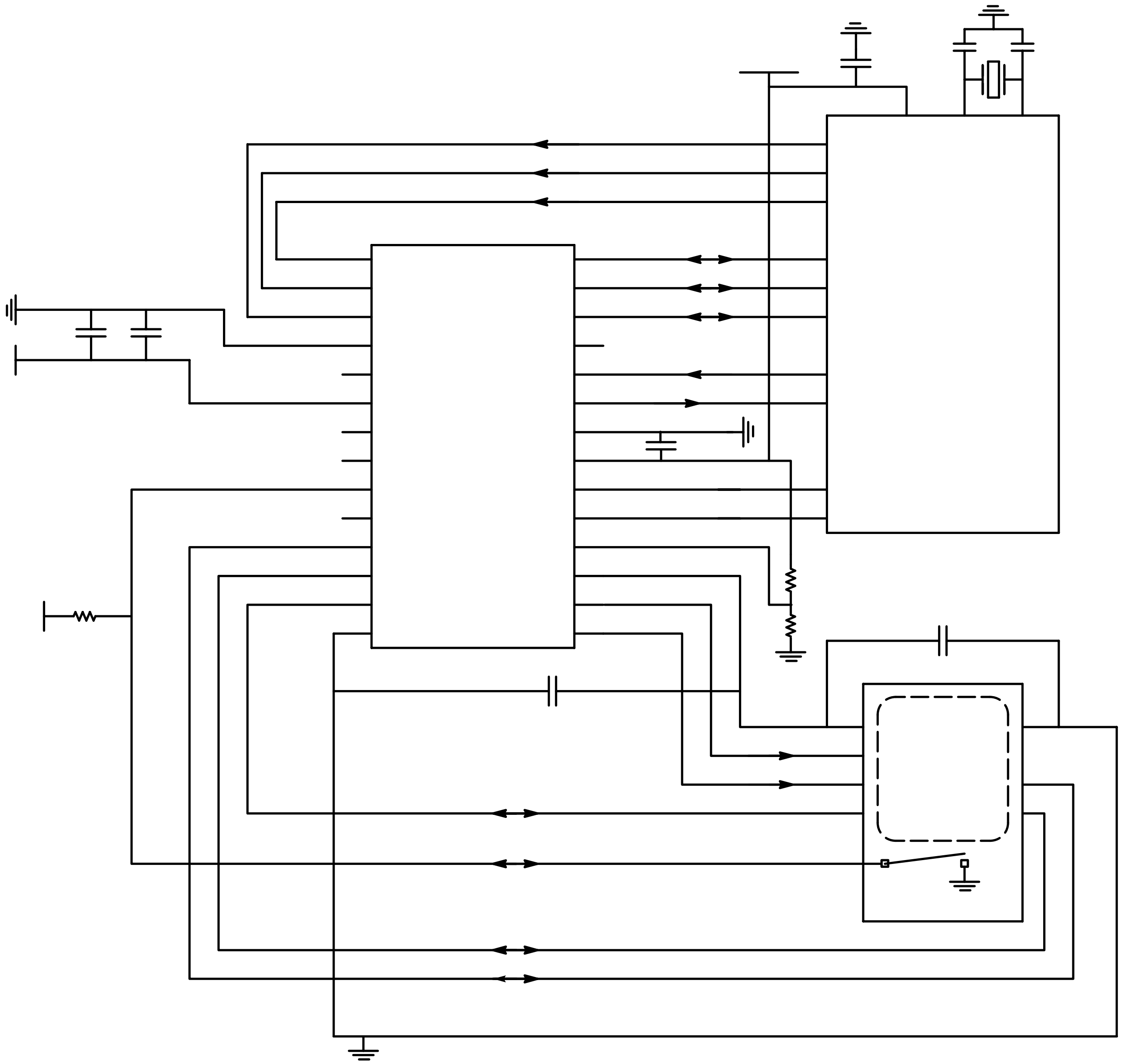
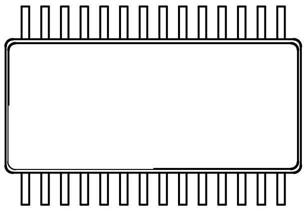


Figure 8. Application Schematic

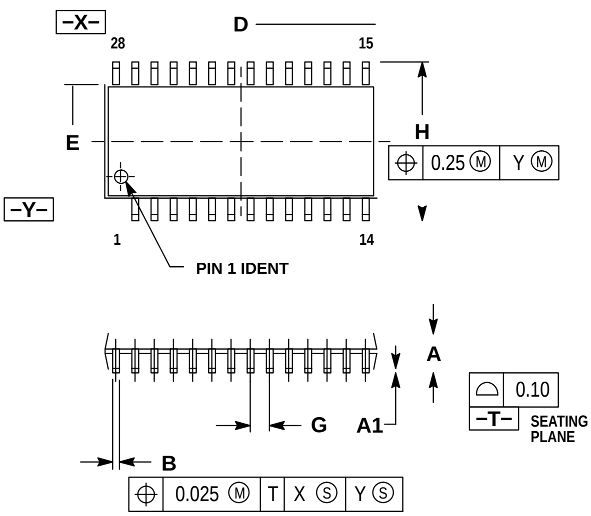
PACKAGE DIMENSIONS

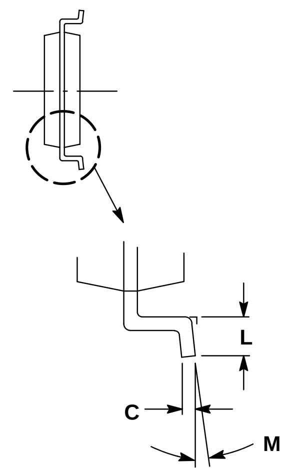
TSSOP28
CASE 948AA
ISSUE A



SOIC−28 WB
CASE 751F
ISSUE J

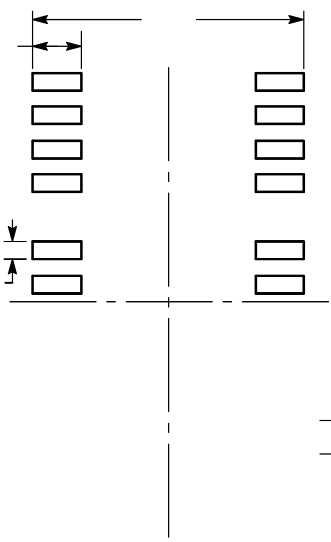
DATE 23 SEP 2015



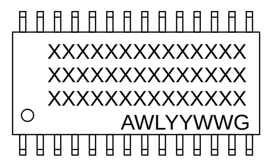


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBER PR5OTRUSION SHALL NOT BE 0.13 TOTATL IN EXCESS OF B DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS	
	MIN	MAX
A	2.35	2.65
A1	0.13	0.29
B	0.35	0.49
C	0.23	0.32
D	17.80	18.05
E	7.40	7.60
G	1.27 BSC	
H	10.05	10.55
L	0.41	0.90
M	0°	8°



GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”,