C 6004A

D A / I I
I C

The NCN6004A is an interface IC dedicated for Secured Access Module reader/writer applications. It allows the management of two external ISO/EMV cards thanks to a simple and flexible microcontroller interface. Several NCN6004A interfaces can share a single data bus, assuming the external MPU provides the right Chip Select signals to identify each IC connected on the bus. A built in accurate protection system guarantees timely and controlled shutdown in the case of external error conditions.

On top of that, the NCN6004A can independently handle the power

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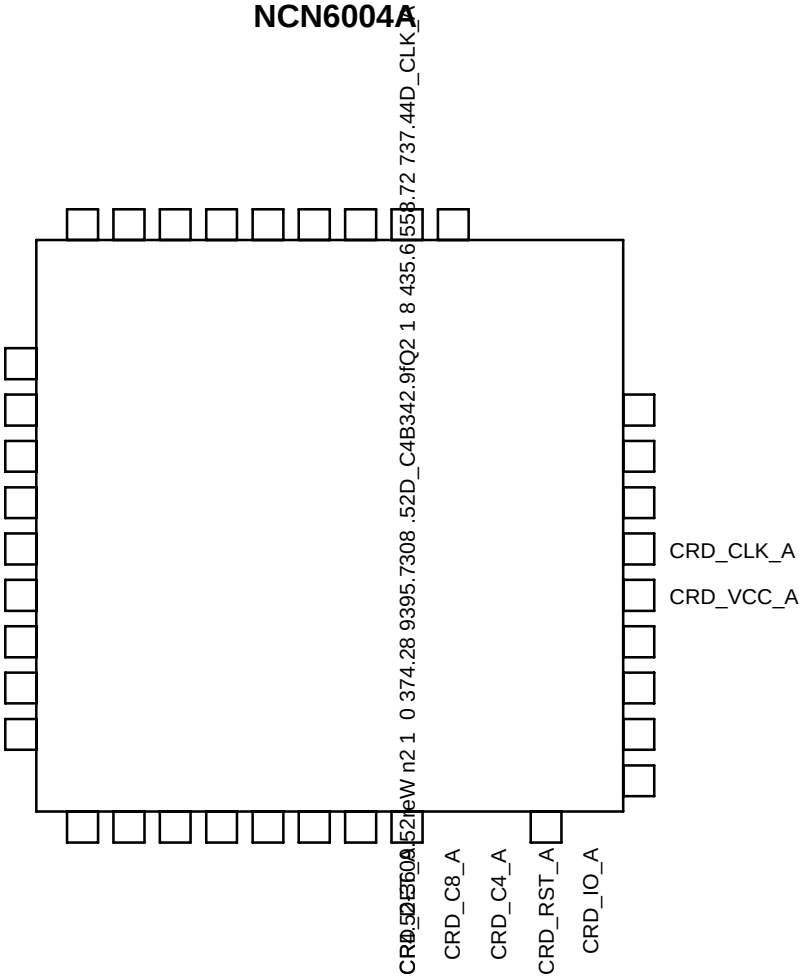
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CRD_VCC_A
CRD_C8_A
CRD_C4_A
CRD_RST_A
CRD_IO_A

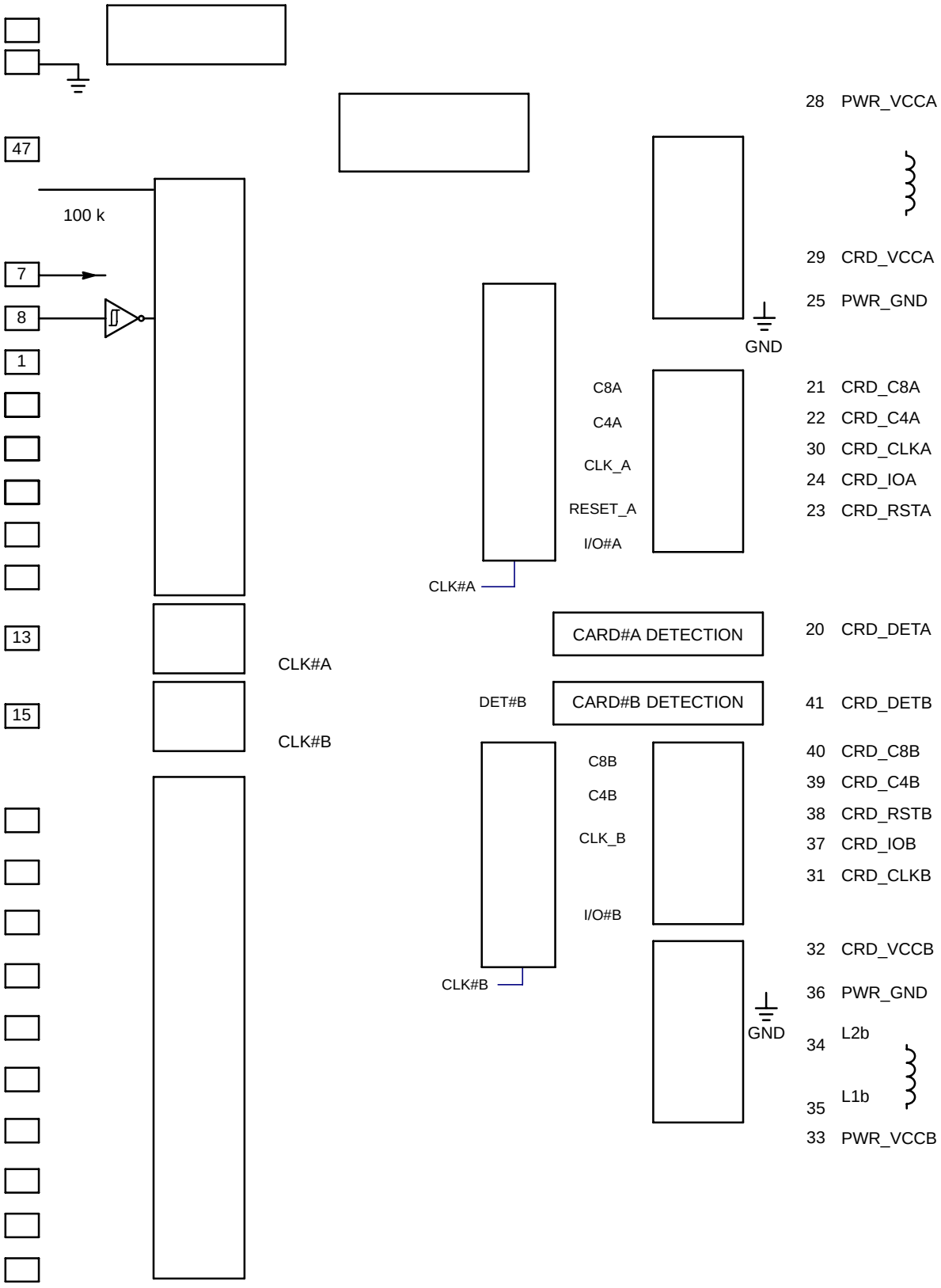


Figure 3. Block Diagram

PIN DESCRIPTION

Pin	Symbol	Type	Description
1	A0	INPUT	This pin is combined with $\overline{CS}$, A1, A2, A3, CARD_SEL and $\overline{PGM}$ to program the chip mode of operation, the CRD_VCC voltage value, and to read the data provided by the internal STATUS register (Table 1).
2	A1	INPUT	This pin is combined with $\overline{CS}$, A0, A2, A3, CARD_SEL and $\overline{PGM}$ to program the chip mode of operation, the CRD_VCC voltage value, and to read the data provided by the internal STATUS register (Table 1).
3	A2	INPUT	This pin is combined with $\overline{CS}$, A0, A1, A3, CARD_SEL and $\overline{PGM}$ to program the chip mode of operation, the CRD_VCC voltage value, and to read the data provided by the internal STATUS register (Table 1).
4	A3	INPUT	This pin is combined with $\overline{CS}$, A0, A1, A2, CARD_SEL and $\overline{PGM}$ to program the chip mode of operation, the CRD_VCC voltage value, and to read the data provided by the internal STATUS register (Table 1).

5	CARD_SEL	INPUT	This pin provides logic identification of the Card #A/Card #B external smart card. The logic signal is set up by the external microcontroller.
			CARD_SEL = High $\rightarrow$ selection of the Smart Card A connected to pins 20, 21, 22, 23, 24, 29 and 30 (respectively CRD_DET_A, CRD_C8_A, CRD_C4_A, CRD_RST_A, CRD_IO_A, CRD_VCC_A and CRD_CLK_A).
			CARD_SEL = Low $\rightarrow$ selection of the Smart Card B connected to pins 41, 39, 40, 31, 38, 37, and 32 (respectively CRD_DET_B, CRD_C4_B, CRD_C8_B, CRD_CLK_B, CRD_RST_B, CRD_IO_B, and CRD_VCC_B).

6	$\overline{PGM}$	DIGITAL INPUT	

PIN DESCRIPTION (continued)

Pin	Symbol	Type	Description
10	RESET_A	INPUT	The signal present on this pin is translated to the RST pin of the external smart card #A. The $\overline{CS}$ signal must be Low to validate the RESET function, regardless of the selected card. Assuming the μP provides two independent lines to control the RESET pins, the NCN6004A can control two cards simultaneously. When MUX_MODE = High, this pin provides an access to either card A or B Reset by means of CARD_SEL selection bit. The associated pull up resistor is either connected to V_{CC} (EN_RPU = H) or disconnected when EN_RPU = Low.
11	C4_A	INPUT	This pin controls the card #A C4 contact The signal can be either de−multiplexed, at MPU level, or is multiplexed with C4_B, depending upon the MUX_MODE logic state. When MUX_MODE = High, this pin provides an access to either card A or B C4 channel by means of CARD_SEL selection bit. The associated pull up resistor is either connected to V_{CC} (EN_RPU = H) or disconnected when EN_RPU = Low.
12	C8_A	INPUT	This pin controls the card #A C8 contact. The signal can be either de−multiplexed, at MPU level, or is multiplexed with C8_B, depending upon the MUX_MODE logic state. When MUX_MODE = High, this pin provides an access to either card A or B C8 channel by means of CARD_SEL selection bit. The associated pull up resistor is either connected to V_{CC} (EN_RPU = H) or disconnected when EN_RPU = Low.
13	CLOCK_IN_A	Clock Input, High Impedance	The signal present on this pin comes from either the MCU master clock, or from any signal fulfilling the logic level and frequency specifications. This signal is fed to the internal clock selection circuit prior to be connected to the external smart card #A. Each of the external card can have different division ratio, depending upon the state of the CRD_SEL pin and associated programming bits. The built−in circuit can be programmed to 1/1, 1/2, 1/4 or 1/8 frequency division ratio. This input is valid and routed to either CRD_CLK_A _DIVIDER or CRD_CLK_B_DIVIDER regardless of the MUX_MODE state, depending upon the CLK_D_A/CRD_D_B and CARD_SEL programmed states (Table 1). Although this input supports the signal coming from a crystal oscillator, care must be observed to avoid digital levels outside the specified V

PIN DESCRIPTION (continued)

Pin	Symbol	Type	Description

PIN DESCRIPTION (continued)

Pin	Symbol	Type	Description
39	CRD_C4_B	OUTPUT	This pin controls the card #B C4 contact, according to the ISO specification. A built−in level shifter is used to adapt the card and the MCU, regardless of the power supply voltage of each signals. The signal present at this pin is latched upon either CARD_SEL or $\overline{CS}$ or $\overline{PGM}$ positive going transient and resume to a transparent mode when card #B is selected. The pin is hardwired to zero, the bias being provided by the V_{CC} supply, when either the V_{CC} voltage drops below 2.7 V, or during the CRD_VCC_B startup time.
40	CRD_C8_B	OUTPUT	This pin controls the card #B C8 contact, according to the ISO specification. A built−in level shifter is used to adapt the card and the MCU, regardless of the power supply voltage of each signals. The signal present at this pin is latched upon either CARD_SEL or $\overline{CS}$ or $\overline{PGM}$ positive going transient and resume to a transparent mode when card #B is selected. The pin is hardwired to zero, the bias being provided by the V_{CC} supply, when either the V_{CC} voltage drops below 2.7 V, or during the CRD_VCC_B startup time.
41	CRD_DET_B	INPUT	This pin senses the signal coming from the external smart card connector to detect the presence of card #B. The polarity of the signal is programmable as Normally Open or Normally Close switch. The logic signal will be activated when the level is either Low or High, with respect to the polarity defined previously. By default, the input is Normally Open. A built−in circuit prevents uncontrolled short pulses to generate an INT signal. The digital filter eliminates pulse width below 50 μs.
42	ANLG_VCC	POWER	This pin is connected to the positive external power supply. The device sustains any voltage from +2.7 V to +5.5 V. This voltage supplies the NCN6004A internal Analog and Logic circuits. A high quality capacitor must be connected across this pin and ANLG_GND, 10 μF/6 V is recommended. A set of extra pins (28 and 33) are provided to connect the power supply to the internal DC/DC converter. Note: The voltage present at pin 28 and 33 must be equal to the voltage present at pin 42
43	ANLG_GND	GROUND	This pin is the ground reference for both analog and digital signals and must be connected to the system Ground. Care must be observed to provide a copper PCB layout designed to avoid small signals and power transients sharing the same track. Good high frequency techniques are strongly recommended.
44	MUX_MODE	INPUT	This pin selects the mode of operation of the card signals from the MPU side. When MUX_MODE = Low, all the card signals are fully de−multiplexed and data transfers can take place with both cards simultaneously. On top of that, both cards can be accessed during the programming sequence, assuming the external microcontroller is capable to run multi tasks software. When MUX_MODE = High, all the card signals are multiplexed and the communications with the cards shall take place in a sequential mode. The card is selected by setting CARD_SEL high or Low. The internal logic will disable the CARD_B inputs and use CARD_SEL inputs as a single channel to controls both output smart cards sequentially when MUX_MODE = H. Moreover, when MUX_MODE = High, all the B channel μP dedicated pins, except CLOCK_IN_B, pin 15, are forced to a high level by means of internal pull up resistors. It is not necessary to connect these pins (16, 17, 18 and 19) to an external bias voltage, but it is mandatory to avoid any connections to ground. On the other hand, in this case the

PIN DESCRIPTION (continued)

Pin	Symbol	Type	Description
47	$\overline{INT}$	OUTPUT	This pin is activated LOW when a card has been inserted and detected in either of the external ports. The signal is reset by either a positive going transition on pin $\overline{CS}$, or by a High level on pin PWR_ON combined with $\overline{CS}$ = Low. Similarly, an interrupt is generated when either one of the CRD_VCC output is overloaded. On the other hand, the pin is forced to a logic High when the input voltage V_{CC} drops below 2.0 V min. The associated pull up resistor is either connected to V_{CC} (EN_RPU = H) or disconnected when EN_RPU = Low.
48	ANLG_GND	GROUND	This pin is the ground reference for both analog and digital signals and must be connected to the system Ground. Care must be observed to provide a copper PCB layout designed to avoid small signals and power transients sharing the same track. Good high frequency techniques are strongly recommended.

MAXIMUM RATINGS

POWER SUPPLY SECTION General test conditions, unless otherwise specified: Operating temperature: −25°C < T_A < +85°C, V_{CC} = +3.0 V, CRD_VCC_A = CRD_VCC_B = +5.0 V.

Rating	Symbol	Pin	Min	Typ	Max	Unit
I_{out} = 2 x 65 mA (both external cards running simultaneously) @ 3.0 V < V_{CC} < 5.5 V	CRD_VCC	29, 32	4.6	–	5.4	V
I_{out} = 2 x 55 mA per pin (both external cards running) V_{out} defined @ CRD_VCC = 3.0 V @ 3.0 V < V_{CC} < 5.5 V	CRD_VCC	29, 32	2.7	–	3.3	V
I_{out} = 2 x 35 mA per pin (both external cards running) V_{out} defined @ CRD_VCC = 1.80 V @ 3.0 V < V_{CC} < 5.5 V	CRD_VCC	29, 32	1.65	–	1.95	V
Output Card Supply Voltage Ripple (per CRD_VCC outputs) @ : L_{out} = 22 μH, L_{ESR} < 2.0 Ω, C_{out} = 10 μF per CRD_VCC (Note 5) I_{out} = 35 mA, V_{out} = 1.80 V I_{out} = 55 mA, V_{out} = 3.0 V I_{out} = 65 mA, V_{out} = 5.0 V	 V_{ORA} V_{ORB}	 29 32	 – – –	 – – –	 50 50 50	mV
DC/DC Dynamic Inductor Peak Current @ V_{bat} = 5.0 V, L_{out} = 22 μH, C_{out} = 10 μF CRD_VCC = 1.8 V CRD_VCC = 3.0 V CRD_VCC = 5.0 V	I_{ccov}	29, 32	 – – –	 200 280 430	 – – –	mA
Standby Supply Current Conditions (Note 5): ANLG_VCC = PWR_VCC = 3.0 V PWR_ON = H, STATUS = H, $\overline{CS}$ = H Card A and Card B CLOCK_IN = H, I/O = H, RESET = H All Logic Inputs = H, Temperature range = 0°C to +50°C ANLG_VCC = PWR_VCC = 5.0 V Temperature range –25°C to +85°C All other test conditions identical ANLG_VCC = PWR_VCC = 1.8 V Temperature range –25°C to +50°C All other test conditions identical Note: This parameter is guaranteed by design, not production tested.	I_{DD}	42, 28, 33	 – – – – – – –		 20 – – 50 – – 5.0 –	μA
Operating Supply Current ANLG_VCC = PWR_VCC = 5.5 V @ CRD_VCC_A/B = 5.0 V @ CRD_VCC_ A/B = 3.0 V @ CRD_VCC_ A/B = 1.85 V ANLG_VCC = PWR_VCC = 3.3 V @ CRD_VCC_A/B = 5.0 V @ CRD_VCC_ A/B = 3.0 V @ CRD_VCC_ A/B = 1.85 V PWR_ON = H, $\overline{CS}$ = H, CLK_A = CLK_B = Low, all card pins unloaded	I_{DDop}	42, 28, 33		 0.7 0.7 0.7 0.2 0.2 0.2		mA
V_{bat} Under Voltage Detection Positive Going Slope V_{bat} Under Voltage Detection Negative Going Slope V_{bat} Under Voltage Detection Hysteresis Note: The voltage present in pins 28 and 33 must be equal to or lower than the voltage present in pin 42.	V_{batLH} V_{batLL} V_{batHY}	42	2.1 2.0 –	– – 100	2.7 2.6 –	V V mV
Output Continuous Current Card A or Card B (both cards can be operating simultaneously) @ 3.0 < V_{CC} < 5.5 V Output Voltage = 1.85 V Output Voltage = 3.0 V Output Voltage = 5.0 V	I_{ccp}	31, 42	 35 55 65			mA
Output Over Current Limit (A or B) V_{bat} = 3.3 V, CRD_VCC = 1.8 V, 3.0 V or 5.0 V V_{bat} = 5.0 V, CRD_VCC = 1.8 V, 3.0 V or 5.0 V	I_{ccov}	31, 42		 100 150		mA
Output Over Current Time Out Per Card	I_{tdoff}	31, 42		4.0		ms
Output Card Supply Turn On Time @ L_{out} = 22 μF, C_{out} = 10 μF Ceramic. V_{CC} = 2.7 V, CRD_VCC = 5.0 V (A or B)	V_{CCTON}	31, 42			 500	μs

5. Assuming ANLG_VCC and PWR_VCC pins are connected to the same power supply.

POWER SUPPLY SECTION General test conditions, unless otherwise specified: Operating temperature: −25°C < T_A < +85°C, V_{CC} = +3.0 V, CRD_VCC_A = CRD_VCC_B = +5.0 V. (continued)

Rating	Symbol	Pin	Min	Typ	Max	Unit
Output Card Supply Shut Off Time @ C_{out} = 10 μF, ceramic. V_{CC} = 2.7 V, CRD_VCC = 5.0 V, V_{CCOFF} < 0.4 V (A or B)	V_{CCTOFF}	31, 42		100	250	μs
DC/DC Converter Operating Frequency (A or B)	F_{SW}	31, 42		600		kHz

5. Assuming ANLG_VCC and PWR_VCC pins are connected to the same power supply.

DIGITAL INPUT/OUTPUT SECTION

2.70 < V_{CC} < 5.50 V, Normal Operating Mode (−25°C to +85°C ambient temperature, unless otherwise noted)

Rating	Symbol	Pin	Min	Typ	Max	Unit
A0, A1, A2, A3, CARD_SEL, PWR_ON, $\overline{PGM}$, $\overline{CS}$, MUX_MODE, EN_RPU, RESET_A, $\overline{RESET\_B}$, $\overline{C4\_A}$, C8_A, C4_B, $\overline{C8\_B}$ High Level Input Voltage Low Level Input Voltage Input Capacitance	 V_{IH} V_{IL} C_{in}	1, 2, 3, 4, 5, 6, 7, 8, 44, 45, 10, 18, 11, 12, 16, 17	0.7 * V_{bat}		 V_{bat} 0.3 * V_{bat} 10	 V V pF
STATUS, $\overline{INT}$ Output High Voltage @ I_{OH} = −10 μA Output Low Voltage @ I_{OH} = 200 μA	 V_{OH} V_{OL}	46, 47	V_{bat} –1.0 V		 0.40	V

STATUS, $\overline{INT}$
Output Rise Time @ C_{out} = 30 pF
Output F_44 Tm-0.0022 Tc0 Tw(bat)Tj8 7 0 0 6.5 18102 Twime @ C

CARD INTERFACE SECTION @ 2.70 < V_{CC} < 5.50 V, Normal Operating Mode (−25°C to +85°C ambient temperature, unless otherwise noted) CRD_VCC_A = CRD_VCC_B = 1.8 V or 3.0 V or 5.0 V

Rating	Symbol	Pin	Min	Typ	Max	Unit
CRD_RST_A, CRD_RST_B Output Voltage						
Output RST High Level @ Irst = −200 μA	V_{OH}	23, 38	CRD_VCC−0.5		CRD_VCC	V
Output RST Low Level @ Irst = 200 μA	V_{OL}	23, 38	0		0.4	V
CRD_RST_A, CRD_RST_B Rise and Fall time						
RST Rise Time @ C_{out} = 30 pF	trrst	23, 38			100	ns
RST Fall Time @ C_{out} = 30 pF	tfrst	23, 38			100	ns

CRD_CLK_A, CRD_CLK_B Output Clock
Output Operating Clock Card A and Card B
Output Operating Clock DC, Card A and Card B
(Input DC = 50%, ±1%)
Note: This parameter is guaranteed by design, functionality 100% tested at production.
Output Operating Clock Rise Time SLOW Mode
Card A and Card B

rd A and Card B

rd A and Card B
()Tj and Tf0.54 TD-0.B

DIGITAL DYNAMIC SECTION NORMAL OPERATING MODE

Rating	Symbol	Pin	Min	Typ	Max	Unit
Card Signal Sequence Interval, CRD_VCC_A and CRD_VCC_B: CRD_IO_A, CRD_RST_A, CRD_CLK_A, CRD_C4_A, CRD_C8_A CRD_IO_B, CRD_RST_B, CRD_CLK_B, CRD_C4_B, CRD_C8_B	td_{seq}	24, 23, 30, 37, 38, 31		 0.5 0.5	 2 2	μs
Internal RESET Delay	td_{reset}			1.0		μs
Internal STATUS Delay Time	td_{ready}	46		1.0		μs
PWR_ON Low State Pulse Width (Figure 11), Assuming CRD_VCC reservoir capacitor = 10 μF.	t_{pwrlow}	8	 5			μs
PWR_ON High State Pulse Width (Figure 11)	t_{pwrset}	8	200			ns
PWR_ON Preset Delay (Figure 11)	t_{pwrpre}	5, 7, 8	300			ns
PWR_ON Programming Hold Time (Figure 11)	$t_{pwrhold}$	5, 7, 8	100			ns
PWR_ON to CARD_SEL Change Delay Time (Figure 12)	$t_{cseldly}$	5, 6, 8	100			ns
$\overline{PGM}$ to PWR_ON Delay Time (Figure 12)	tpgmdly	5, 6, 8	300			ns
PWR_ON internal Set/Reset Pulses Width (Figure 12)	tpwrp	8		20		ns

DIGITAL DYNAMIC SECTION PROGRAMMING MODE

Rating	Symbol	Pin	Min	Typ	Max	Unit
Data Set−up Time, Time Reference = $\overline{PGM}$, A0, A1, A2, A3, CARD_SEL, and $\overline{CS}$. Data Signal Rise and Fall Time	t_{smod} t_{smodtr}	8, 46, 1, 2, 3, 4, 5, 6	100		 50	ns ns
Data Hold Time, Time Reference = $\overline{PGM}$, A0, A1, A2, A3, CARD_SEL, and $\overline{CS}$.	t_{smod} t_{smodtr}	8, 46, 1, 2, 3, 4, 5, 6	100		 50	ns ns
Chip Select $\overline{CS}$ Low State Pulse Width $\overline{CS}$ Signal Rise and Fall Time	t_{wcs} t_{rfcs}	7	300		 50	ns ns

PROGRAMMING AND STATUS FUNCTIONS

The NCN6004A includes a programming interface and a status interface. Figure 4 illustrates the sequence one must follow to enter and exit the programming mode. Table 1 and Table 2 provide the logical functions associated with the input and output signals. The parameters are latched upon the rising edge of the $\overline{PGM}$ signal, the $\overline{CS}$ pin being held low. Any number of programming sequences can be performed while the $\overline{CS}$ pin is Low, but the minimum timings must be observed.

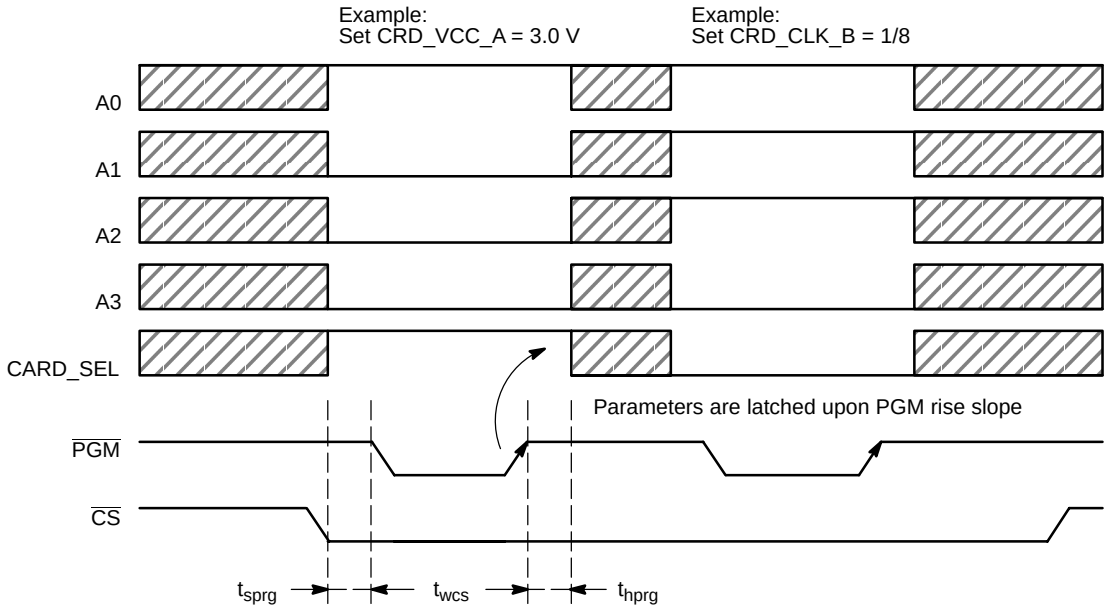


Figure 4. Programming Sequence

On the other hand, since the programming data are latched upon the rising edge of the $\overline{PGM}$ signal, the most up to date selected card (using CARD_SEL = H or L) is used to activate the associated card. Consequently, when both cards must be updated with the same programmed content, a dual $\overline{PGM}$ sequence must be carried out, changing the CARD_SEL signal during the High level state of the $\overline{PGM}$ pin.

Although selecting a card in possible during the same Chip Select sequence (as depicted here above), the user must make sure that no data will be present to a card not ready for such a function. As a matter of fact, all the card signals are routed to the selected card immediately after a CARD_SEL change, the NCN6004A taking no further logic control prior to activate the swap. To avoid any risk, one can run a sequence with the selected card, return $\overline{CS}$ to High, change the CARD_SEL according to the expected card selection, and pull $\overline{CS}$ to Low to activate the selected card.

Table 1. Programming and Reading Basic Functions

Pin	Name	Select #A #B	Select V_{CC} ON/OFF	Program CLOCK_IN	Poll Card Status #A or #B	Poll I_{CC} Overload #A or #B	ANLG_VCC Input Voltage OK
7	$\overline{CS}$	0	0	0	0	0	0
46	STATUS	–	–	–	READ	READ	READ
1	A0	0/1	0/1	0/1	1	0	0
2	A1	0/1	0/1	0/1	1	1	0
3	A2	0/1	0/1	0/1	X	X	X
4	A3	0/1	0/1	0/1	X	X	X
5	CARD_SEL	0/1	0/1	0/1	0/1	0/1	0/1
6	$\overline{PGM}$	0/1	0/1	0/1	1	1	1

Table 2. Programming Functions (Conditions at start−up are in **Bold**)

(HEX)	$\overline{\text{PGM}}$	A3	A2	A1	A0

Table 3. Status Pins Data

STATE (HEX)	$\overline{PGM}$	A3	A2	A1	A0	CARD_SEL	STATUS #A	STATUS #B
00	1	X	X	0	0	X	Vcc_V_{bat}_OK Pass = Low VCC_OK Fail = High	
01	1	X	X	0	1	1	CRD_VCC_A In Range Pass = High Fail =Low	
02	1	X	X	1	0	1	CRD_VCCA Overloaded Pass = High Fail = Low	
03	1							

PARALLEL/MULITPLEXED OPERATION MODES

The logic input MUX_MODE, pin 44, provides a way to select the operation mode of the NCN6004A. Depending upon the logic level, the device operates either in a parallel mode (all the card pins, on the μP side, are fully independent) or in multiplexed mode (all the logic card pins, on the μP side, share a common bus). Figure 6 shows a simplified schematic of the multiplex circuit built in the NCN6004A chip.

Figure 6. Simplified MUX_MODE Logic and Multiplex Circuit

to either CARD_A or CARD_B. It is neither possible to connect directly I/O_A to I/O_B nor to connect the I/O_B pin to ground or voltage supply.

The multiplexer is activated and the CARD_SEL signal is used to select the card in use for a given transaction. The switches Q1, Q2 and Q3 and swapped to the A position, thus providing a path for the control signals applied to the CARD_A side.

When the CARD_SEL signal flips from one card to the other, the previous logic states of the on going card are latched in the chip and the related output card pin are maintained at the appropriate levels. When the system resumes to the previous card, the latches return to the transparent operation and the signals presented by the μP take priority over the previously latched states.

On the other hand, the input clocks (CLK_IN_A and CLK_IN_B) are maintained independent and can be routed to either CARD_A or CARD_B according to the programming functions given in Table 2.

CARD POWER SUPPLY TIMING

When the PWR_ON signal is high, the associated CRD_VCC_A or CRD_VCC_B power supply rise time depends upon the current capability of the DC/DC converter together with the external inductors L1/L2 and the reservoir capacitor connected across each card power supply pin and GROUND.

On the other hand, at turn off, the CRD_VCC_A and CRD_VCC_B fall times depend upon the external reservoir capacitor and the peak current absorbed by the internal NMOS device built across each CRD_VCC_A/ CRD_VCC_B and GROUND. These behaviors are depicted by Figure 7, assuming a 10 μF output capacitor.

Since none of these parameters can have infinite values, the designer must take care of these limits if the t_{ON} or the t_{OFF} provided by the data sheets does not meet his requirement.

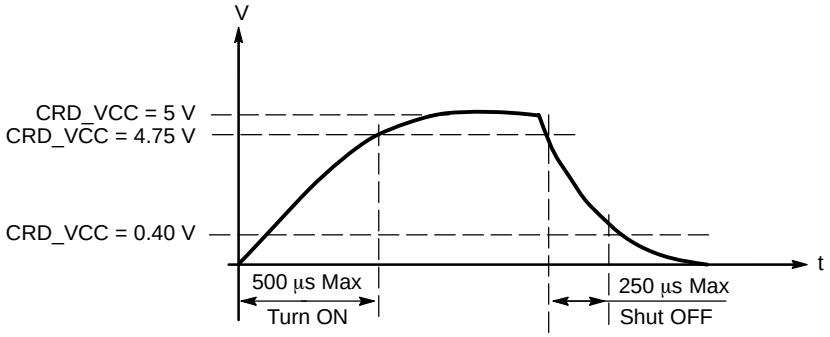
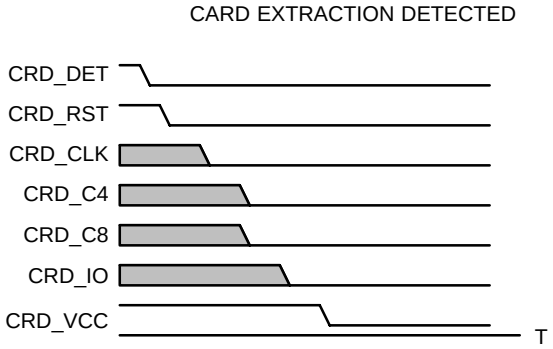


Figure 7. Card Power Supply Turn ON and Shut OFF Typical Timings

POWER DOWN OPERATION

The power down mode can be initiated by either the external MPU or by the internal error condition. The communication session is terminated immediately, according to the ISO7816−3 sequence. On the other hand, the MPU can run the Stand By mode by forcing $\overline{CS}$ = H, leaving the chip in the previous operating mode.

When the card is extracted, the interface will detect the operation and will automatically run the Power Down Sequence of the related card as described by the ISO/CEI 7816−3 sequence depicted in Figure 8 and illustrated by the oscillogram in Figure 9.



On the other hand, the Power Down sequence is automatically activated when the V_{bat}

CARD DETECTION

The card detector circuit provides a constant low current to

POWER MANAGEMENT

The main purpose of the power management is to provides the necessary output voltages to drive the 1.80 V, 3.0 V or 5.0 V smart card types. On top of that, the DC/DC converter efficiency must absorb a minimum current on the V_{bat} supply.

Beside the power conversion, in the Stand by mode (PWR_ON = L), the power management provides energy to the card detection circuit only. All the card interface pins are forced to ground potential, saving as much current as possible out of the battery supply.

In the event of a power up request coming from the external MPU (CARD_SEL =H/L, PWR_ON = H, $\overline{CS}$ = L), the power manager starts the DC/DC converter related to the selected interface section.

When the selected section (either CRD_VCC_A or CRD_VCC_B) voltage reaches the programmed value (1.8 V, 3.0 V or 5.0 V), the circuit activates the card signals according to the following sequence:

CRD_VCC_x → CRD_IO_x → CRD_C4_x → CRD_C8_x → CRD_CLK_x → CRD_RST_x

The logic level of the data lines are asserted High or Low, depending upon the state forced by the external MPU, when the start−up sequence is completed. Under no situation the NCN6004A shall automatically launch a smart card ATR sequence.

At the end of the transaction, asserted by the MPU (CARD_SEL = H/L, PWR_ON = L, $\overline{CS}$ = L), or under a card extraction, the ISO7816−3 power down sequence takes place:

CRD_RST_x → CRD_CLK_x → CRD_C4_x → CRD_C8_x → CRD_IO_x → CRD_VCC_x

When $\overline{CS}$ = H, the bi−directional I/O lines (pins 9 and 19) are forced into the High impedance mode to avoid signal collision with any data coming from the external MPU.

OUTPUT VOLTAGE PROGRAMMING

The internal logic provides a reliable circuit to activate any of the DC/DC converters safely. In particular, the Turn On/Turn Off of these converters is edge sensitive and controlled by the rising/falling edges of the PWR_ON signal applied with Chip Select pin Low. The CARD_SEL signal is used to select either CRD_VCC_A or CRD_VCC_B as defined by the functions programming in Table 2.

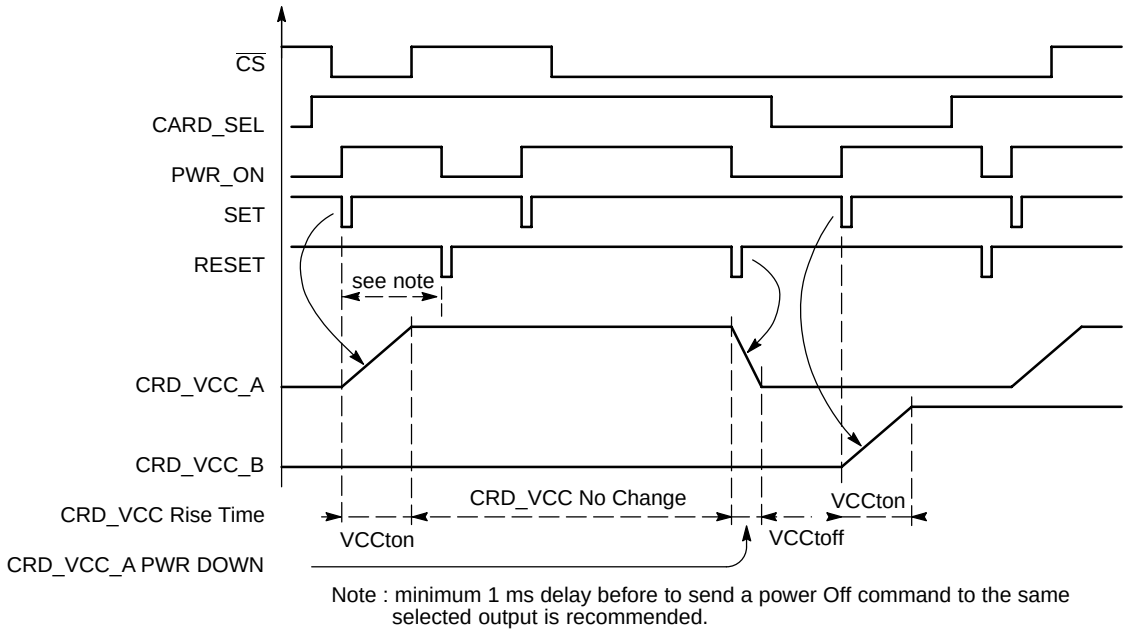


Figure 12. Card Power Supply Controls

Although it is possible to change the output voltage straightly from 5.0 V to 1.80 V, care must be observed as the stabilization time will be relatively long if no current is absorbed from the related output pin.

According to the typical sequence depicted, it is not possible to program simultaneously the two DC/DC converters,

When the output voltage reaches the specified value (1.80 V or 3.0 V or 5.0 V), Q1 and Q16 are switched OFF immediately to avoid over voltage on the output load. In the mean time, the two extra NMOS Q2 and Q3 are switched ON to fully discharge any current stored into the inductor, avoiding ringing and voltage spikes over the system. Figure 16 illustrates the theoretical basic waveforms present in the DC/DC converter.

The control block gives the logic states according to the bits provided by the external μP. These controls bits are applied to the selected DC/DC converter to generate the programmed output voltage. The MOS drive block includes the biases necessaries to drive the NMOS and PMOS devices as depicted in the block diagram given Figure 15.

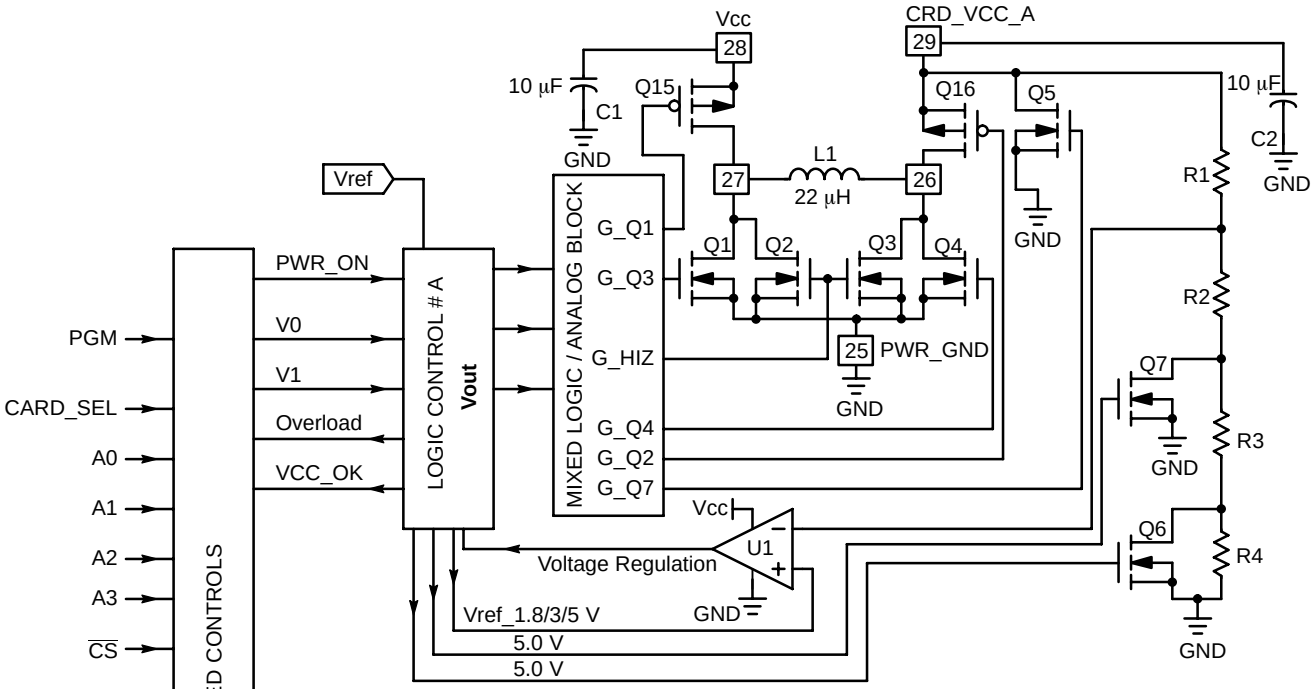
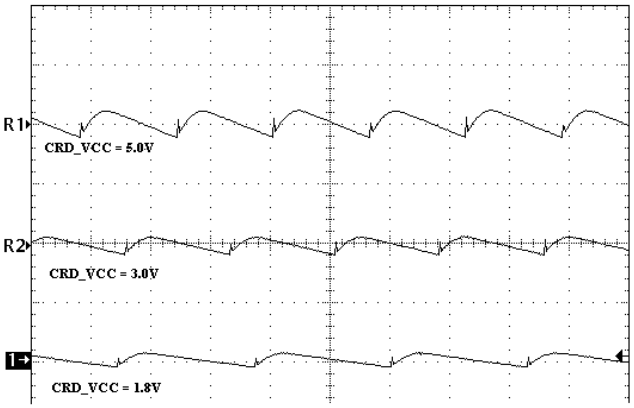
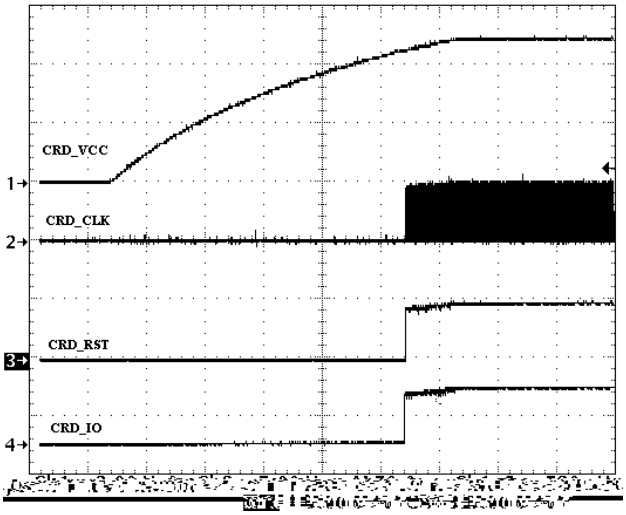


Figure 15. Basic DC/DC Converter Diagram

Since the output inductor L1 and the reservoir capacitor C1 carry relative high peak current, low ESR devices must be used to prevent the system from poor output voltage ripple and low efficiency. Using ceramic capacitors, X5R or X7R type, are recommended, splitting the 10 μF in two separate parts when there is a relative long distance between the CRD_VCC_x output pin and the card VCC input. On the other hand, the inductor shall have an ESR below 1.0 Ω to achieve the high efficiency over the full temperature range.





NOTE: Operating conditions under full output load.

Figure 17. Typical CRD_VCC Ripple Voltage

Figure 18. Typical Card Voltage Turn ON and Start−up Sequence

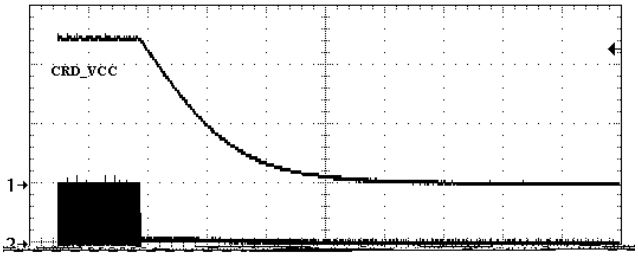


Figure 19. Typical Card Supply Turn OFF

74

72

70

68

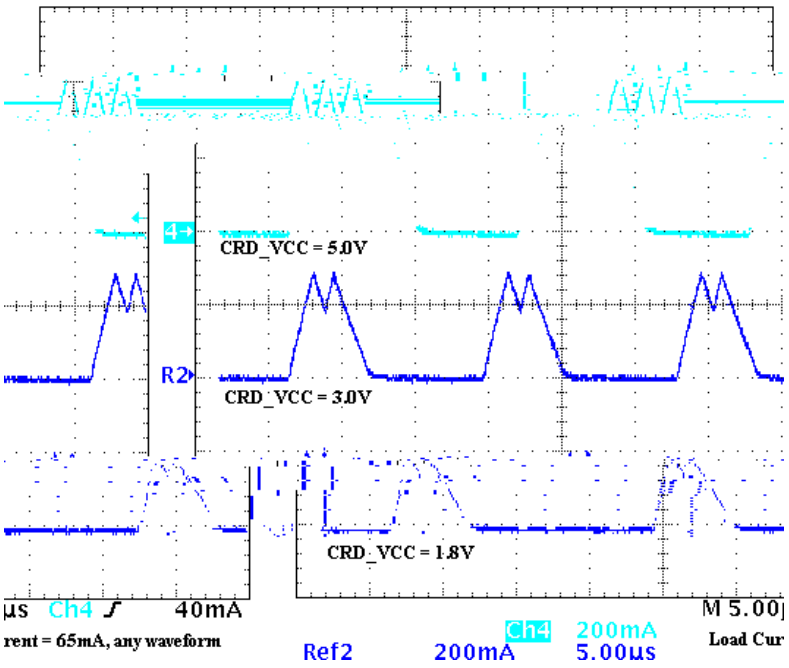
66

64

62

60

58



Test conditions: Input V_{CC} voltage = 5.0 V, Current = 200 mA /div,
T_{amb} = +20°C

Figure 21. Typical Output Voltage Ripple

According to the ISO7816−3 and EMV specifications, the

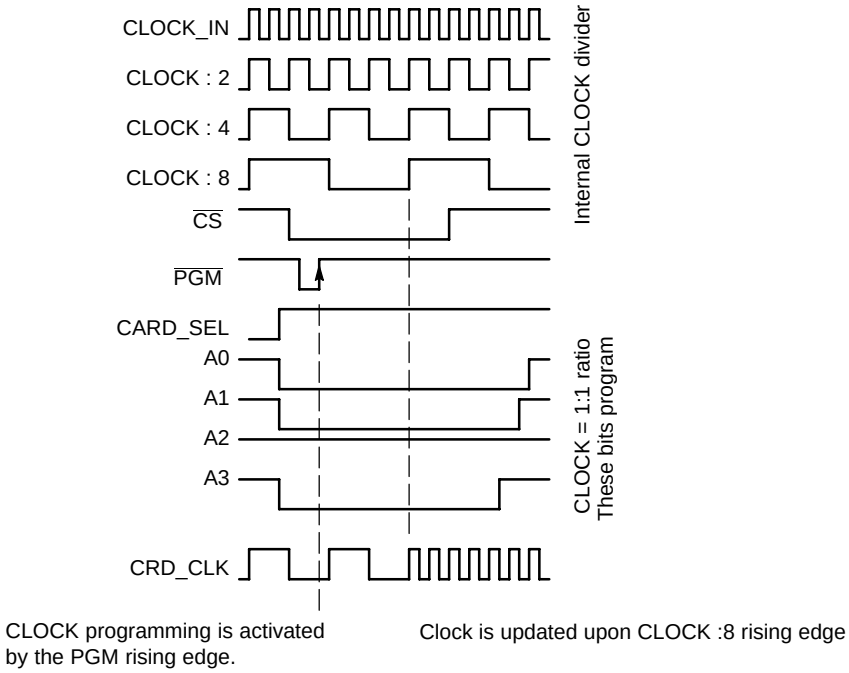


Figure 25. Clock Programming Timings

The example given in Figure 25 highlights the delay coming from the internal clock duty cycle re−synchronization. Since the clock signal is asynchronous, it is up to the programmer to make sure the next card transaction is not activated before, respectively, either the CRD_CLK_A or CRD_CLK_B signal has been updated. Generally speaking, such a delay can be derived from the maximum clock frequency provided to the interface.

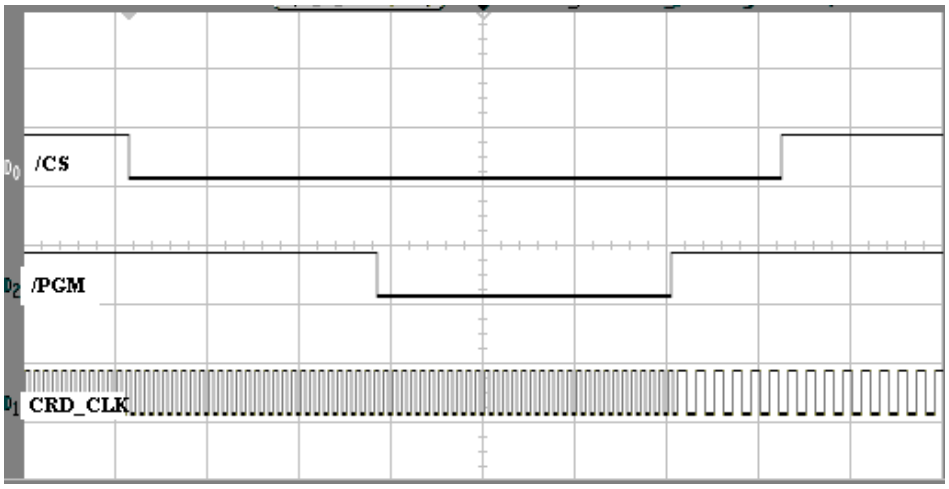


Figure 26. Card Clock 1/2 Divider Operation

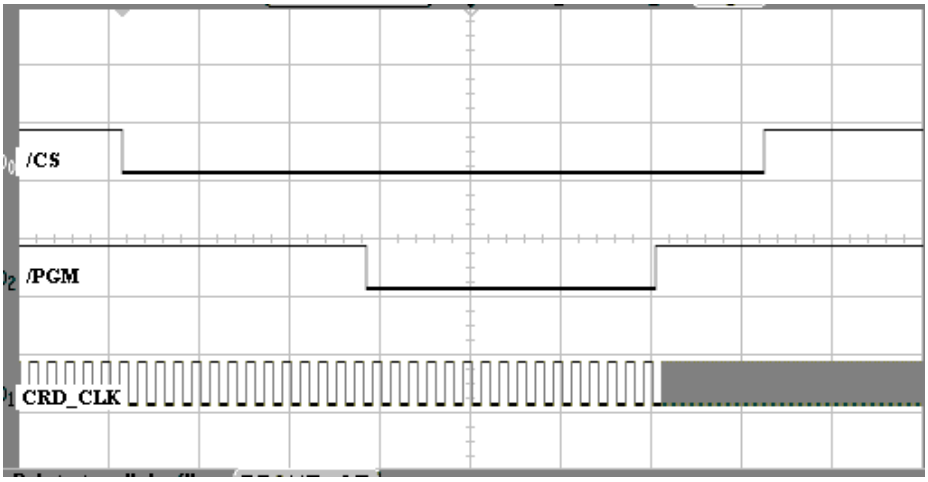


Figure 27. Clock Divider: 8 to 1 Operation

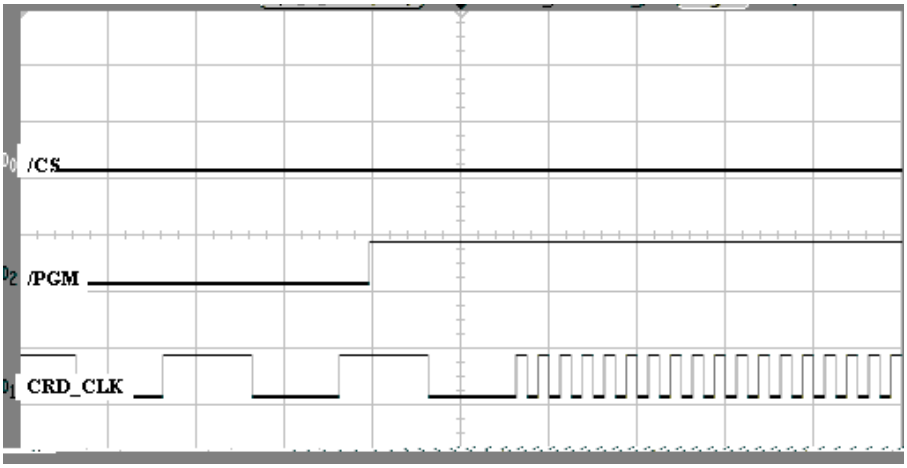


Figure 28. Clock Divider Timing Details

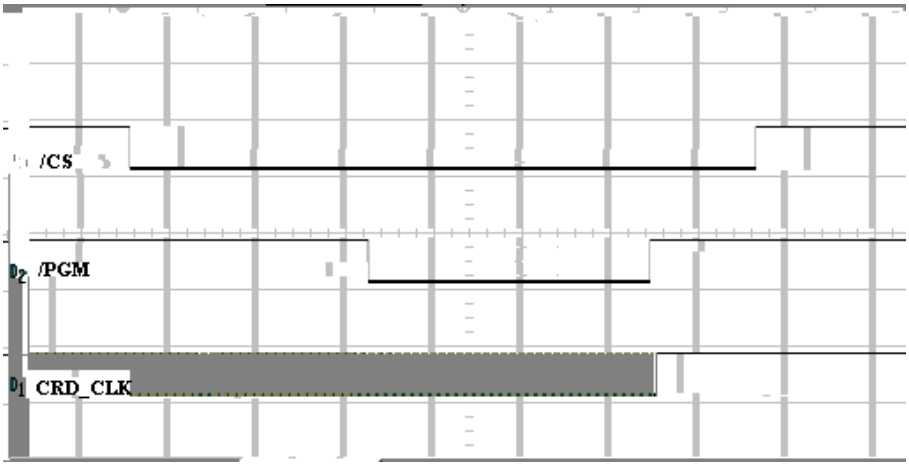


Figure 29. Clock Divider: Run to Stop High Operation

The input clock A and B can be re routed to either CRD_CLK_A or CRD_CLK_B output pins by using the programming function as defined in Table 2 and Table 7. The clock signals can have any frequency value necessary to handle a given type of card (asynchronous or synchronous). These clock signals can be multiplexed at any time, but the system must be locked in a safe state prior to make such a change. In particular, the designer must make sure that A and B cards can support such a hot change prior to change the related clocks.

Table 7. Programming Clock Routing

STATE	$\overline{CS}$	$\overline{PGM}$	A3	A2	A1	A0	CARD_SEL

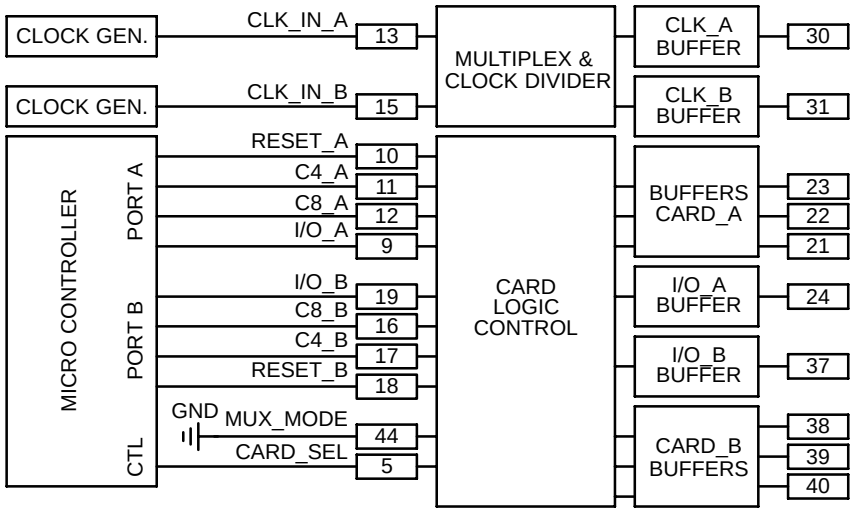


Figure 31. Parallel Operation Wiring → MUX_MODE = Low

When the chip operates in the parallel mode, all the logic signals must be independently controlled by the microcontroller as depicted in Figure 31. The MUX_MODE pin must be hardwired to VCC and it cannot be changed during an operation of the chip. Beside this parameter, the user must select to force or not the internal pull up resistors as defined by the EN_RPU logic state.

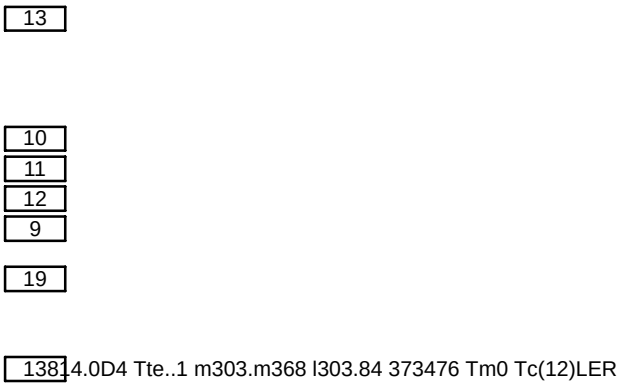


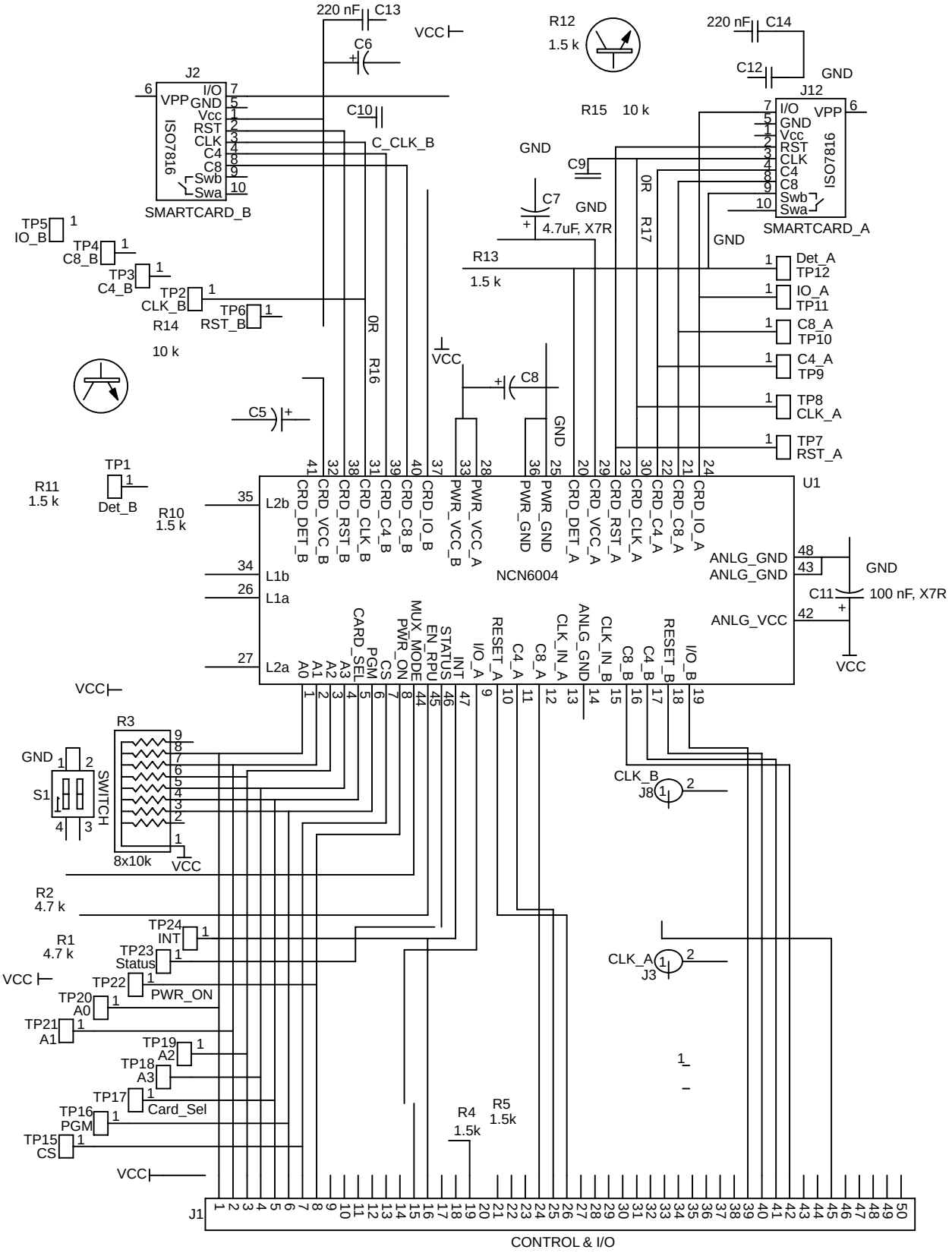
Figure 32. Multiplexed Operation Wiring → MUX_MODE = High

MUX_MODE = Low → PARALLEL OPERATION

The bi−directional switch Q9 is OFF and the I/O signals are routed straightforward to their appropriate outputs. The two I/O lines can operate simultaneously, depending upon the μP capabilities, regardless of the CARD_SEL signal logic level.

The pull up resistors, on the μP side of each I/O line, can be connected or not as defined by the EN_RPU signal.

TEST BOARD SCHEMATIC DIAGRAM



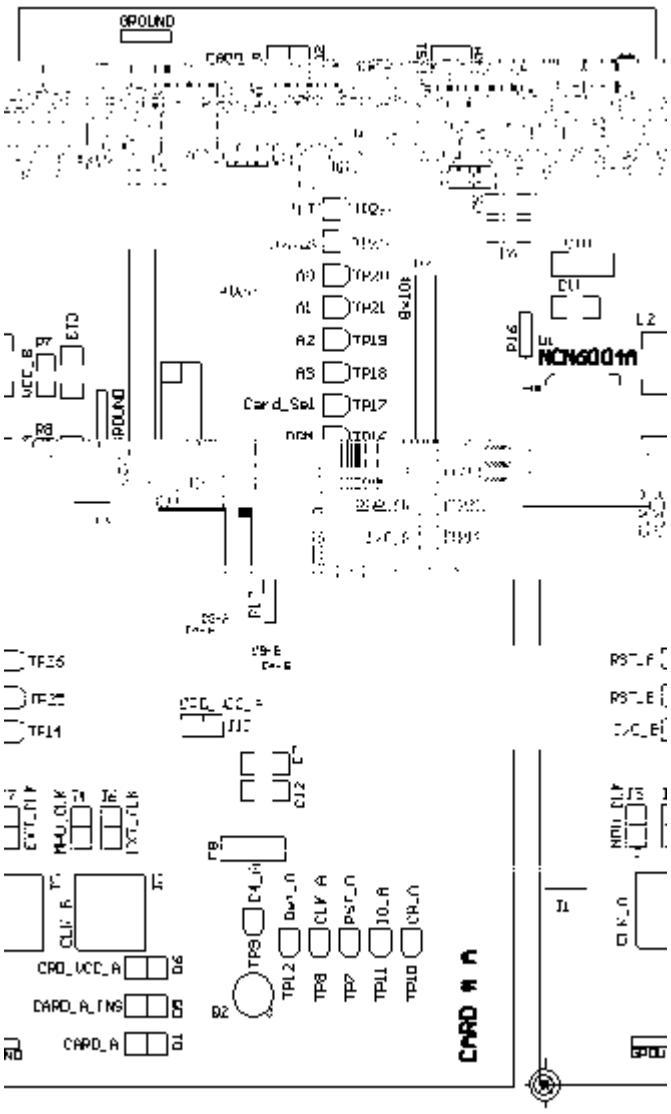


Figure 36. Demo Board PCB Top Overlay

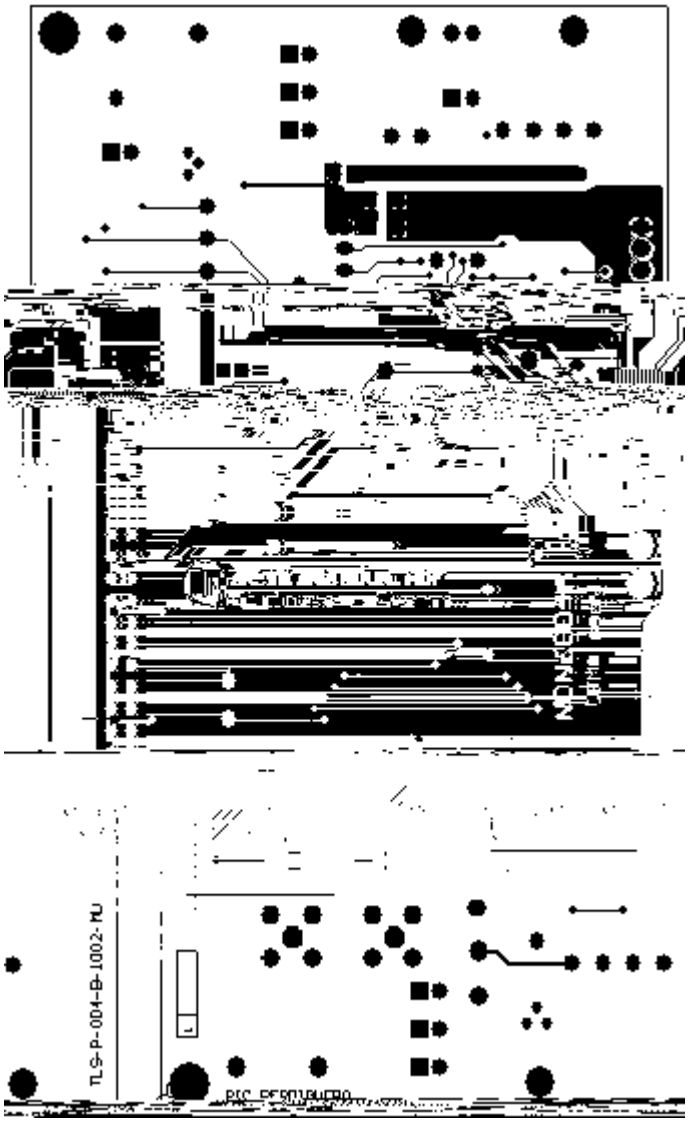


Figure 37. Demo Board PCB Top Layer

ABBREVIATIONS

L1a and L1b	DC/DC external inductor #A	**CRD_VCC_A**	Interface IC Card #A Power Supply Line
L2a and L2b	DC/DC external inductor #B	**CRD_CLK_A**	Interface IC Card #A Clock Input
Cout	Output Capacitor	**CRD_RST_A**	Interface IC Card #A RESET Input
CRD_VCC	Card Power Supply Input	**CRD_IO_A**	Interface IC Card #A Data link
VCC	MPU Power Supply Voltage	**CRD_C4_A**	Interface IC Card #A Data Control
Icc	Current at card VCC pin	**CRD_C8_A**	Interface IC Card #A Data Control
Class A	5 V Smart Card	**CRD_DET_A**	Card insertion/extraction detection
$\overline{CS}$	Chip Select	**CARD_SEL**	Card #A/B Selection bit
CRD_CLK_B	Interface IC Card #B Clock Input		
CRD_IO_B	Interface IC Card #B Data link	**EN_RPU**	Enable/Disable internal pull up
CRD_IO_B	Interface IC Card #B RESET Input	**$\overline{PGM}$**	Chip Programming Mode
EMV	Euro Card Master Card Visa	**ISO**	International Standards Organization
Class B	3 V Smart Card	**CRD_VCC_B**	Interface IC Card #B Power Supply Line
ANLG_VCC = VCC = V_{bat}	Input Voltage	**CRD_C4_B**	Interface IC Card #B Data Control
PWR_ON	Chip Power On bit	**CRD_C8_A**	Interface IC Card #B Data Control
MUX_MODE	Card Multiplex or Parallel Op.		
CRD_DET_B	Card insertion/extraction detection	**T0**	Smart Card Data transfer procedure by bytes
T1	Smart Card Data transfer procedure by strings	**μC**	Microcontroller

SEATING