© Semiconductor Components Industries, LLC, 2006

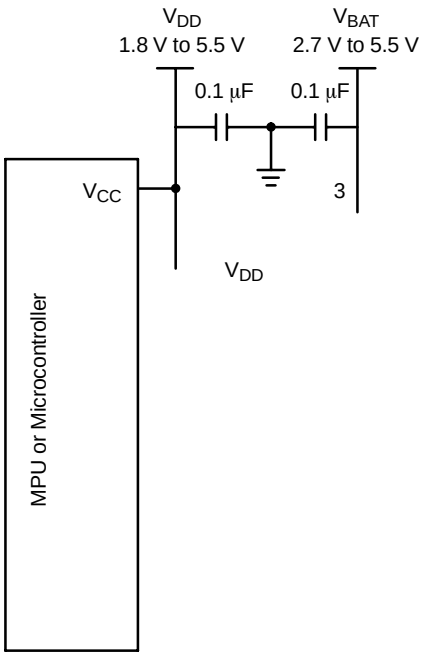


Figure 1. Typical Interface Application

Figure 3. NCN4557 Block Diagram

PIN DESCRIPTIONS

PIN	Name	Type	Description
1	CRD_V_{CC}B	POWER	This pin is connected to the Card power supply pin (C1) (Card B).The corresponding LDO is programmable using the pins SEL0, SEL1 and ENABLE to provide 1.8 V, 3.0 V or 0 V (disable).
4	.edo- 5.8CRD_V_{CC}B can not be active when CRD_V_{CC}A is active and conversely.		
2	V_{DD}	POWER	This pin is connected to the controller power supply. It configures the level shifter input stage to accept the signal coming from the microcontroller. A 0.1 μF capacitor shall be used to bypass the power supply voltage. When V_{DD} is below 1.5 V typical CRD_V_{CC}A and B are disabled; the NCN4557 comes into a shutdown mode.
3	V_{BAT}	POWER	DC/DC converter power supply input shared by the LDOs A & B. This pin has to be bypassed by a 0.1 μF capacitor.
4	CRD_V_{CC}A	POWER	

ATTRIBUTES

Characteristics		Values
ESD protection Human Body Model (HBM): Card Pins (1, 4, 5, 6, 7, 14, 15 , 16 & 17) (Note 1) All Other Pins (Note 1) Machine Model (MM): Card Pins (1, 4, 5, 6, 7, 14, 15 , 16 & 17) All Other Pins Charged Device Model (CDM): Card Pins (1, 4, 5, 6, 7, 14, 15 , 16 & 17) All Other Pins		 8 kV 2 kV 600 V 200 V 2 kV 400 V
Moisture sensitivity (Note 2)	QFN−16	Level 1
Flammability Rating	Oxygen Index: 28 to 34	UL 94 V−0 @ 0.125 in
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test		

1. Human Body Model (HBM): R =1500 Ω, C = 100 pF.
2. For additional information, see Application Note AND8003/D.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
LDO Power Supply Voltage	V_{BAT}	$-0.5 \le V_{BAT} \le 6$	V
Power Supply Microcontroller Side	V_{DD}	$-0.5 \le V_{DD} \le 6$	V
External Card Power Supply	CRD_V_{CC}	$-0.5 \le$ CRD_$V_{CC} \le 6$	V
Digital Input Pins	V_{in} I_{in}	$-0.5 \le V_{in} \le V_{DD} + 0.5$ but < 6.0 ±5	V mA
Digital Output Pins	V_{out} I_{out}	$-0.5 \le V_{out} \le V_{DD} + 0.5$ but < 6.0 ± 10	V mA
CRD Output Pins	V_{out}		
CRD_I/O & CRD_RST Pins CRD_CLK Pin	Iout		

POWER SUPPLY SECTION (−40°C to +85°C)

Pin	Symbol	Rating	Min	Typ	Max	Unit
3	V_{BAT}	Power Supply	2.7		5.5	V
3	I_{VBAT}	Operating current CRD_V_{CC}A = 3.0 V, CRD_V_{CC}B = 0 V, I_{CC}A & B = 0 mA CRD_V_{CC}A = 1.8 V, CRD_V_{CC}B = 0 V, I_{CC}A & B = 0 mA CRD_V_{CC}A = 0 V, CRD_V_{CC}B = 3.0 V, I_{CC}A & B = 0 mA CRD_V_{CC}A = 0 V, CRD_V_{CC}B = 1.8 V, I_{CC}A & B = 0 mA				

APPLICATION INFORMATION

The NCN4557 is a dual LDO−based DC/DC converter and level shifter able to handle independently 2 smart card interfaces. When one of these interfaces is operating the other one is not active and conversely. Class B (3.0 V) and C (1.8 V) cards can be used.

The Card and the CRD_V_{CC} power supply are selected using the pins SEL0, SEL1 and ENABLE according to Table 1.

Table 1. CARD AND CRD_V_{CC} SELECTION

ENABLE	SEL1	SEL0	Card# / CRD_V_{CC}
1	0	0	Card A / 1.8 V
1	0	1	Card A / 3.0 V
1	1	0	Card B / 1.8 V
1	1	1	Card B / 3.0 V
0	X	X	A & B Disabled

Card Supply Converter

The built−it NCN4557 DC/DC converters are Low Drop−Out Voltage Regulators capable to supply a current in excess of 50 mA under 1.8 V or 3.0 V. These voltages are selected according to Table 1. Using the Boolean input ENABLE pin the NCN4557 device can be disabled setting the circuit in a shutdown mode for which the power consumption features values typically in the range of a few tens of nA. Figure 9 shows a simplified view of the NCN4557 voltage regulator. The CRD_V_{CC} output is internally current limited and protected against short circuits. The short−circuit current IV_{CC} varies with V_{BAT} typically in the range of 30 mA to 60 mA.

In order to guarantee a stable and satisfying operating of the LDO the CRD_V_{CC} output will be connected to a 1.0 μF bypass ceramic capacitor to the ground. At the input, V_{BAT} will be bypassed to the ground with a 0.1 μF ceramic capacitor.

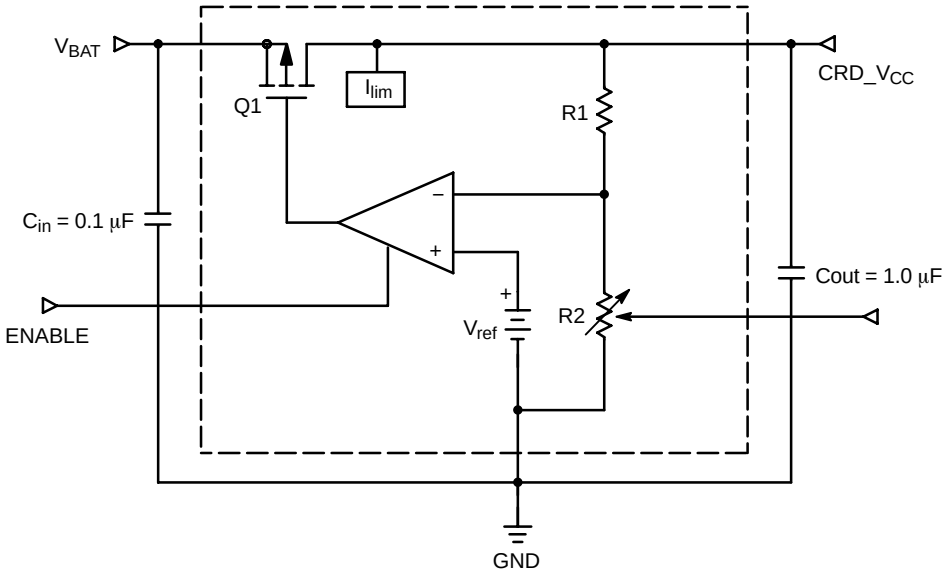


Figure 9. Simplified Block Diagram of the LDO Voltage Regulator

Level Shifters

The level shifters accommodate the voltage difference

this state or 8 μs after the ENABLE pin is set LOW in the other cases.

- CRD_I/O is forced to LOW about 8 μs after the ENABLE pin is set LOW.
- Then CRD_V_{CC} Supply Shuts Off

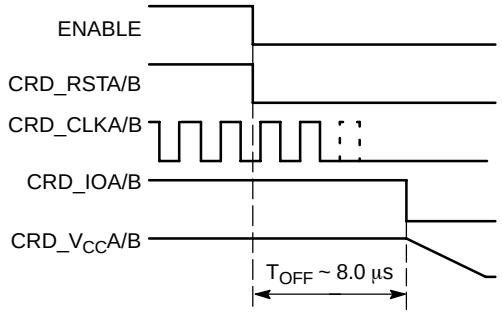
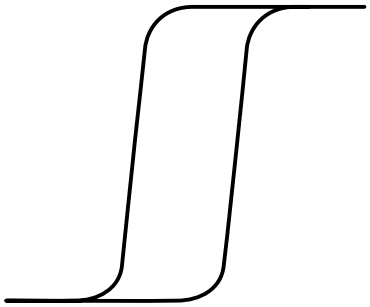


Figure 13. NCN4557 Power Down Sequence

Input Schmitt Triggers

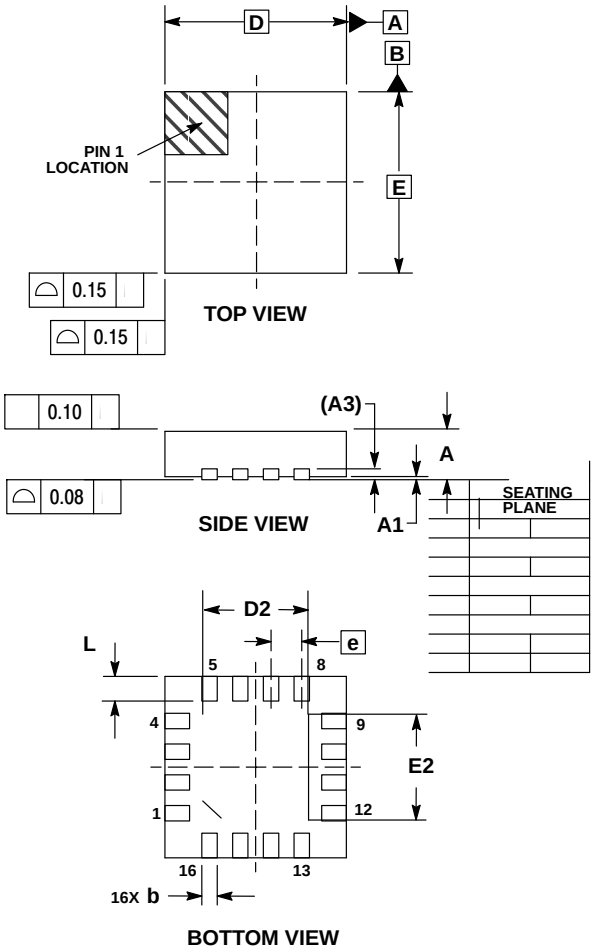
All the logic input pins (excepted I/O and CRD_I/O, Figure 3) have built−in Schmitt trigger circuits to prevent the NCN4557 against uncontrolled operation. The typical dynamic characteristics of the related pins are depicted in Figure 14.



QFN16 3*3*0.75 MM, 0.5 P
CASE 488AK−01
ISSUE O

DATE 13 SEP 2004

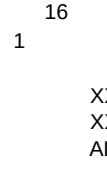
SCALE 2:1



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 MM FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
5. L_{max} CONDITION CAN NOT VIOLATE 0.2 MM SPACING BETWEEN LEAD TIP AND FLAG.

A1	0.00	0.05
A3	0.20 REF	
b	0.18	0.30

GENERIC
MARKING DIAGRAM*



XXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G”, may or not be present.

onsemi, , and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba “**onsemi**” or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi**’s product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent−Marking.pdf. **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided “as−is” and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi**