





# NCN4555

## PIN DESCRIPTIONS

PIN	Name	Type	Description
1	$\overline{\text{STOP}}$	INPUT	Power Down Mode pin: $\overline{\text{STOP}} = \text{Low} \rightarrow$ Low current shutdown mode activated $\overline{\text{STOP}} = \text{High} \rightarrow$ Normal Operation A Low level on this pin resets the SIM interface, switching off the SIM_VCC.
2	MOD_VCC	INPUT	The signal present on this pin programs the SIM_VCC value: MOD_VCC = Low $\rightarrow$ SIM_VCC = 1.8 V MOD_VCC = High $\rightarrow$ SIM_VCC = 3 V
3	V <sub>DD</sub>	POWER	This pin is connected to the system controller power supply. It configures the level shifter input stage to accept the signals coming from the microprocessor. A 0.1 $\mu\text{F}$ capacitor shall be used to bypass the power supply voltage. When V <sub>DD</sub> is below 1.1 V typical the SIM_VCC is disabled. The NCN4555 comes into a shutdown mode.
4	NC		No Connect
5	V <sub>BAT</sub>	POWER	DC-DC converter supply input. The input voltage ranges from 2.7V up to 5.5V. This pin has to be bypass by a 0.1 $\mu\text{F}$ capacitor.
6	NC		No Connect
7	SIM_VCC	POWER	This pin is connected to the SIM card power supply pin. An internal LDO converter is programmable by the external MPU to supply either 1.8 V or 3.0 V output voltage. An external 1.0 $\mu\text{F}$ minimum ceramic capacitor recommended must be connected across SIM_VCC and GND. During a normal operation, the SIM_VCC voltage can be set to 1.8 V followed by a 3.0 V value, or can start directly to any of these two values.
8	SIM_I/O	INPUT/ OUTPUT	Provides the connection to the serial I/O of the card connector. A bidirectional level shifter provides the serial I/O signal between the card and the micro controller. A 14 k $\Omega$ (typical) resistor provides a High impedance state for the SIM card I/O link.
9	SIM_RST	OUTPUT	Connected to the RESET pin of the card connector. A level translator adapts the (RST) signal to the SIM card.
10	GND	GROUND	GROUND reference for the integrated circuit and associated signals. Care must be taken to avoid voltage spikes when the device operates in a normal operation.
11	SIM_CLK	OUTPUT	Connected to the CLOCK pin of the card connector. The CLOCK (CLK) signal comes from an external clock generator, the internal level shifter being used to adapt the voltage defined on the card connector.
12	NC		No Connect
13	CLK	INPUT	The clock signal, coming from the external controller, must have a Duty Cycle within the Min/Max specified by the specification (typically 50%). The built-in level shifter translates the input signal to the internal SIM card CLK input.
14	RST	INPUT	The RESET signal present at this pin is connected to the SIM card through the internal level shifter which translates the level according to the SIM_VCC programmed value.
15	I/O	INPUT/ OUTPUT	This pin is connected to an external microcontroller or cellular phone management unit. A level shifter provides the connection to the external microcontroller or cellular phone management unit. A 14 k $\Omega$ (typical) resistor provides a High impedance state for the I/O link.

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## ATTRIBUTES

Characteristics	Values
ESD protection	

**NCN4555**

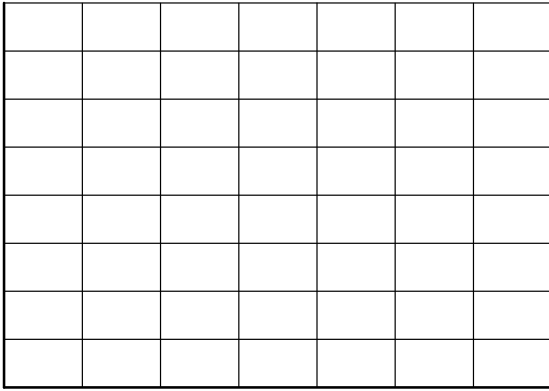
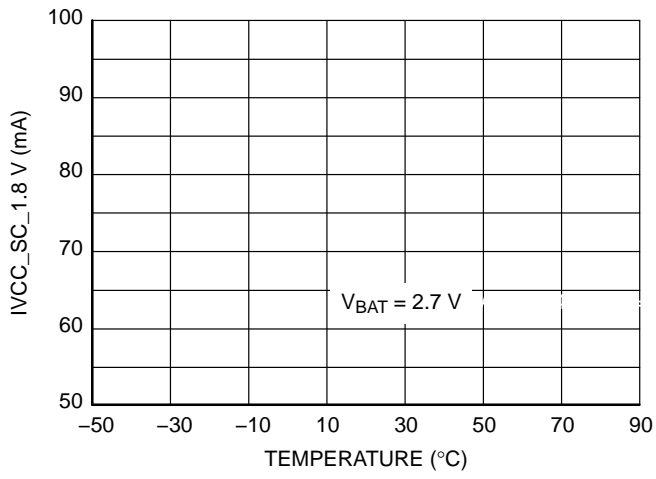
# NCN4555

## SIM INTERFACE SECTION (Note 10)

Pin	Symbol	Rating	Min	Typ	Max	Unit
9	SIM_RST	SIM_V <sub>CC</sub> = +3.0 V (MOD_V <sub>CC</sub> = High) Output RESET V <sub>OH</sub> @ I <sub>sim_rst</sub> =				

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## TYPICAL CHARACTERISTICS



APPLICATION INFORMATION

CARD SUPPLY CONVERTER

The NCN4555 interface DC-DC converter is a Low Dropout Voltage Regulator capable of supplying a current in excess of 50 mA under 1.8 V or 3.0 V. This device features a very low quiescent current typically lower than 25  $\mu$ A (Figure 6 and 7). MOD\_VCC is a select input allowing a logic level signal to select a regulated voltage of 1.8 V (MOD\_VCC = LOW) or 3.0 V (MOD\_VCC = HIGH). Additionally, the NCN4555 has a shutdown input allowing it to turn off or turn on the regulator output. The shutdown mode power consumption is typically in the range of a few tens of nA (30 nA Typical). Figure 8 shows a simplified view of the NCN4555 voltage regulator. The SIM\_VCC output is internally current limited and protected against short circuits. The short-circuit current  $I_{VCC}$  is constant over the temperature and SIM\_VCC. It varies with V\_BAT typically in the range of 60 mA to 90 mA (Figure 4 and 5).

In order to guarantee a stable and satisfying operating of the LDO the SIM\_VCC output will be connected to a 1.0  $\mu$ F bypass ceramic capacitor to the ground. At the input, V\_BAT will be bypassed to the ground with a 0.1  $\mu$ F ceramic capacitor.

LEVEL SHIFTERS

The level shifters accommodate the voltage difference that might exist between the microcontroller and the smart card. The RESET and CLOCK level shifters are monodirectional and feature both the same architecture.

The bidirectional I/O line provides a way to automatically adapt the voltage difference between the MCU and the SIM card in both directions. In addition with the pullup resistor, an active pullup circuit (Figure 8, Q1 and Q2) provides a fast charge of the stray capacitance, yielding a rise time fully within the ISO7816 specifications.

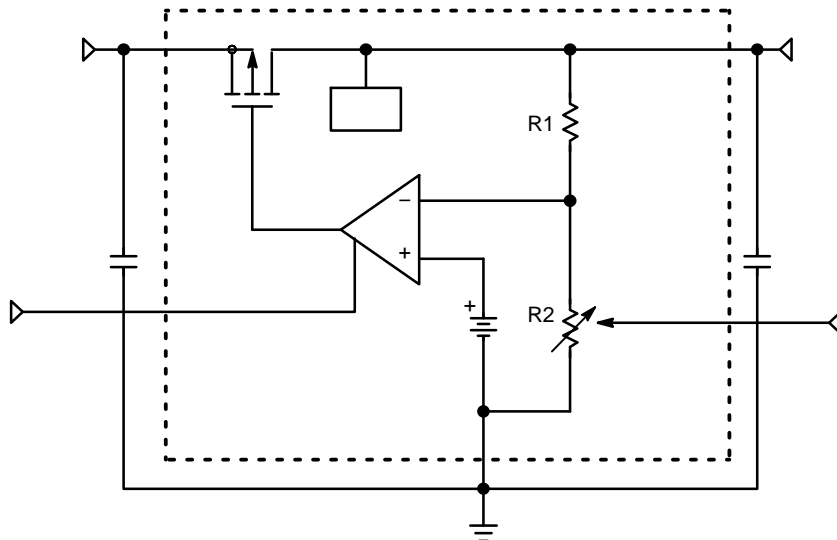


Figure 8. Simplified Block Diagram of the LDO Voltage Regulator



The typical waveform provided in Figure 10 shows how the accelerator operates. During the first 200 ns (typical), the slope of the rise time is solely a function of the pullup resistor associated with the stray capacitance. During this period, the PMOS devices are not activated since the input voltage is below their  $V_{gs}$  threshold. When the input slope crosses the  $V_{gsth}$ , the opposite one shot is activated, providing a low impedance to charge the capacitance, thus increasing the rise time as depicted in Figure 10. The same mechanism applies for the opposite side of the line to make sure the system is optimum.

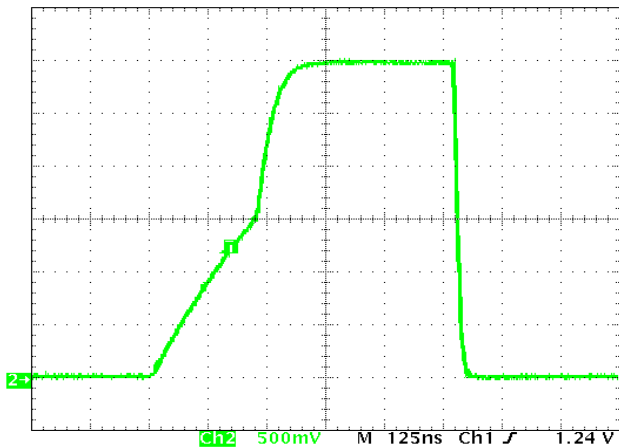
**INPUT SCHMITT TRIGGERS**

All the Logic input pins (excepted I/O and SIM\_I/O, See Figure 3) have built-in Schmitt trigger circuits to prevent the NCN4555 against uncontrolled operation. The typical dynamic characteristics of the related pins are depicted Figure 11.

The output signal is guaranteed to go High when the input voltage is above  $0.7 \times V_{DD}$ , and will go Low when the input voltage is below  $0.4 \text{ V}$ .

**SHUTDOWN OPERATING**

In order to save power or for other purpose required by the application it is possible to put the NCN4555 in a shutdown mode by setting Low the pin  $\overline{STOP}$ . On the other hand the device enters automatically in a shutdown mode when  $V_{DD}$  becomes lower than  $1.1 \text{ V}$  typically.



**Figure 10. SIM\_IO Typical Rise and Fall Times with Stray Capacitance > 30 pF (33 pF Capacitor Connected on the Board)**

**ESD PROTECTION**

The NCN4555 SIM interface features an HBM ESD voltage protection in excess of  $7 \text{ kV}$  for all the SIM pins (SIM\_IO, SIM\_CLK, SIM\_RST, SIM\_VCC and GND). All the other pins (microcontroller side) sustain at least  $2 \text{ kV}$ . These values are guaranteed for the device in its full integrity without considering the external capacitors added to the circuit for a proper operating. Consequently in the operating conditions it is able to sustain much more than  $7 \text{ kV}$  on its SIM pins making it perfectly protected against electrostatic discharge well over the HBM ESD voltages required by the ISO7816 standard ( $4 \text{ kV}$ ).

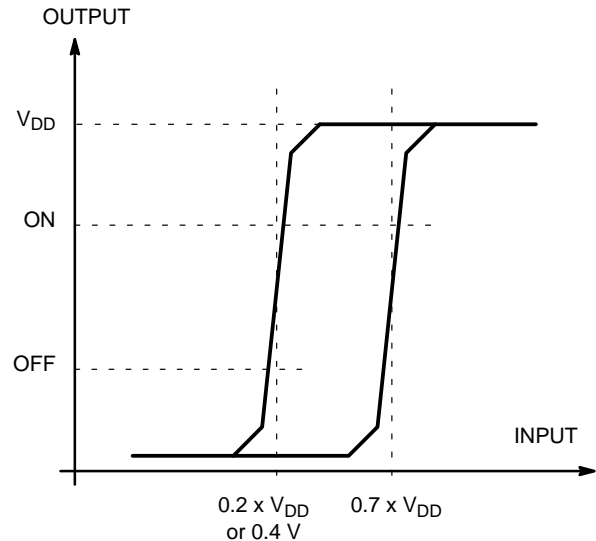
**PRINTED CIRCUIT BOARD LAYOUT**

Careful layout routing will be applied to achieve a good and efficient operating of the device in its mobile or portable environment and fully exploit its performance.

The bypass capacitors have to be connected as close as possible to the device pins (SIM\_VCC,  $V_{DD}$  or  $V_{BAT}$ ) in order to reduce as much as possible parasitic behaviors (ripple and noise). It is recommended to use ceramic capacitors.

The exposed pad of the QFN-16 package will be connected to the ground as well as the unconnected pins (NC). A relatively large ground plane is recommended.

Figures 12 and 13 shows an example of PCB device implementation in an evaluation environment.



**Figure 11. Typical Schmitt Trigger Characteristics**



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## EVALUATION BOARD AND PCB GUIDELINES

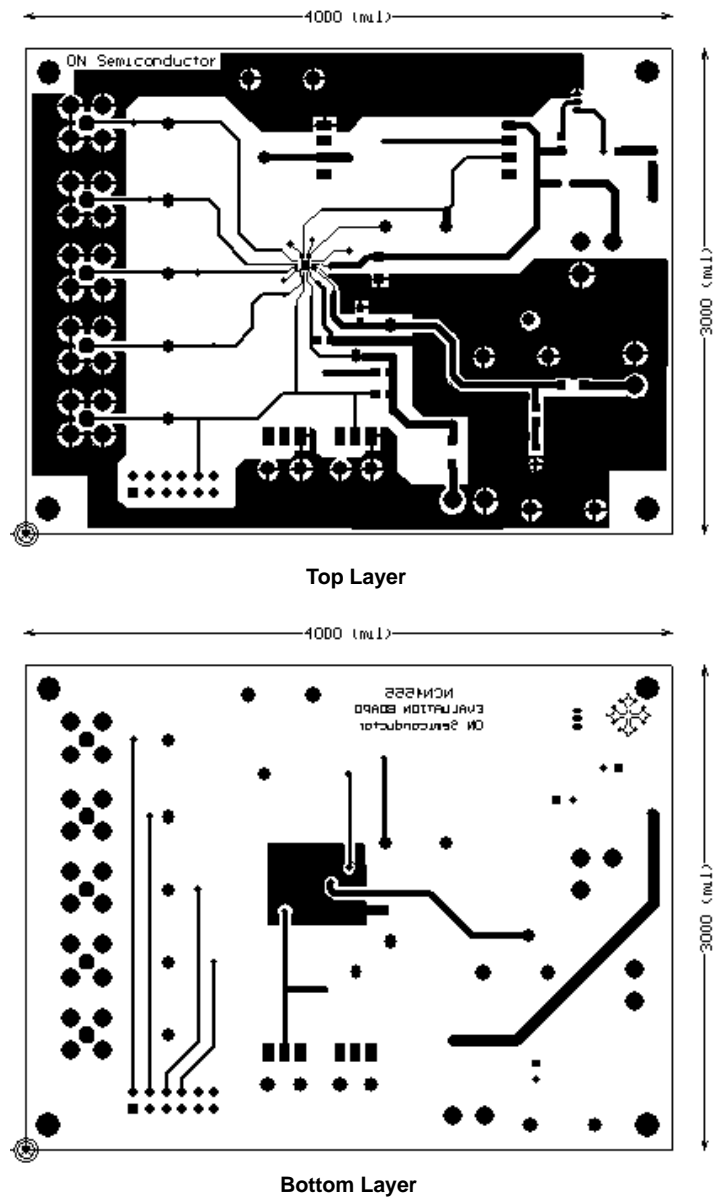


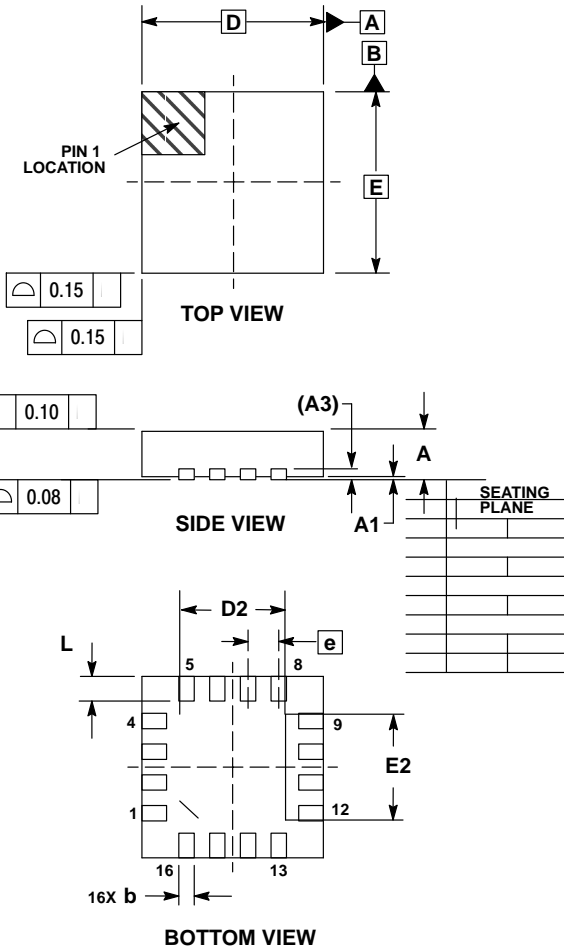
Figure 13. NCN4555 Printed Circuit Board Layout (Engineering board)



**QFN16 3\*3\*0.75 MM, 0.5 P**  
**CASE 488AK-01**  
**ISSUE O**

DATE 13 SEP 2004

SCALE 2:1



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 MM FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
5.  $L_{max}$  CONDITION CAN NOT VIOLATE 0.2 MM SPACING BETWEEN LEAD TIP AND FLAG.

A1	0.00	0.05
A3	0.20	REF
b	0.18	0.30

**GENERIC MARKING DIAGRAM\***

16  
 1  
 XXXX  
 XXXX  
 ALYW

XXXX = Specific Device Code  
 A = Assembly Location  
 L = Wafer Lot  
 Y = Year  
 W = Work Week

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G", may or not be present.

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