High Speed Dual-Channel, Ceramic Digital Isolator

Product Preview

NCID9200

Description

The NCID9200 is a galvanically isolated high−speed dual−channel digital isolator. This device supports isolated communications thereby allowing digital signals to communicate between systems without conducting ground loops or hazardous voltages.

It utilizes **onsemi**'s patented galvanic off−chip capacitor isolation technology and optimized IC design to achieve high insulation and high noise immunity, characterized by high common mode rejection and power supply rejection specifications. The thick ceramic substrate yields capacitors with ~25 times the thickness of thin film on−chip capacitors and coreless transformers. The result is a combination of the electrical performance benefits that digital isolators offer with the safety reliability of a >0.5 mm insulator barrier similar to what has historically been offered by optocouplers.

The device is housed in a 16−pin wide body small outline package.

Features

- Off−Chip Capacitive Isolation to Achieve Reliable High Voltage Insulation
  - DTI (Distance Through Insulation): Ø 0.5 mm
  - Maximum Working Insulation Voltage: 2000 V_{peak}
- 100 kV/ s Minimum Common Mode Rejection
- 8 mm Creepage and Clearance Distance to Achieve Reliable High Voltage Insulation
- Specifications Guaranteed Over 2.5 V to 5.5 V Supply Voltage and −40°C to 125°C Extended Temperature Range
- Over Temperature Detection
- NCIV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable (Pending)

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PIN CONFIGURATION

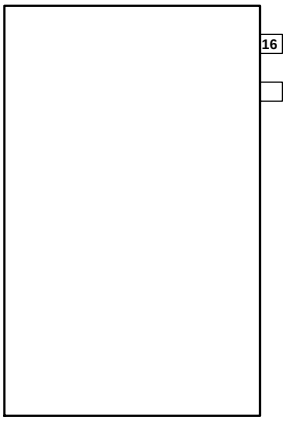

Figure 1. Pin and Channel Configuration

SPECIFICATIONS

TRUTH TABLE (Note 1)

V_{INX}	V_{DDI}	V_{DDO}	V_{OX}	Comment
H	Power Up	Power Up	H	Normal Operation
L	Power Up	Power Up	L	

ABSOLUTE MAXIMUM RATINGS (T_A = 25∀C unless otherwise specified)

Symbol	Parameter	Value	Unit
T_{STG}	Storage Temperature	−55 to +150	∀C
T_{OPR}	Operating Temperature	−40 to +125	∀C
T_J	Junction Temperature	−40 to +150	∀C
T_{SOL}	Lead Solder Temperature (Refer to Reflow Temperature Profile)	260 for 10 s	∀C
V_{DD}	Supply Voltage (V_{DDx})		

ELECTRICAL CHARACTERISTICS

Apply over all recommended conditions, T_A = −40°C to +125°C, V_{DD1} = V_{DD2} = 2.5 V to 5.5 V, unless otherwise specified. All typical values are measured at T_A = 25°C.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	Figure
V_{OH}	High Level Output Voltage	V_{DD} = 5 V, I_{OH} = −4 mA	V_{DDO} − 0.4	V_{DDO} − 0.1	−	V	7
		V_{DD} = 3.3 V, I_{OH} = −2 mA					
		V_{DD} = 2.5 V, I_{OH} = −1 mA					
V_{OL}	Low Level Output Voltage	V_{DD} = 5 V, I_{OL} = 4 mA	−	0.1	0.4	V	8
		V_{DD} = 3.3 V, I_{OL} = 2 mA					
		V_{DD} = 2.5 V, I_{OL} = 1 mA					
V_{INT+}	Rising Input Voltage Threshold		−	−	0.7 Δ V_{DDI}	V	
V_{INT-}							

SUPPLY CURRENT CHARACTERISTICS (continued)
Apply over all recommended conditions, T_A = −40°C to +125°C unless otherwise specified. All typical values are measured at T_A = 25°C.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	Figure
I_{DD1}	AC Supply Current 20 Mbps	V_{DD} = 5 V, EN = 5 V, C_L = 15 pF, V_{IN} = 5 V Square Wave	−	8.3	13.6	mA	3, 4
I_{DD2}				14.2	15.2		
I_{DD1}		V_{DD} = 3.3 V, EN = 3.3 V, C_L = 15 pF, V_{IN} = 3.3 V Square Wave		8.2	12.2		
I_{DD2}				11.9	13.2		
I_{DD1}		V_{DD} = 2.5 V, EN = 2.5 V, C_L = 15 pF, V_{IN} = 2.5 V Square Wave		8.1	11.6		
I_{DD2}				11.1	12.7		

SWITCHING CHARACTERISTICS
Apply over all recommended conditions, T_A = −40°C to +125°C unless otherwise specified. All typical values are measured at T_A = 25°C.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	Figure
t_{PHL}							

TYPICAL PERFORMANCE CHARACTERISTICS

Figure 3. Supply Current vs. Data Rate (No Load)

Figure 4. Supply Current vs. Data Rate (Load = 15 pF)

Figure 5. Supply Voltage UVLO Threshold vs. Ambient Temperature

Figure 6. Propagation Delay vs. Ambient Temperature

TEST CIRCUITS

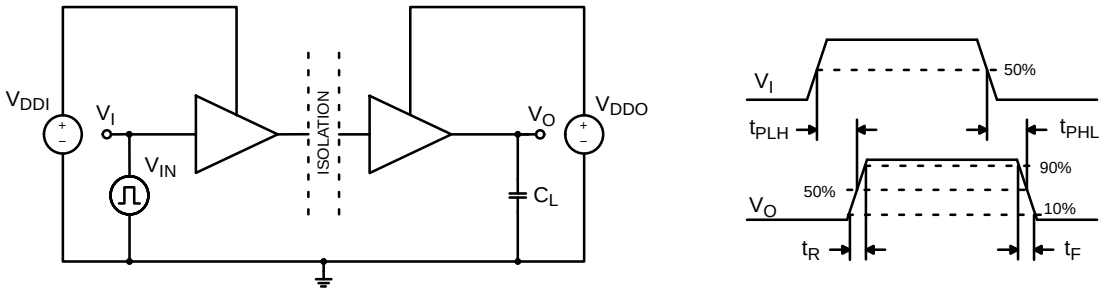

Figure 9. V_{IN} to V_O Propagation Delay Test Circuit and Waveform

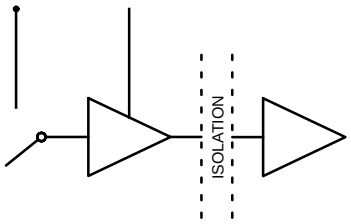

Figure 10. Common Mode Transient Immunity Test Circuit

NCID9200

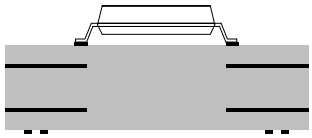

Figure 14. 4−Layer PCB for Digital Isolator

Figure 15. Placement of Bypass Capacitors

SOIC16 W