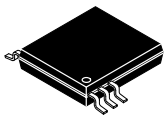


June, 2024 – Rev. 4

NCD9830

Table 4. ELECTRICAL CHARACTERISTICS ±2.7 V

T_A = −40°C to +125°C, V_{DD} = 2.7 V, V_{REF} = 2.5 V, SCL Freq = 3.4 MHz, unless otherwise noted.

Parameter	Test Conditions	Min	Typ	Max	Unit
ANALOG INPUT					
Full scale input range					

Table 4. ELECTRICAL CHARACTERISTICS ±2.7 V

T_A = −40°C to +125°C, V_{DD} = 2.7 V, V_{REF} = 2.5 V, SCL Freq = 3.4 MHz, unless otherwise noted.

Parameter		Test Conditions	Min	Typ	Max	Unit
DIGITAL INPUT/OUTPUT						
Logic Levels:	V_{IH}		0.7 x V_{DD}		V_{DD} + 0.5	V
	V_{IL}		0		0.3 x V_{DD}	V
	V_{OL}	Minimum 3 mA sink current			0.4	V
Input Leakage:	I_{IH}	$V_{IH} = V_{DD} + 0.5$			10	μA
	I_{IL}	V_{IL} = 0 V	−10			μA
POWER SUPPLY REQUIREMENTS						
V_{DD}			2.7		3.6	V
Quiescent Current		High speed mode: SCL = 3.4 MHz		225	320	μA
		Fast mode: SCL = 400 kHz		100		μA
		Standard mode: SCL = 100 kHz		60		μA
Power Dissipation		High speed mode: SCL = 3.4 MHz		675	1000	μW
		Fast mode: SCL = 400 kHz		300		μW
		Standard mode: SCL = 100 kHz		180		μW
Power Down Mode (Wrong address selected)		High speed mode: SCL = 3.4 MHz		70		μA
				25		

Table 5. ELECTRICAL CHARACTERISTICS ±5 V

T_A = −40°C to +125°C, V_{DD} = 5 V, V_{REF} = 5 V (external), SCL Freq = 3.4 MHz, unless otherwise noted.

Parameter	Test Conditions	Min	Typ	Max	Unit
SAMPLING DYNAMICS					
Throughput Frequency	High speed mode: SCL = 3.4 MHz			70	kSPS
	Fast mode: SCL = 400 kHz			10	kSPS
	Standard mode: SCL = 100 kHz			2.5	kSPS
Conversion Time			5		μs
AC ACCURACY					
Total Harmonic Distortion	V_{IN} = 2.5 Vpp at 1 kHz		−72		dB
Signal−to−Ratio	V_{IN} = 2.5 Vpp at 1 kHz		50		dB
Signal−to−(Noise+Distortion) Ratio	V_{IN} = 2.5 Vpp at 1 kHz		49		dB
Spurious Free Dynamic Range	V_{IN} = 2.5 Vpp at 1 kHz		68		dB
Channel to channel isolation			90		dB
VOLTAGE REFERENCE OUTPUT					
Range		2.475	2.5	2.525	V
Internal Reference Drift			15		ppm/°C
Output Impedance	Internal reference ON		700		Ω
	Internal reference OFF		1		GΩ
Quiescent Current	Internal Reference ON, SCL and SDA pulled HIGH		1300		μA
VOLTAGE REFERENCE INPUT					
Range		0.05		V_{DD}	V
Resistance			1		GΩ
Current Drain	High Speed Mode: SCL = 3.4 MHz		20		μA
DIGITAL INPUT/OUTPUT					
Logic Levels: V_{IH}		0.7 x V_{DD}		V_{DD} + 0.5	V
V_{IL}		0		0.3 x V_{DD}	V
V_{OL}	Minimum 3 mA sink current			0.4	V
Input Leakage: I_{IH}	V_{IH} = V_{DD} + 0.5			10	μA
I_{IL}	V_{IL} = 0 V	−10			μA
POWER SUPPLY REQUIREMENTS					
V_{DD}		4.75		5.25	V
Quiescent Current	High speed mode: SCL = 3.4 MHz		750	1000	μA
	Fast mode: SCL = 400 kHz		300		μA
	Standard mode: SCL = 100 kHz		150		μA
Power Dissipation	High speed mode: SCL = 3.4 MHz		3.75	5	mW
	Fast mode: SCL = 400 kHz		1.5		mW
	Standard mode: SCL = 100 kHz		0.75		mW

Table 5. ELECTRICAL CHARACTERISTICS ±5 V

T_A = −40°C to +125°C, V_{DD} = 5 V, V_{REF} = 5 V (external), SCL Freq = 3.4 MHz, unless otherwise noted.

Parameter	Test Conditions	Min	Typ	Max	Unit
Total Harmonic Distortion	V_{IN} = 2.5 Vpp at 1 kHz		−72		dB
POWER SUPPLY REQUIREMENTS					
Power Down Mode (Wrong address selected)	High speed mode: SCL = 3.4 MHz		400		μA
	Fast mode: SCL = 400 kHz		150		μA
	Standard mode: SCL = 100 kHz		35		μA
Full Power Down	SCL, SDA pulled HIGH TA = −40°C to 85°C TA = −40°C to 125°C		 400 400	 3000 3500	nA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

TIMING CHARACTERISTICS

Table 6. I²C TIMING

Parameter (Note 3)	Symbol	Conditions	Min	Max	Unit
Clock Frequency	f_{SCL}	Standard Mode Fast Mode High speed Mode (100 pF) High speed Mode (400 pF)	10	100 400 3.4 1.7	kHz kHz MHz MHz
Bus Free Time	t_{BUF}	Standard Mode Fast Mode	4.7 1.3		µs µs
Start Hold Time (Note 4)	$t_{HD;STA}$	Standard Mode Fast Mode High speed Mode	4.0 600 160		µs ns ns
SCL Low Time	t_{LOW}	Standard Mode Fast Mode High speed Mode (100 pF) High speed Mode (400 pF)	4.7 1.3 160 320		µs µs ns ns
SCL High Time	t_{HIGH}	Standard Mode Fast Mode High speed Mode (100 pF) High speed Mode (400 pF)	4.0 600 60 120		µs ns ns ns
Start Setup Time	$t_{SU;STA}$	Standard Mode Fast Mode High speed Mode	4.7 600 160		µs ns ns
Data Setup Time (Note 5)	$t_{SU;DAT}$	Standard Mode Fast Mode High speed Mode	250 100 10		ns
Data Hold Time (Note 6)	$t_{HD;DAT}$	Standard Mode Fast Mode High speed Mode (100 pF) High speed Mode (400 pF)	0 0 0 0	3.45 0.9 70 150	µs µs ns ns
SCL Rise Time	t_{RCL}	Standard Mode Fast Mode High speed Mode (100 pF) High speed Mode (400 pF)	 $20+0.1C_B$ 10 20	1000 300 40 80	ns ns ns ns
SCL Rise Time (after repeated start)	t_{RCL1}	Standard Mode Fast Mode High speed Mode (100 pF) High speed Mode (400 pF)	 $20+0.1C_B$ 10 20	1000 300 80 160	ns ns ns ns
SCL Fall Time	t_{FCL}	Standard Mode Fast Mode High speed Mode (100 pF) High speed Mode (400 pF)	 $20+0.1C_B$ 10 20	300 300 40 80	ns ns ns ns
SDA Rise Time	t_{RDA}	Standard Mode Fast Mode High speed Mode (100 pF) High speed Mode (400 pF)	 $20+0.1C_B$ 10 20	1000 300 80 160	ns ns ns ns
SDA Fall Time	t_{FDA}	Standard Mode Fast Mode High speed Mode (100 pF) High speed Mode (400 pF)	 $20+0.1C_B$ 10 20	300 300 80 160	ns ns ns ns
Stop Setup Time	$t_{SU;STO}$	Standard Mode Fast Mode High speed Mode	0.4 600 160		µs ns ns
Capacitive load	C_B			400	pF

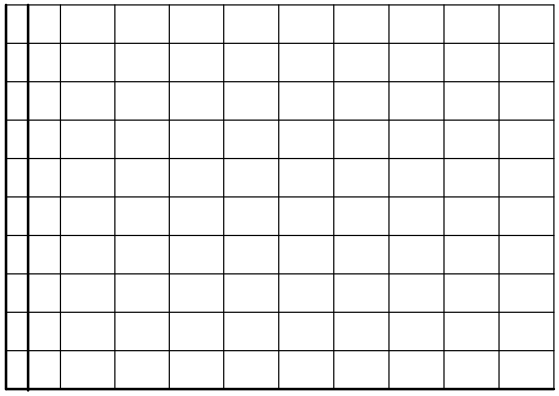
3. Guaranteed by design, but not production tested.
4. Time from 10% of SDA to 90% of SCL.
5. Time for 10%or 90% of SDA to 10% of SCL.
6. A device must internally provide a hold time of at least 300 ns for the SDA signal to bridge the undefined region of the falling edge of SCL.

Table 6. I^2C TIMING

Parameter (Note 3)

TYPICAL CHARACTERISTICS

T_A = +25°C, V_{DD} = +2.7 V, V_{REF} = External 2.5 V, f_{SAMPLE} = 50 kHz, unless otherwise stated.



TYPICAL CHARACTERISTICS

T_A = +25°C, V_{DD} = +2.7 V, V_{REF} = External 2.5 V, f_{SAMPLE} = 50 kHz, unless otherwise stated.

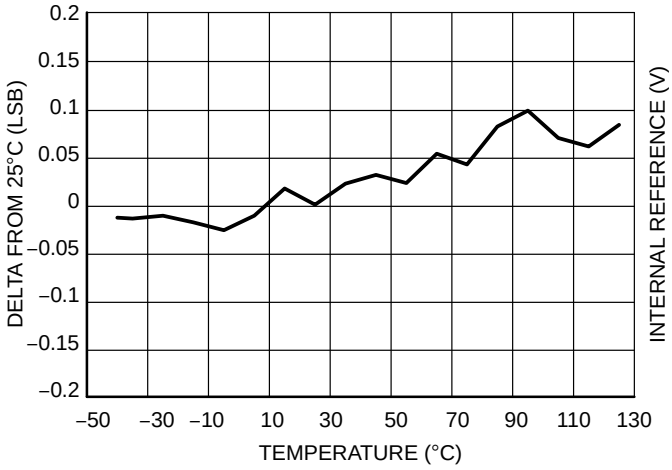


Figure 10. Change in Gain vs. Temperature

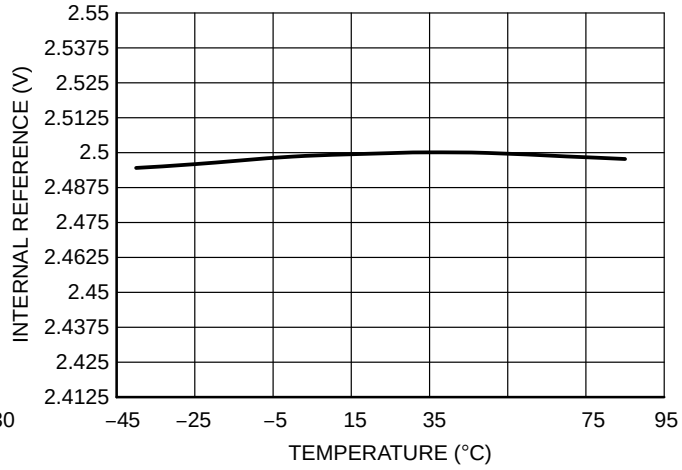


Figure 11. Internal V_{REF} vs. Temperature

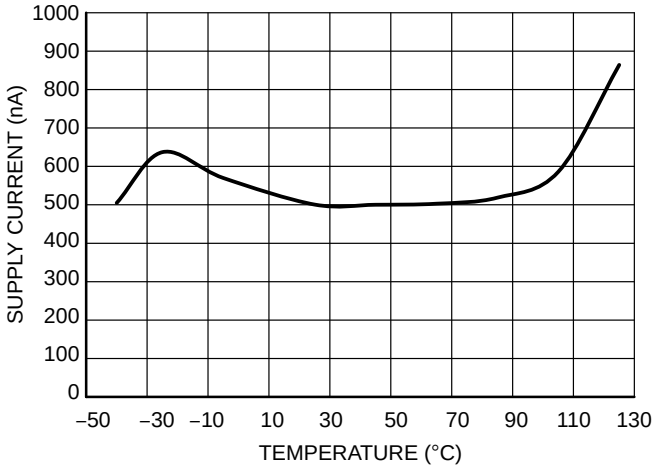


Figure 12. Power−Down Supply Current vs. Temperature

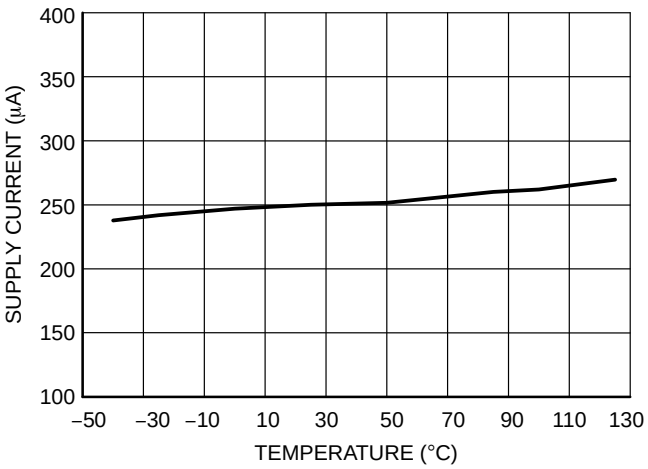
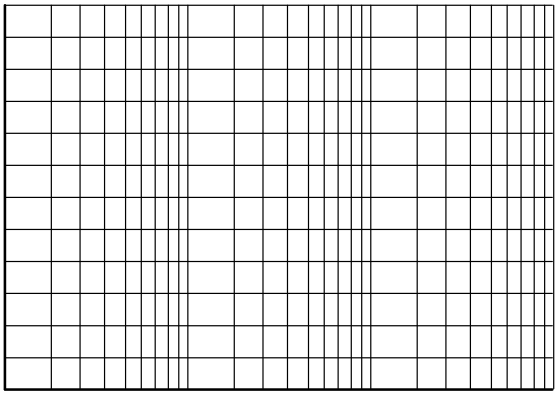


Figure 13. Supply Current vs. Temperature



CIRCUIT INFORMATION

OPERATION

The NCD9830 is a low power successive approximation ADC with a built in 8 channel multiplexer and 8 bit resolution. The 8 bit resolution assures high noise immunity and fast digitization that makes this device suitable for medium to high speed applications. The device internal circuitry operates at speed higher than the conversion time of the device because of the binary algorithm used. The algorithm is based on approximating the input signal by comparing with successive analog signal generated from the built in DAC.

The device can be operated at supply voltages of 2.7 V and 5 V. The liberty of supply voltage variation must be used with appropriate reference voltage selection. The NCD9830 internal DAC can be configured with an externally (50 mV ĭ5 V) supplied or an internally internally generated reference voltage of 2.5 V. However, to avail full dynamic range an external reference of 5 V must be used while operating the device at 5 V supply voltage. The internal 2.5 V reference voltage is sufficient for full dynamic range while operating the device at 2.7 V.

The value of each output bit is evaluated on the basis of output of the comparator. The converter requires N conversion periods to give N bit digital output of the input analog signal. The SAR register stores the digital equivalent bits of the input analog signal and can be read by the master device using an I^2C interface. The main building block of the device are

i. Digital to Analog Converter

ii. Comparator

iii. Digital Logic

DIGITAL TO ANALOG CONVERTER

A charge scaling DAC is used due to its compatibility with the switch capacitor circuits. The DAC operation consists of two phases called acquisition phase and the conversion phase. The acquisition phase is analogous to sample and hold circuit while the conversion phase is the process of conversion of the internal digital word in to an analog output.

Acquisition phase: The top plates of all the capacitors on the array are connected to the ground and the bottom plates are connected to the applied voltage Vin. Thus there is a charge proportional to input voltage on the capacitor array. After acquisition the top and bottom plates are disconnected from their respective connections.

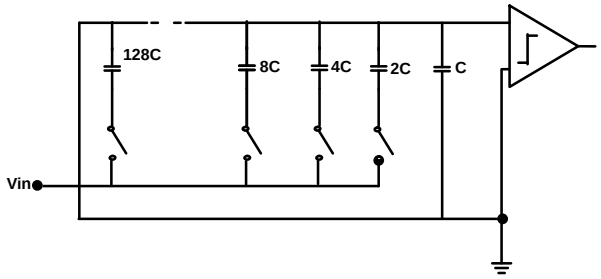


Figure 16. The Acquisition Phase of a Typical ADC

Conversion Phase: The conversion phase is administered by a two phase non overlapping clock with phases ϕ_1 and ϕ_2 respectively.

During ϕ_1 the bottom plates of all the capacitors are grounded i.e the top plates of all the capacitors are now Vin times higher than the ground. As the conversion process starts the digital c(t)14.5t5 1 Tf3.2769 0 87lSBT.8348periods to e the top p

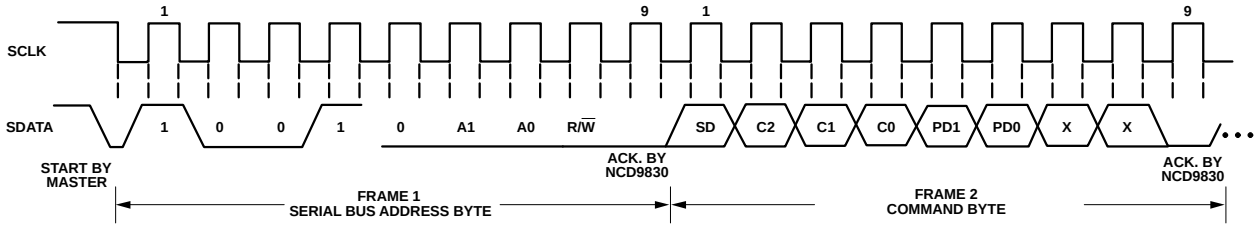
MSB	6	5	4	3	2	1	0
SD	C2	C1	C0	PD1	PD0	x	x

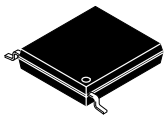
Bit 7: SD ĭ this configures the type of input to be used. If set to 0 then the device performs a differential measurement. If 7:s a used. If set

INITIATING CONVERSIONS

Communication in Standard/Fast Mode

Communication in standard/fast mode corresponds to a clock speed of 100/400 kHz. The device address is sent over the bus followed by R/W set to 0. This is followed by the Command byte. If the Command byte is correct the device initiates the conversion cycle by turning on the converter circuit after it receives the channel selection bits (SD, C_2-C_0) of the Command byte. After receiving the Command byte the NCD 9830 sends an acknowledge bit. The device is now ready to be read by the master.





SCALE 2:1

TSSOP−16 WB
CASE 948F
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